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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207rbt6c

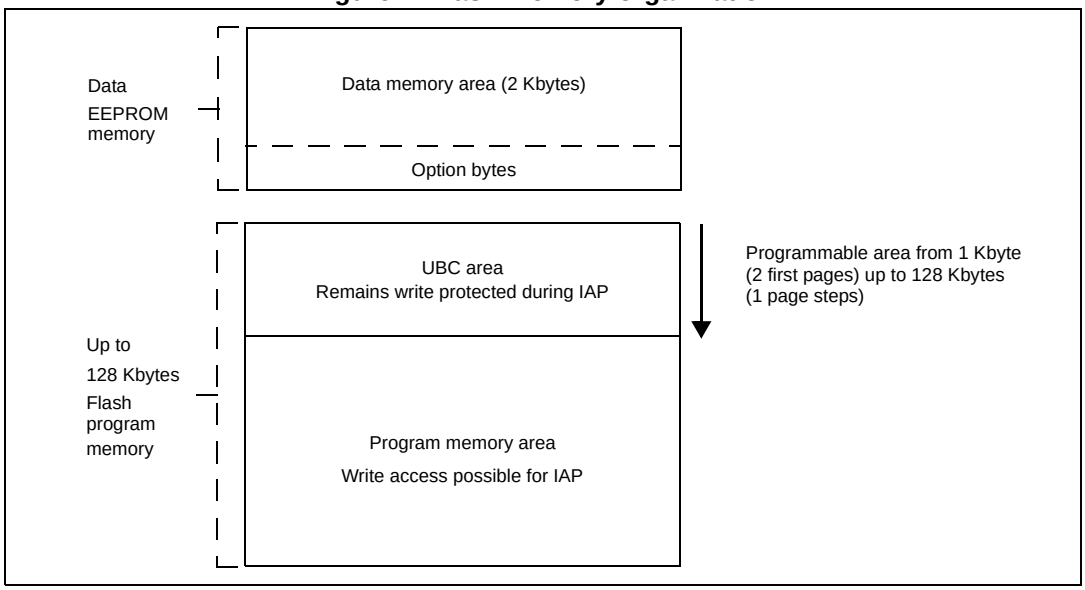
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15%
- Sync delimiter checking
- 11-bit LIN sync break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.4 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

4.14.5 beCAN

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the beCAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

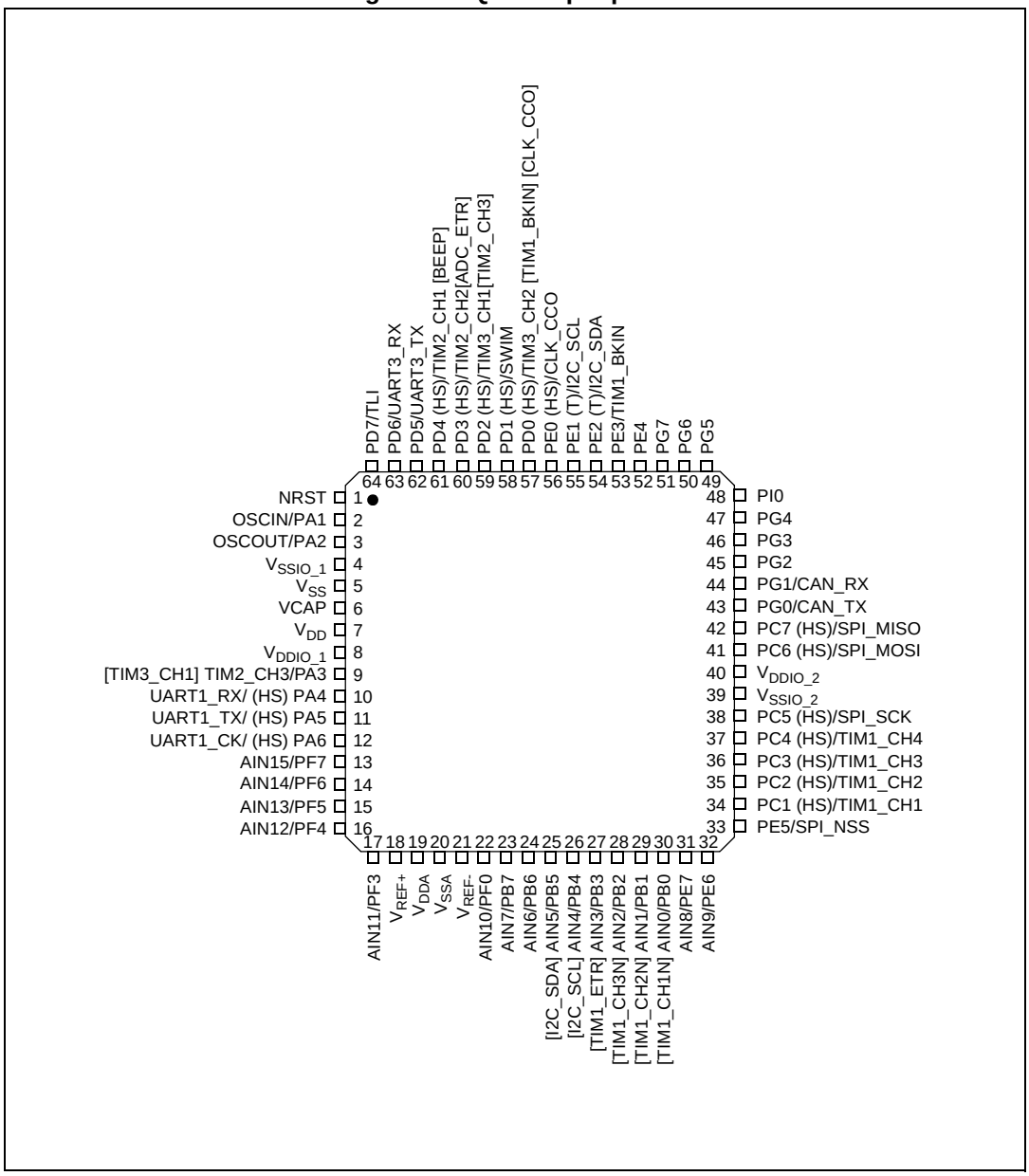
Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

Reception

- 8-, 11- and 29-bit ID
- One receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- Six filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
  - Mask mode permitting ID range filtering
  - ID list mode
- Time triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time stamp sent in last two data bytes

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0x00
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0x00
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0x00
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5216	I²C	I2C_DR	I²C data register	0x00
0x00 5217		I2C_SR1	I²C status register 1	0x00
0x00 5218		I2C_SR2	I²C status register 2	0x00
0x00 5219		I2C_SR3	I²C status register 3	0x00
0x00 521A		I2C_ITR	I²C interrupt control register	0x00
0x00 521B		I2C_CCRL	I²C clock control register low	0x00
0x00 521C		I2C_CCRH	I²C clock control register high	0x00
0x00 521D		I2C_TRISER	I²C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	UART3	UART3_SR	UART3 status register	C0h
0x00 5241		UART3_DR	UART3 data register	0xXX
0x00 5242		UART3_BRR1	UART3 baud rate register 1	0x00
0x00 5243		UART3_BRR2	UART3 baud rate register 2	0x00
0x00 5244		UART3_CR1	UART3 control register 1	0x00
0x00 5245		UART3_CR2	UART3 control register 2	0x00
0x00 5246		UART3_CR3	UART3 control register 3	0x00
0x00 5247		UART3_CR4	UART3 control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	UART3 control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 13. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wakeup unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles
OPT6	Reserved
OPT7	**WAITSTATE** *Wait state configuration* This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 1 wait state is required if f_{CPU} > 16 MHz. 0: No wait state 1: 1 wait state

Total current consumption in halt mode

Table 26. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C	Max at 125 °C	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63.5			µA
		Flash in power-down mode, HSI clock after wakeup	6.5	35	100	

Table 27. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	61.5	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	

Low power mode wakeup times

Table 28. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(3)					See note(2)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz.			0.56		
$t_{WU(AH)}$	Wakeup time active halt mode to run mode.(3)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
			Flash in power-down mode(5)		3(6)		
		MVR voltage regulator off(4)	Flash in operating mode(5)		48(6)		
			Flash in power-down mode(5)		50(6)		
$t_{WU(H)}$	Wakeup time from halt mode to run mode(3)	Flash in operating mode(5)			52		
		Flash in power-down mode(5)			54		

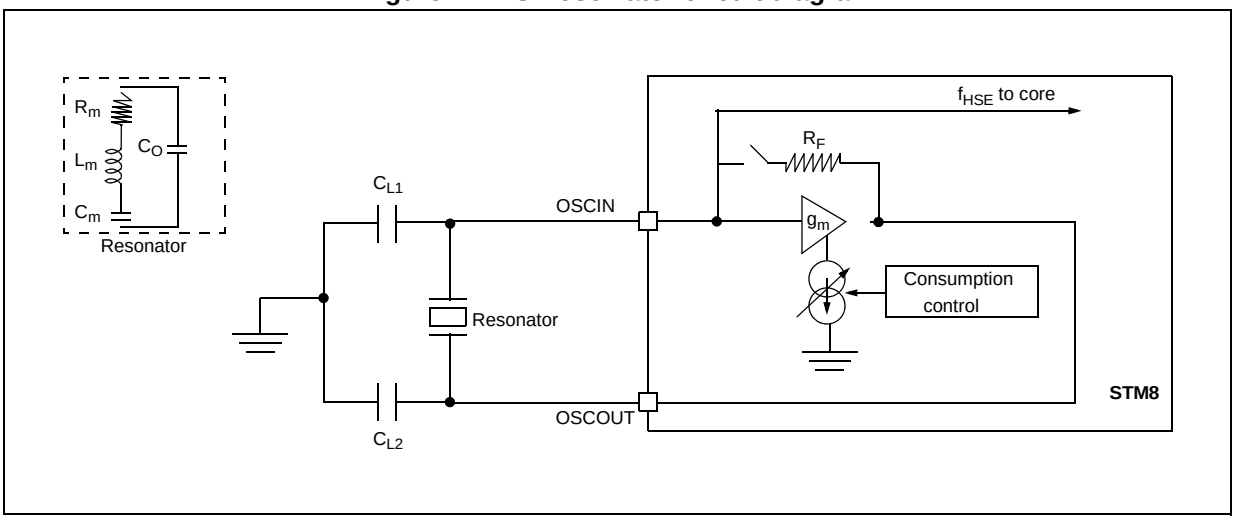
1. Data guaranteed by design, not tested in production.
2. $t_{WU(WFI)} = 2 \times 1/f_{master} + 7 \times 1/f_{CPU}$
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		24	MHz
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz			6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz			6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

High speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions	-1.0(1)		1.0	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-1.5		1.5	
		V_{DD} = 5 V, 25 °C ≤ T_A ≤ 85 °C	-2.2		2.2	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3.0(2)		3.0(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration				1.0(1)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(2)	µA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production

Figure 18. Typical HSI frequency variation vs V_{DD} at 4 temperatures

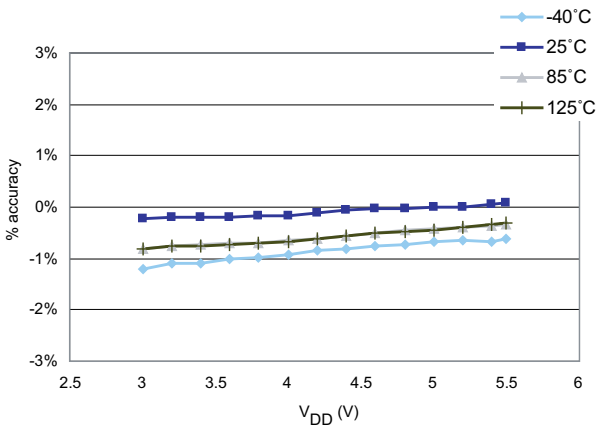


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)

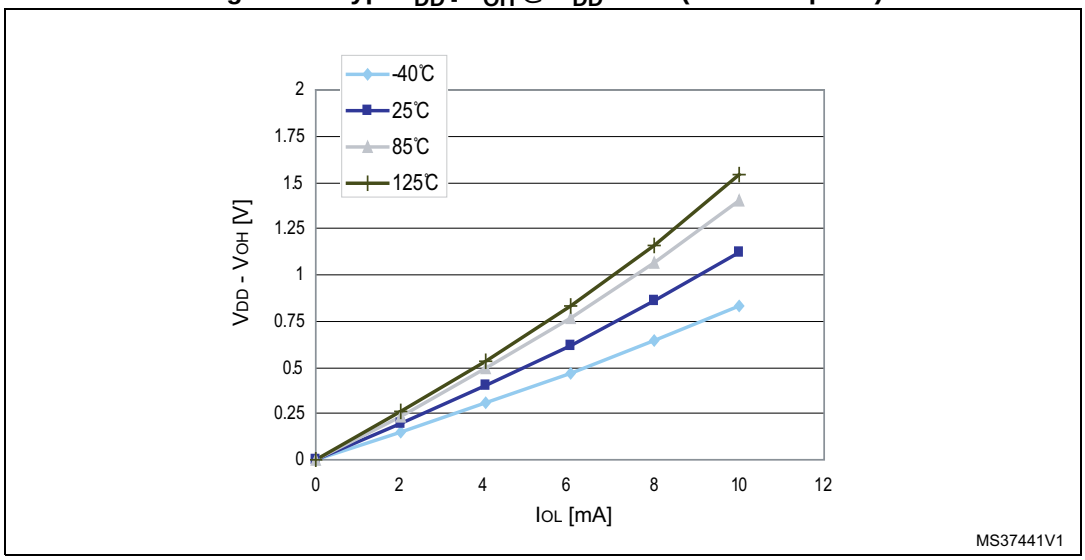


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

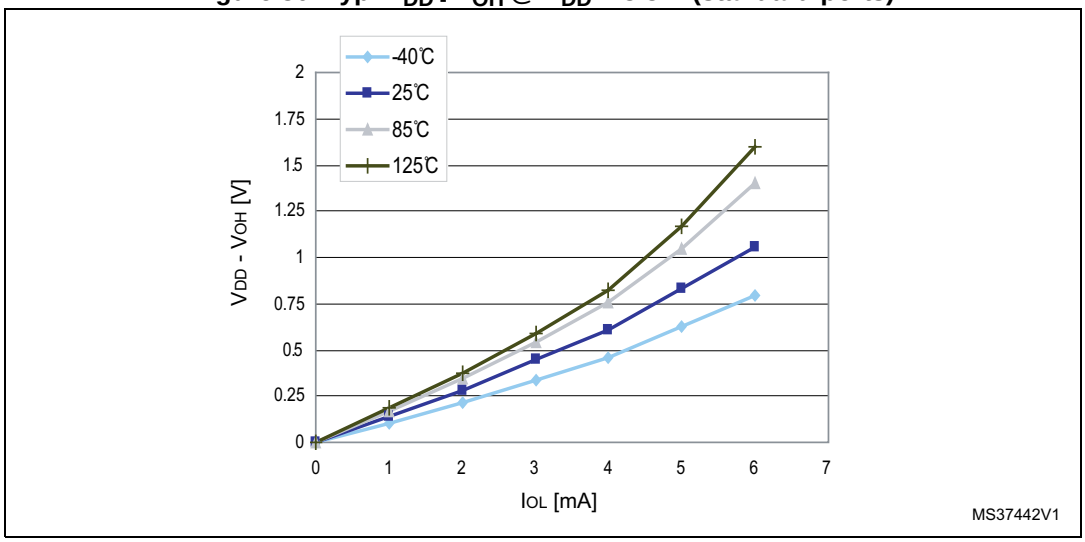


Figure 34. Typical NRST pull-up resistance vs V_{DD} @ 4 temperatures

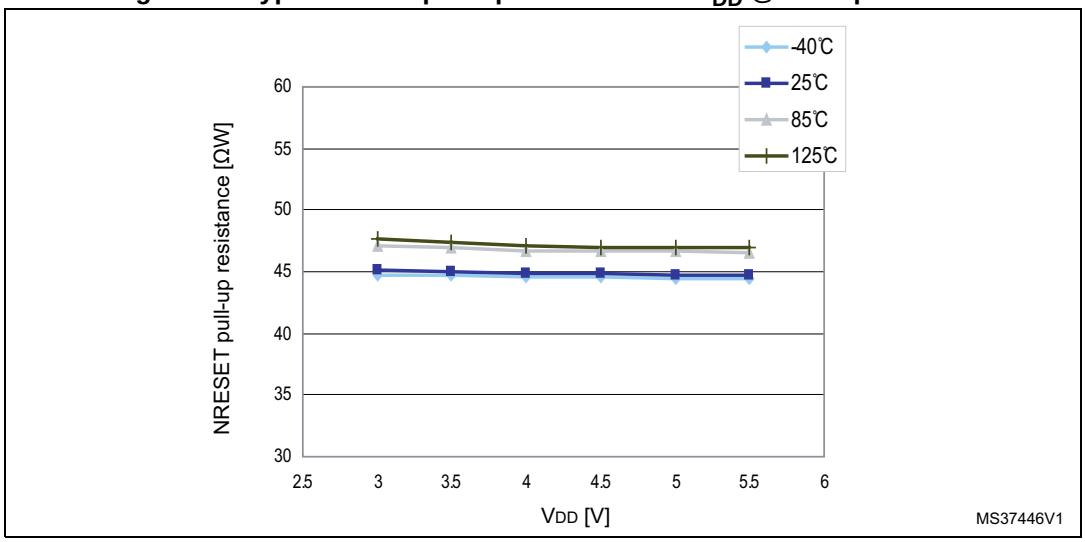
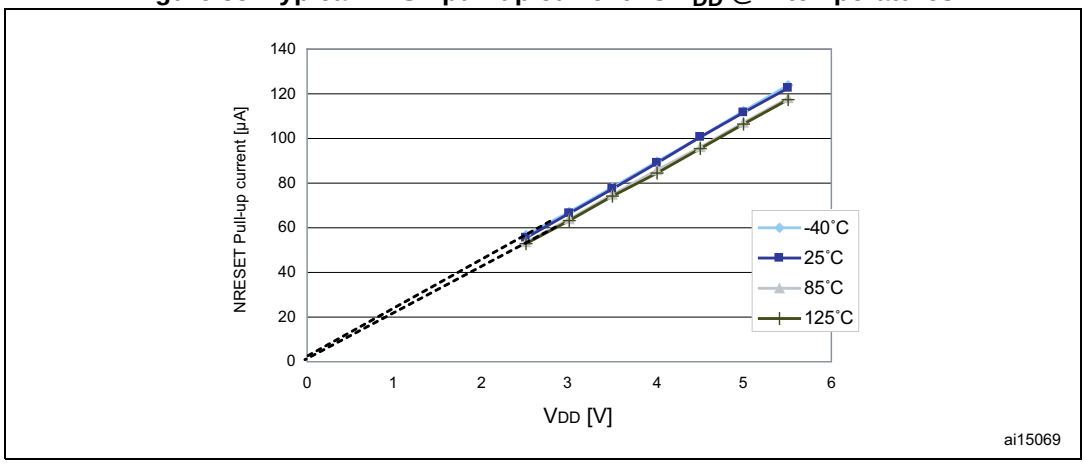
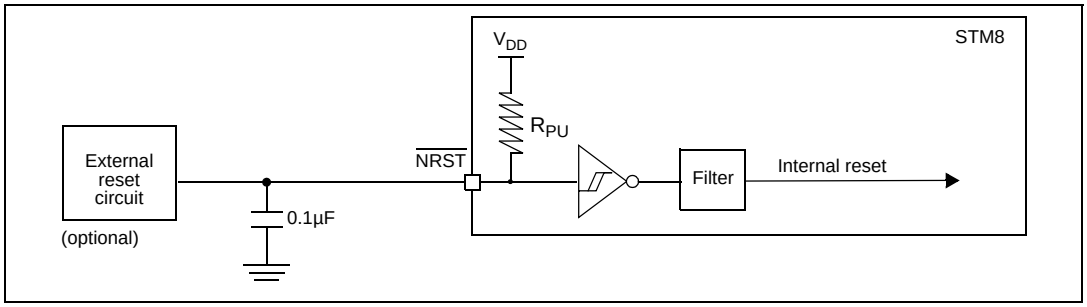


Figure 35. Typical NRST pull-up current vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 36* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 41*. Otherwise the reset is not taken into account internally. For power consumption sensitive applications, the capacity of the external reset capacitor can be reduced to limit charge/discharge current. If the NRSTsignal is used to reset the external circuitry, care must be taken of the charge/discharge time of the external capacitor to fulfill the external device's reset timing conditions. The minimum recommended capacity is 10 nF.

Figure 36. Recommended reset pin protection



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

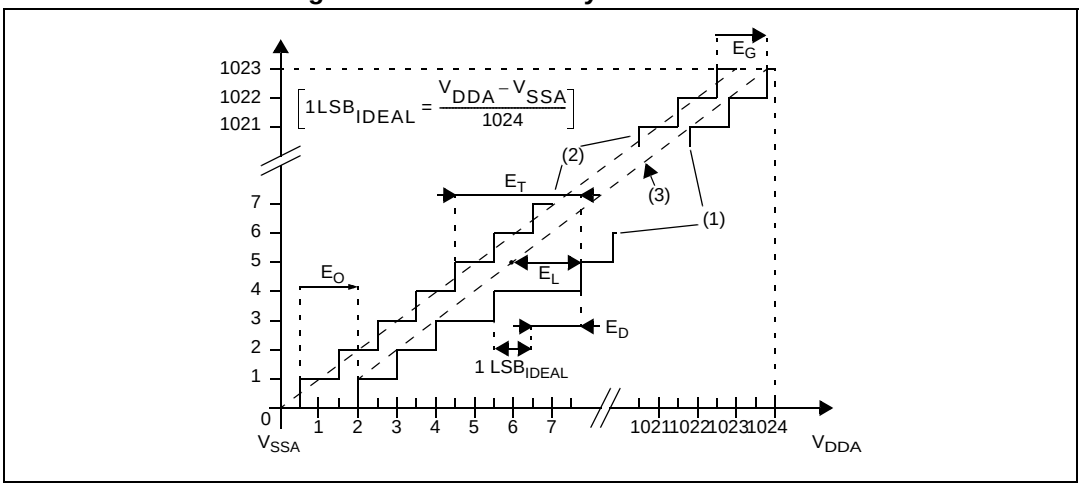
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC

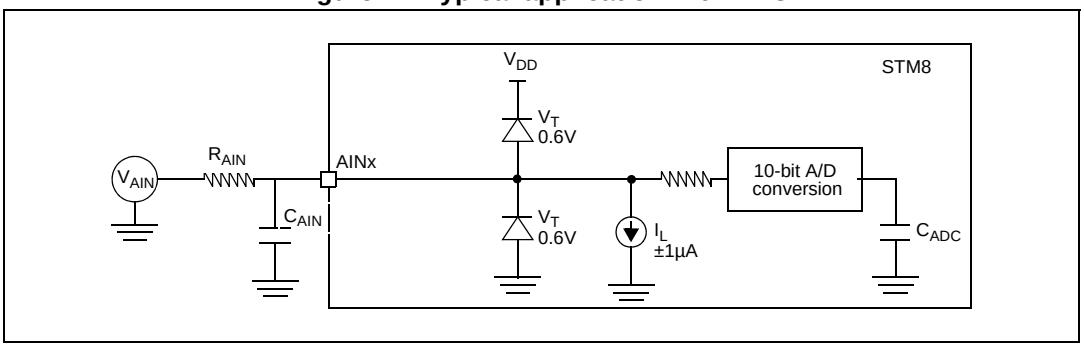
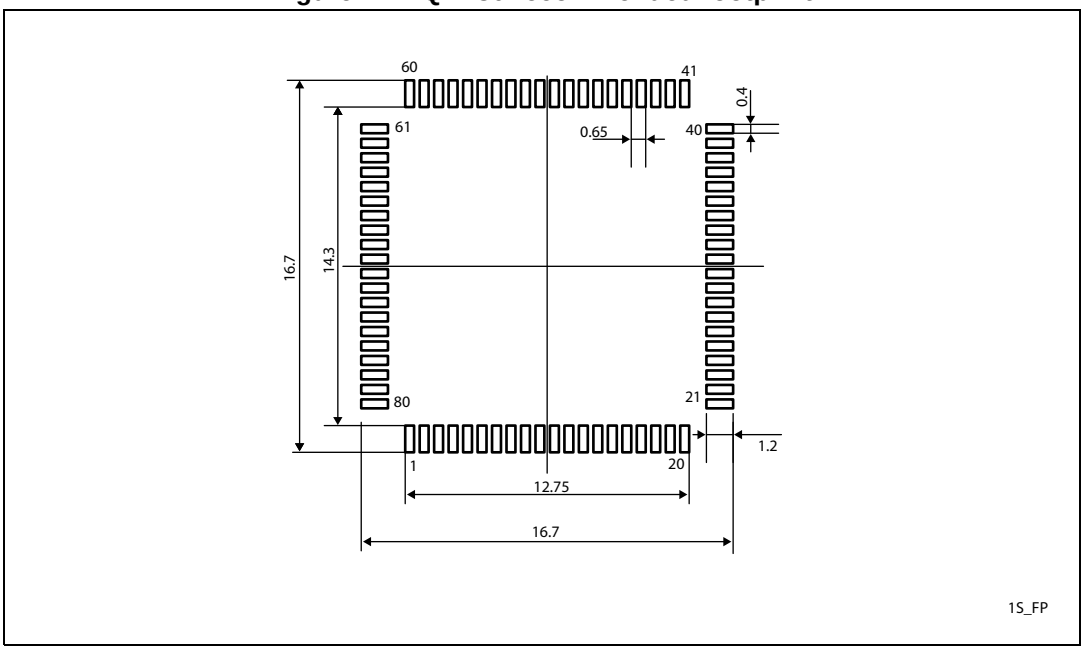


Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1) (continued)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.350	-	-	0.4862	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.350	-	-	0.4862	-
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

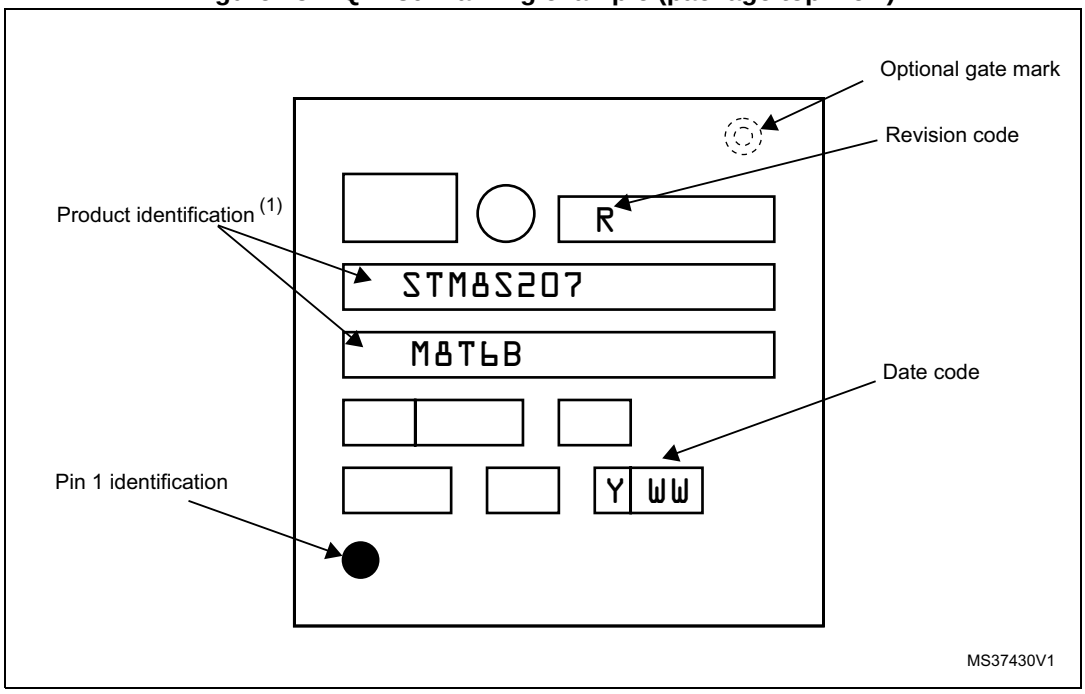
Figure 44. LQFP80 recommended footprint



Device marking

The following figure shows the marking for the LQFP80 package.

Figure 45. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.1.2 LQFP64 package information

Figure 46. LQFP64 - 64-pin 14 mm x 14 mm low-profile quad flat package outline

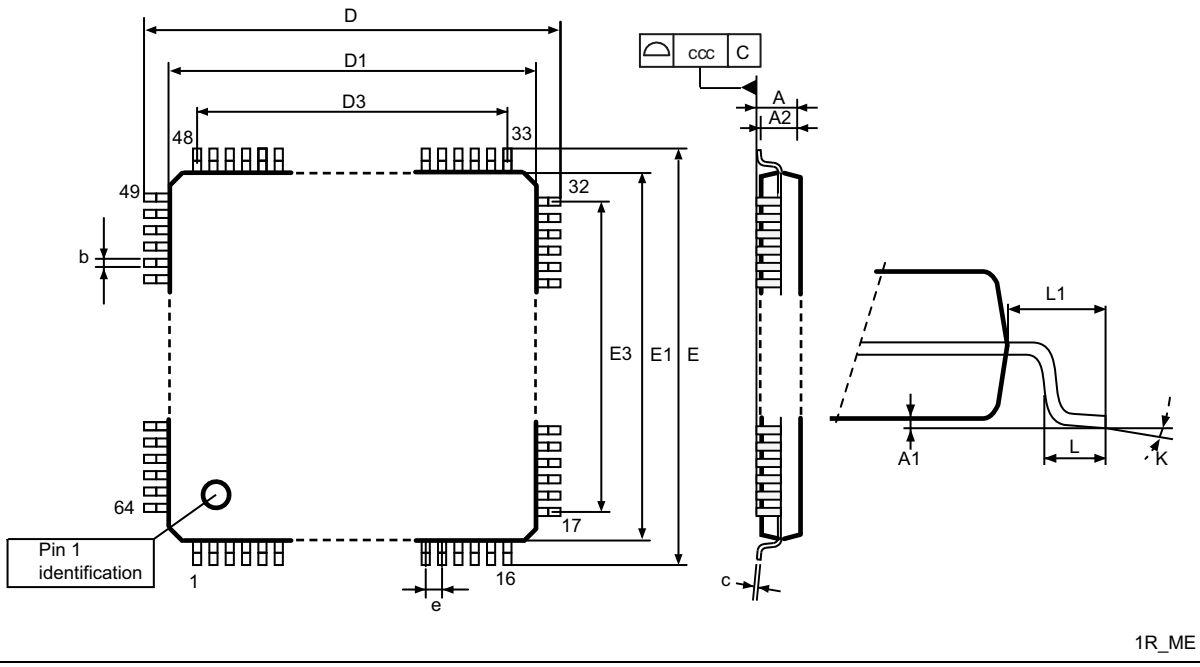


Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical data

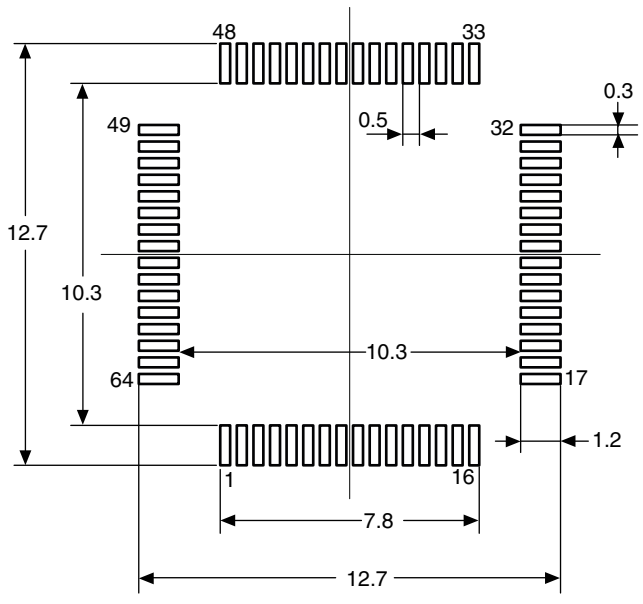
Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



11.1.4 LQFP44 package information

Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline