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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207rbt6tr

List of figures

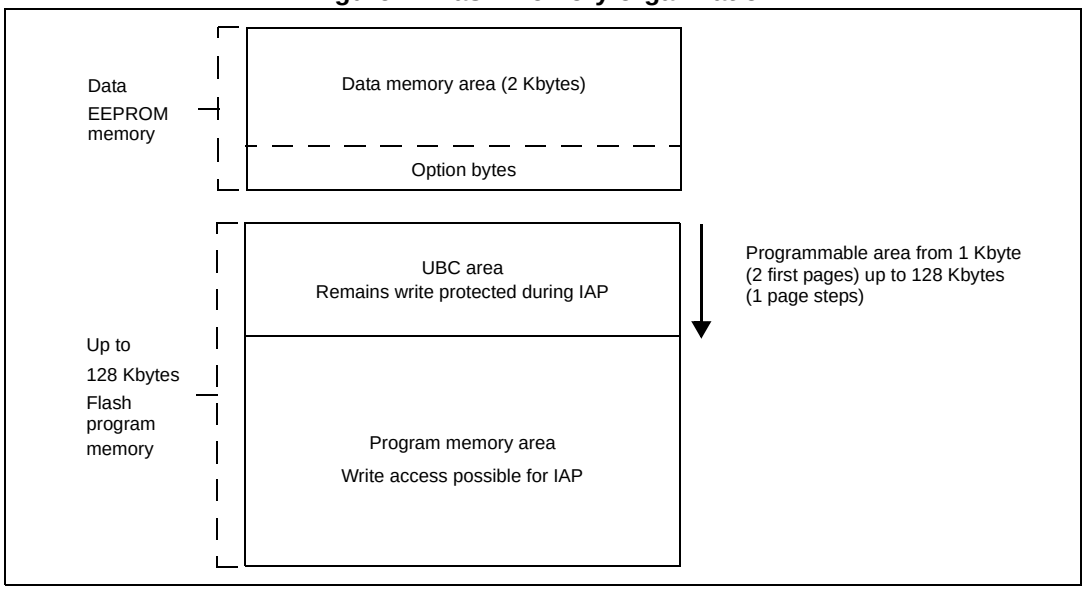
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

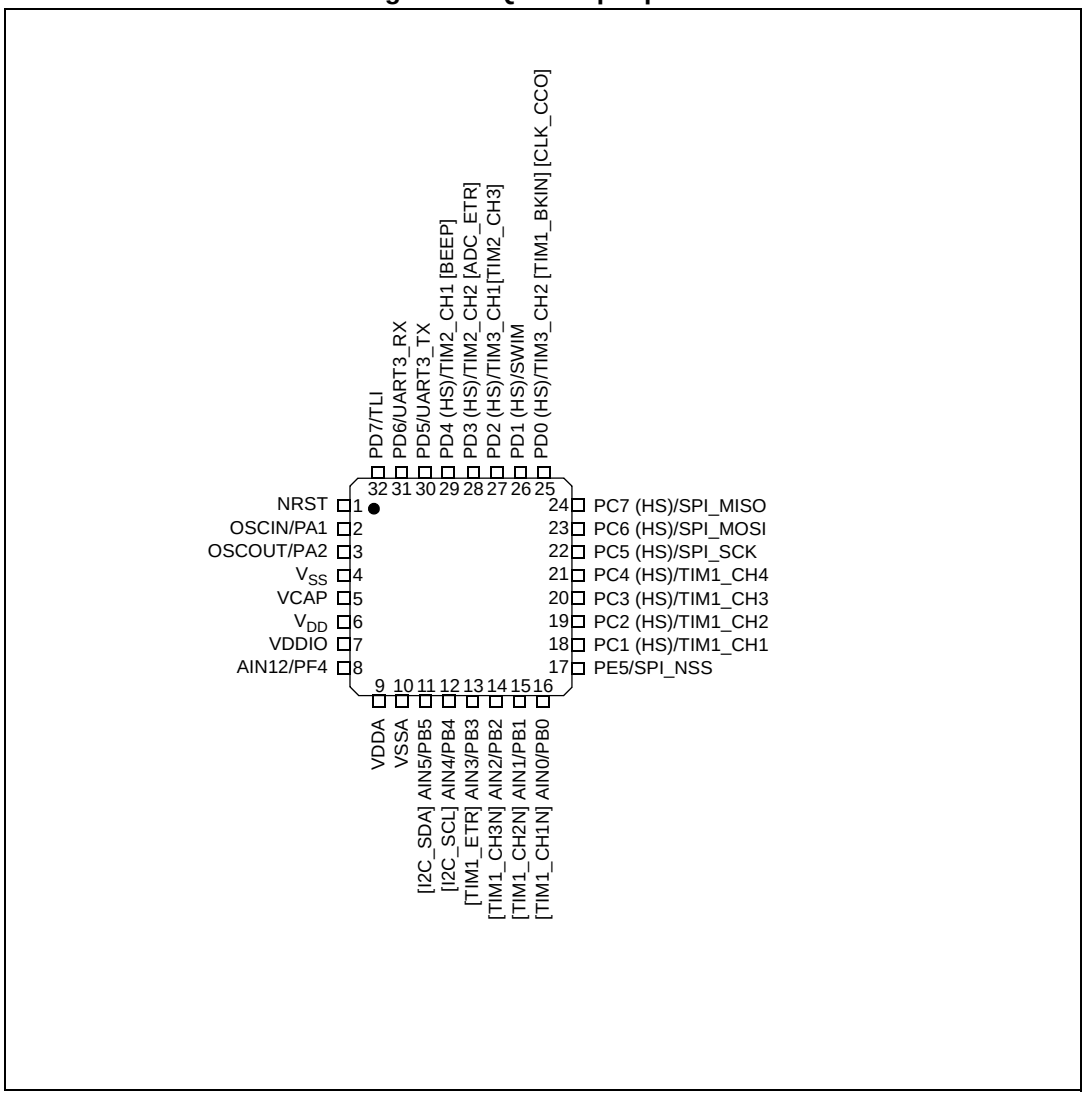
LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15%
- Sync delimiter checking
- 11-bit LIN sync break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

Figure 7. LQFP 32-pin pinout



1. (HS) high sink capability.
2. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
69	55	39	35	-	PE1/I^{2}C_SCL	I/O	**X**		X		O1	T(3)		**Port E1**	I^{2}C clock	
70	56	40	36	-	PE0/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port E0**	Configurable clock output	
71	-	-	-	-	PI6	I/O	**X**	X			O1	X	X	**Port I6**		
72	-	-	-	-	PI7	I/O	**X**	X			O1	X	X	**Port I7**		
73	57	41	37	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	38	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
75	59	43	39	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	40	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	41	29	PD4/TIM2_CH1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
78	62	46	42	30	PD5/ UART3_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART3 data transmit	
79	63	47	43	31	PD6/ UART3_RX(1)	I/O	**X**	X	X		O1	X	X	**Port D6**	UART3 data receive	
80	64	48	44	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CH4 [AFR4](5)

1. The default state of UART1_RX and UART3_RX pins is controlled by the ROM bootloader. These pins are pulled up as part of the bootloader activation process and returned to the floating state before a return from the bootloader.
2. The beCAN interface is available on STM8S208xx devices only
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.
5. Available in 44-pin package only. On other packages, the AFR4 bit is reserved and must be kept at 0.

5.2 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function

Table 7 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 7. Flash, Data EEPROM and RAM boundary addresses

Memory area	Size (bytes)	Start address	End address
Flash program memory	128 K	0x00 8000	0x02 7FFF
	64 K	0x00 8000	0x01 7FFF
	32 K	0x00 8000	0x00 FFFF
RAM	6 K	**0x00 0000**	0x00 17FF
	4 K	**0x00 0000**	0x00 1000
	2 K	**0x00 0000**	0x00 07FF
Data EEPROM	2048	0x00 4000	**0x00 47FF**
	1536	0x00 4000	**0x00 45FF**
	1024	0x00 4000	**0x00 43FF**

6.2 Register map

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0x00
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0x00
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0x00
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0x00
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0x00
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0x00
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 52*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \leq 105$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	4.4		mA
			HSE user ext. clock (24 MHz)	3.7	7.3(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.3		
			HSE user ext. clock (16 MHz)	2.7	5.8	
			HSI RC osc. (16 MHz)	2.5	3.4	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1(1)	
			HSI RC osc. (16 MHz)	1.0	1.3(1)	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.45		
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	11.4		
			HSE user ext. clock (24 MHz)	10.8	18(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	9.0		
			HSE user ext. clock (16 MHz)	8.2	15.2(1)	
			HSI RC osc.(16 MHz)	8.1	13.2(1)	
		$f_{CPU} = f_{MASTER}$ = 2 MHz.	HSI RC osc. (16 MHz/8)(2)	1.5		
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.1		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 24. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1000		µA
				LSI RC oscillator (128 kHz)	200	260	
			Power-down mode	HSE crystal oscillator (16 MHz)	940		
				LSI RC oscillator (128 kHz)	140		
		Off	Operating mode	LSI RC oscillator 128 kHz)	68		
			Power-down mode		11	45	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source		
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	600	µA
				LSI RC osc. (128 kHz)	200	
			Power-down mode	HSE crystal osc. (16 MHz)	540	
				LSI RC osc. (128 kHz)	140	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	
			Power-down mode		9	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

High speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions	-1.0(1)		1.0	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-1.5		1.5	
		V_{DD} = 5 V, 25 °C ≤ T_A ≤ 85 °C	-2.2		2.2	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3.0(2)		3.0(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration				1.0(1)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(2)	µA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production

Figure 18. Typical HSI frequency variation vs V_{DD} at 4 temperatures

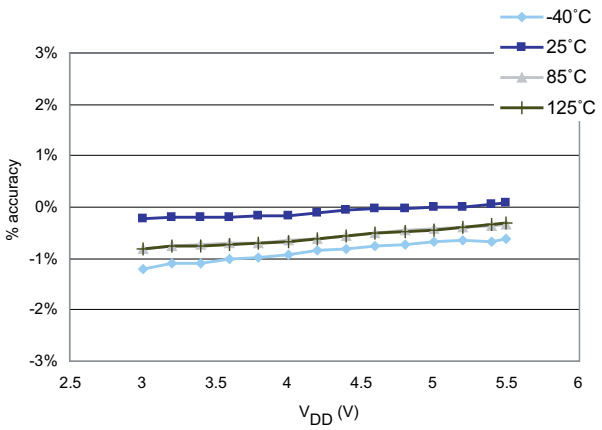
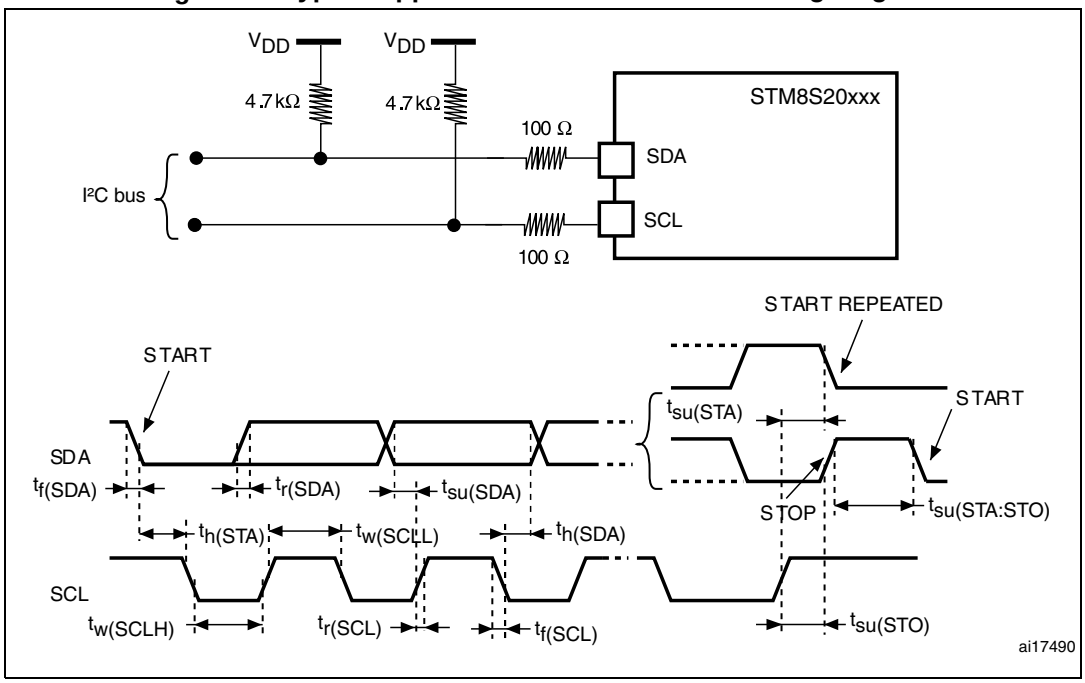


Figure 40. Typical application with I²C bus and timing diagram



1. Measurement points are made at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

10.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 44. ADC characteristics

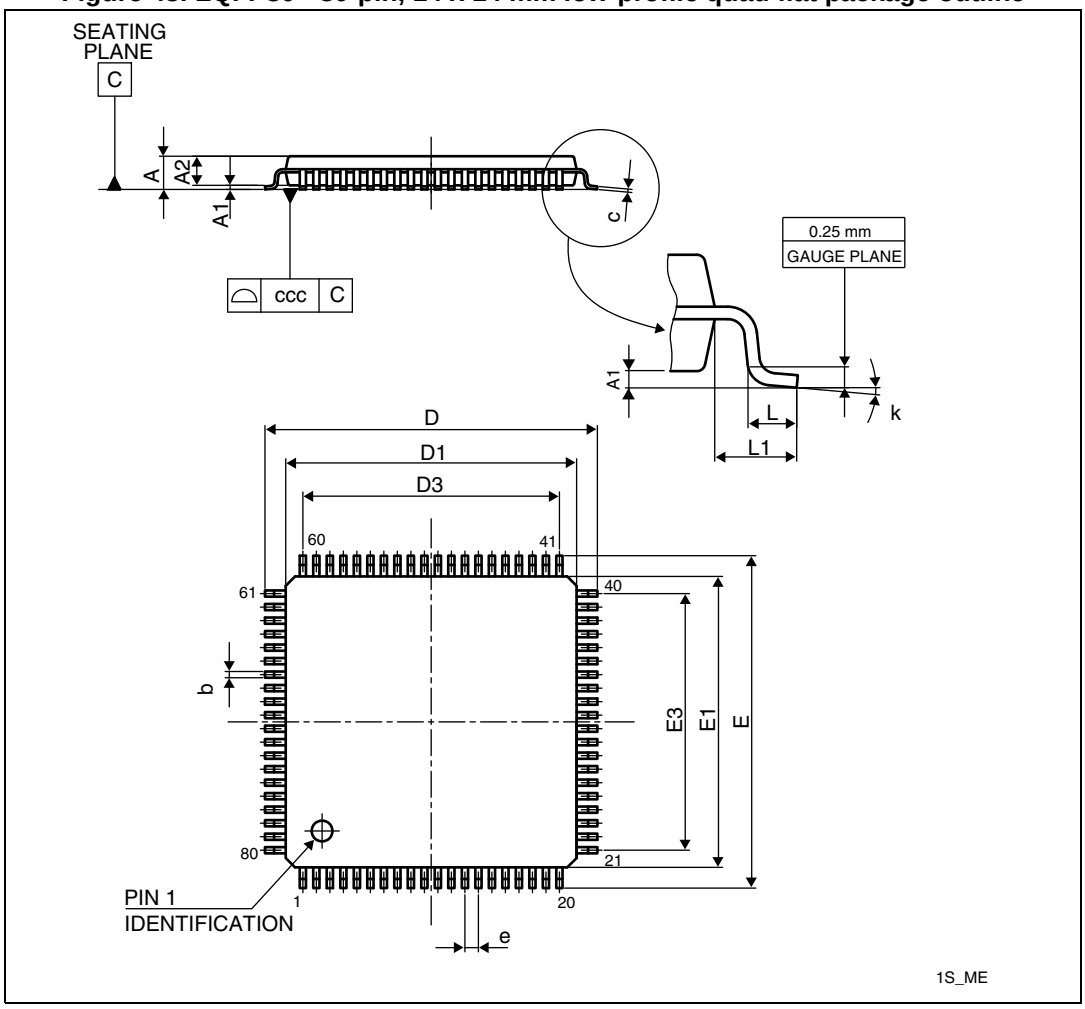
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DDA} = 3 to 5.5 V	1		4	MHz
		V_{DDA} = 4.5 to 5.5 V	1		6	
V_{DDA}	Analog supply		3		5.5	V
V_{REF+}	Positive reference voltage		2.75(1)		V_{DDA}	V
V_{REF-}	Negative reference voltage		V_{SSA}		0.5(1)	V
V_{AIN}	Conversion voltage range(2)		V_{SSA}		V_{DDA}	V
		Devices with external V_{REF+}/V_{REF-} pins	V_{REF-}		V_{REF+}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
t_S(2)	Sampling time	f_{ADC} = 4 MHz	0.75			µs
		f_{ADC} = 6 MHz	0.5			
t_{STAB}	Wakeup time from standby			7		µs
t_{CONV}	Total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
			14			$1/f_{ADC}$

1. Data guaranteed by design, not tested in production.
2. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

11.1 Package information

11.1.1 LQFP80 package information

Figure 43. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)

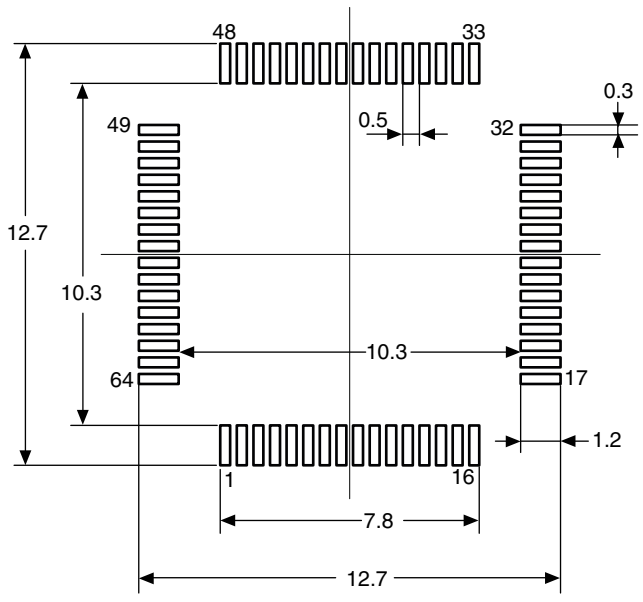
Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090	-	0.200	0.0035	-	0.0079

Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



11.1.4 LQFP44 package information

Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline

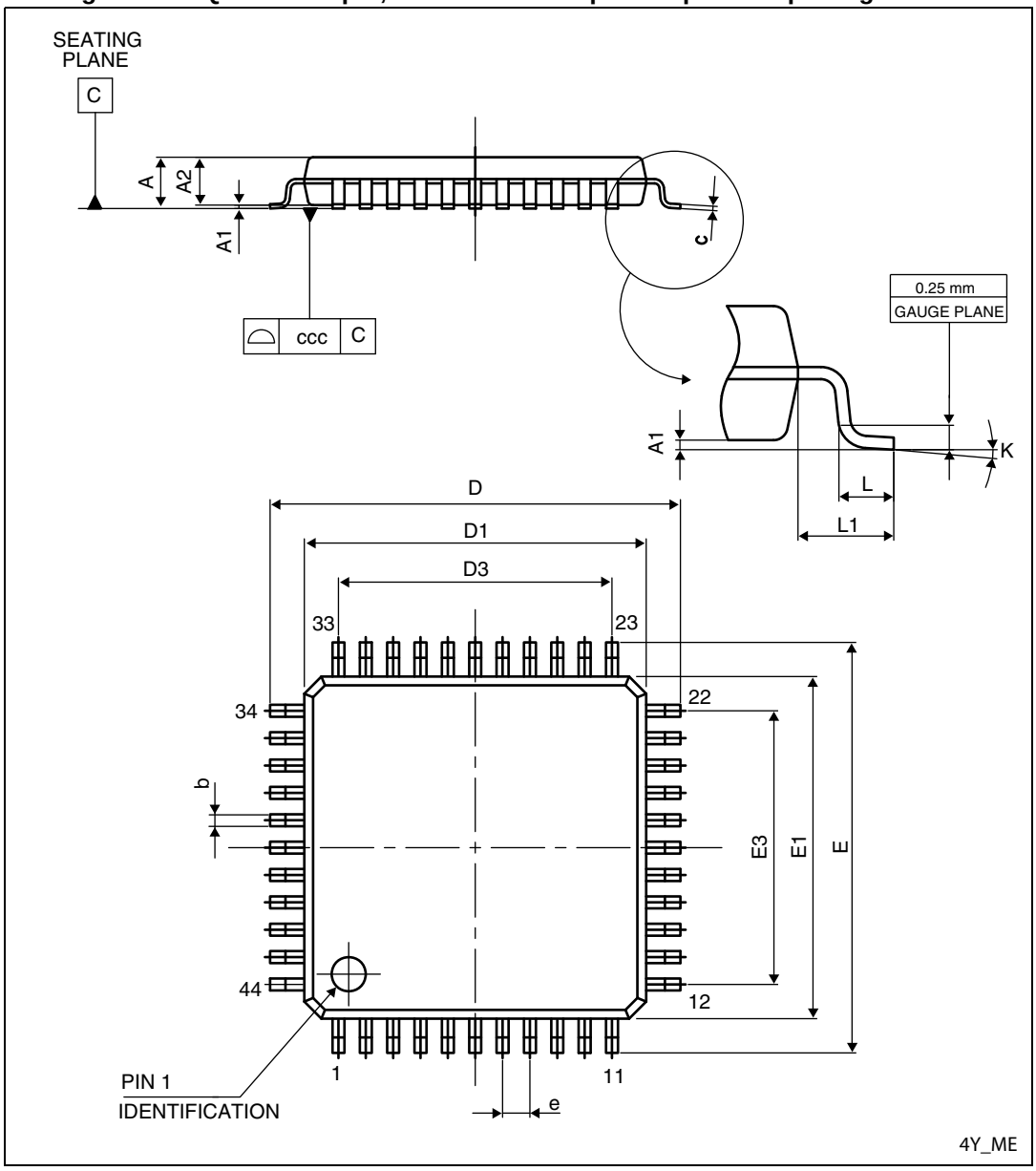


Table 58. Document revision history (continued)

Date	Revision	Changes
10-Jul-2009	8 cont'd	*Section 10: Electrical characteristics*: Added data for TBD values; updated *Table 15: Voltage characteristics* and *Table 18: General operating conditions*; updated VCAP specifications in *Table 18* and in *Section 10.3.1: VCAP external capacitor*; updated *Figure 18*; replaced *Figure 19*; updated *Table 35: RAM and hardware registers*; updated *Figure 22* and *Figure 35*; added *Figure 40: Typical application with I2C bus and timing diagram*. Removed *Table 56: Junction temperature range.* Added link between ordering information *Figure 59* and STM8S20xx features *Table 2*.
13-Apr-2010	9	Document status changed from "preliminary data" to "datasheet". *Table 2: STM8S20xxx performance line features*: high sink I/O for STM8S207C8 is 16 (not 13). *Table 3: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*: updated bit positions for TIM2 and TIM3. *Figure 5: LQFP 48-pin pinout*: added CAN_TX and CAN_RX to pins 35 and 36; noted that these pins are available only in STM8S208xx devices. *Figure 7: LQFP 32-pin pinout*: replaced uart2 with uart3. *Table 6: Pin description*: added footnotes concerning beCAN availability and UART1_RX and UART3_RX pins. *Table 13: Option byte description*: added description of STM8L bootloader option bytes to the option byte description table. Added *Section 9: Unique ID* (and listed this attribute in *Features*). *Section 10.3: Operating conditions*: added introductory text. *Table 18: General operating conditions*: replaced "C_{EXT}" with "VCAP" and added data for ESR and ESL; removed "low power dissipation" condition for T_A. *Table 26: Total current consumption in halt mode at VDD = 5 V*: replaced max value of $I_{DD(H)}$ at 85 °C from 30 µA to 35 µA for the condition "Flash in power-down mode, HSI clock after wakeup". *Table 33: HSI oscillator characteristics*: updated the ACC_{HSI} factory calibrated values. *Functional EMS (electromagnetic susceptibility)* and *Table 47*: replaced "IEC 1000" with "IEC 61000". *Electromagnetic interference (EMI)* and *Table 48*: replaced "SAE J1752/3" with "IEC 61967-2". *Table 57: Thermal characteristics*: changed the thermal resistance junction-ambient value of LQFP32 (7x7 mm) from 59 °C/W to 60 °C/W.