What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s207s6t6ctr

Contents

1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

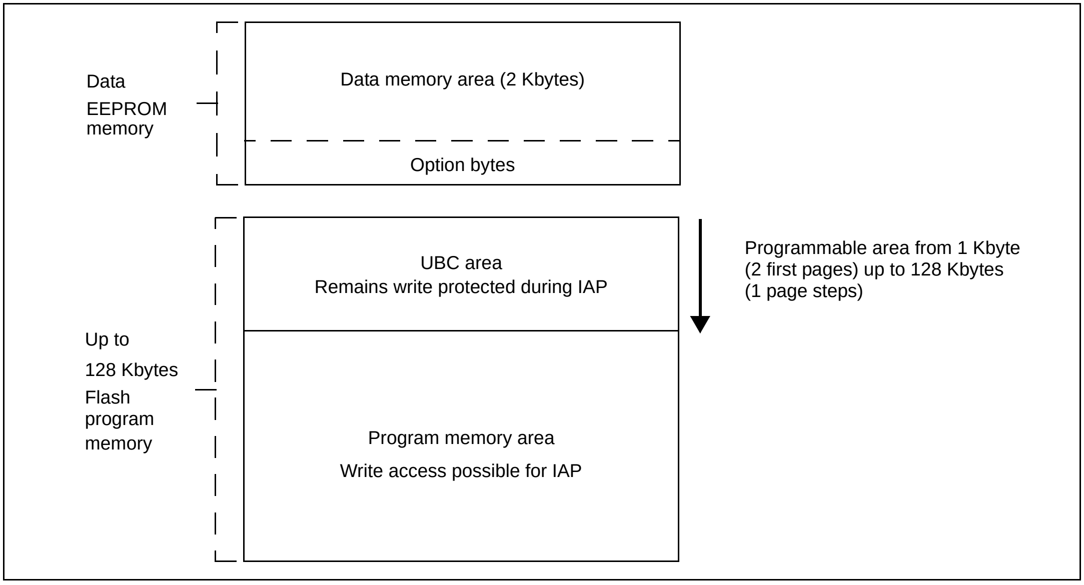
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

Table 7 lists the boundary addresses for each memory size. The top of the stack is at the RAM end address in each case.

Table 7. Flash, Data EEPROM and RAM boundary addresses

Memory area	Size (bytes)	Start address	End address
Flash program memory	128 K	0x00 8000	0x02 7FFF
	64 K	0x00 8000	0x01 7FFF
	32 K	0x00 8000	0x00 FFFF
RAM	6 K	**0x00 0000**	0x00 17FF
	4 K	**0x00 0000**	0x00 1000
	2 K	**0x00 0000**	0x00 07FF
Data EEPROM	2048	0x00 4000	**0x00 47FF**
	1536	0x00 4000	**0x00 45FF**
	1024	0x00 4000	**0x00 43FF**

6.2 Register map

Table 8. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0x00
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0x00
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0x00
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX[2]
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I^2C	I2C_CR1	I^2C control register 1	0x00
0x00 5211		I2C_CR2	I^2C control register 2	0x00
0x00 5212		I2C_FREQR	I^2C frequency register	0x00
0x00 5213		I2C_OARL	I^2C own address register low	0x00
0x00 5214		I2C_OARH	I^2C own address register high	0x00
0x00 5215		Reserved		

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5216	I^2C	I2C_DR	I^2C data register	0x00
0x00 5217		I2C_SR1	I^2C status register 1	0x00
0x00 5218		I2C_SR2	I^2C status register 2	0x00
0x00 5219		I2C_SR3	I^2C status register 3	0x00
0x00 521A		I2C_ITR	I^2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I^2C clock control register low	0x00
0x00 521C		I2C_CCRH	I^2C clock control register high	0x00
0x00 521D		I2C_TRISER	I^2C TRISE register	0x02
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F	Reserved area (5 bytes)			
0x00 5240	UART3	UART3_SR	UART3 status register	C0h
0x00 5241		UART3_DR	UART3 data register	0xXX
0x00 5242		UART3_BRR1	UART3 baud rate register 1	0x00
0x00 5243		UART3_BRR2	UART3 baud rate register 2	0x00
0x00 5244		UART3_CR1	UART3 control register 1	0x00
0x00 5245		UART3_CR2	UART3 control register 2	0x00
0x00 5246		UART3_CR3	UART3 control register 3	0x00
0x00 5247		UART3_CR4	UART3 control register 4	0x00
0x00 5248		Reserved		
0x00 5249		UART3_CR6	UART3 control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5428	beCAN	CAN_P0	CAN paged register 0	0xXX[3]
0x00 5429		CAN_P1	CAN paged register 1	0xXX[3]
0x00 542A		CAN_P2	CAN paged register 2	0xXX[3]
0x00 542B		CAN_P3	CAN paged register 3	0xXX[3]
0x00 542C		CAN_P4	CAN paged register 4	0xXX[3]
0x00 542D		CAN_P5	CAN paged register 5	0xXX[3]
0x00 542E		CAN_P6	CAN paged register 6	0xXX[3]
0x00 542F		CAN_P7	CAN paged register 7	0xXX[3]
0x00 5430		CAN_P8	CAN paged register 8	0xXX[3]
0x00 5431		CAN_P9	CAN paged register 9	0xXX[3]
0x00 5432		CAN_PA	CAN paged register A	0xXX[3]
0x00 5433		CAN_PB	CAN paged register B	0xXX[3]
0x00 5434		CAN_PC	CAN paged register C	0xXX[3]
0x00 5435		CAN_PD	CAN paged register D	0xXX[3]
0x00 5436		CAN_PE	CAN paged register E	0xXX[3]
0x00 5437		CAN_PF	CAN paged register F	0xXX[3]
0x00 5438 to 0x00 57FF	Reserved area (968 bytes)			

1. Depends on the previous reset source.
2. Write only register.
3. If the bootloader is enabled, it is initialized to 0x00.

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU[(1)]	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17[(2)]
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register Label	Register Name	Reset Status
0x00 7F98	DM	DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only
2. Product dependent value, see *Figure 8: Memory map*.

Table 13. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 0x00: no UBC, no write-protection 0x01: Pages 0 to 1 defined as UBC, memory write-protected 0x02: Pages 0 to 3 defined as UBC, memory write-protected 0x03: Pages 0 to 4 defined as UBC, memory write-protected ... 0xFE: Pages 0 to 255 defined as UBC, memory write-protected 0xFF: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^{2}C_SDA, port B4 alternate function = I^{2}C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CH4 **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

10.2 Absolute maximum ratings

Stresses above those listed as ‘absolute maximum ratings’ may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including $V_{DDA\ and}$ V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx}$ - $V_{DD}\rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx}$ - $V_{SS}\rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

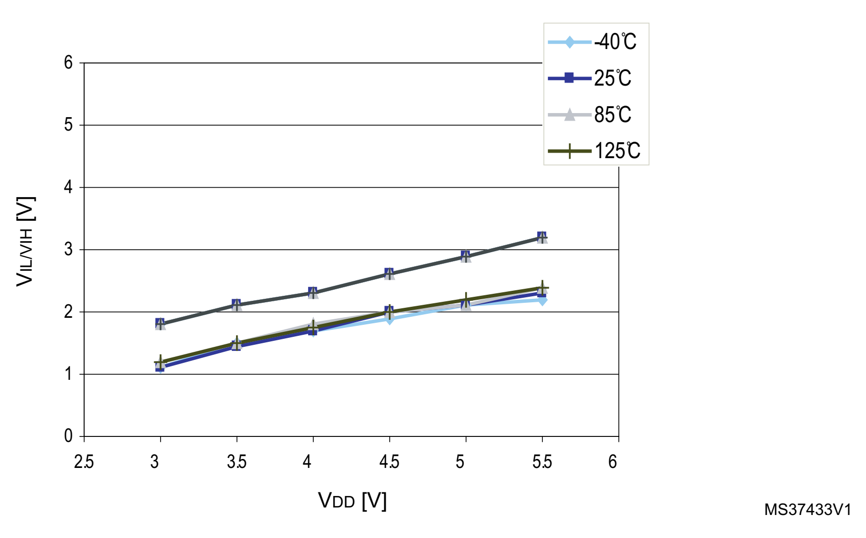


Figure 21. Typical pull-up resistance vs V_{DD} @ 4 temperatures

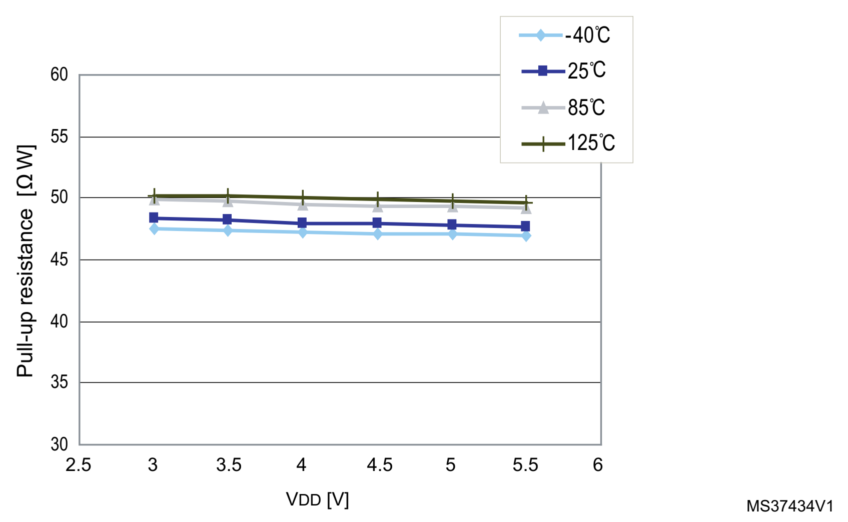


Figure 37. SPI timing diagram - slave mode and CPHA = 0

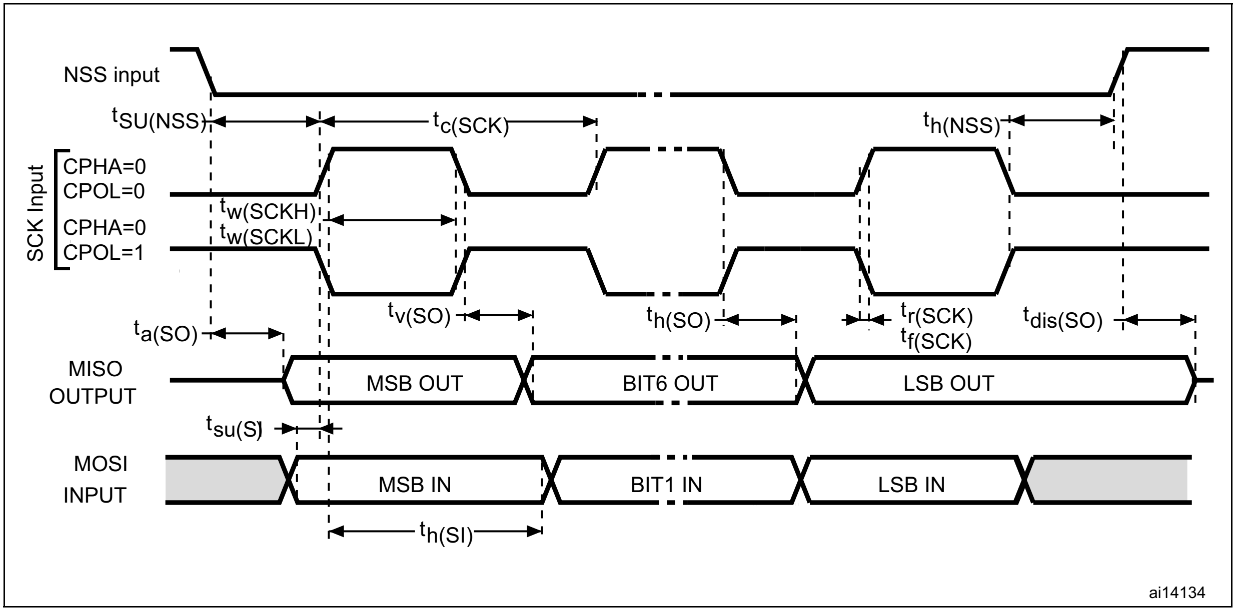
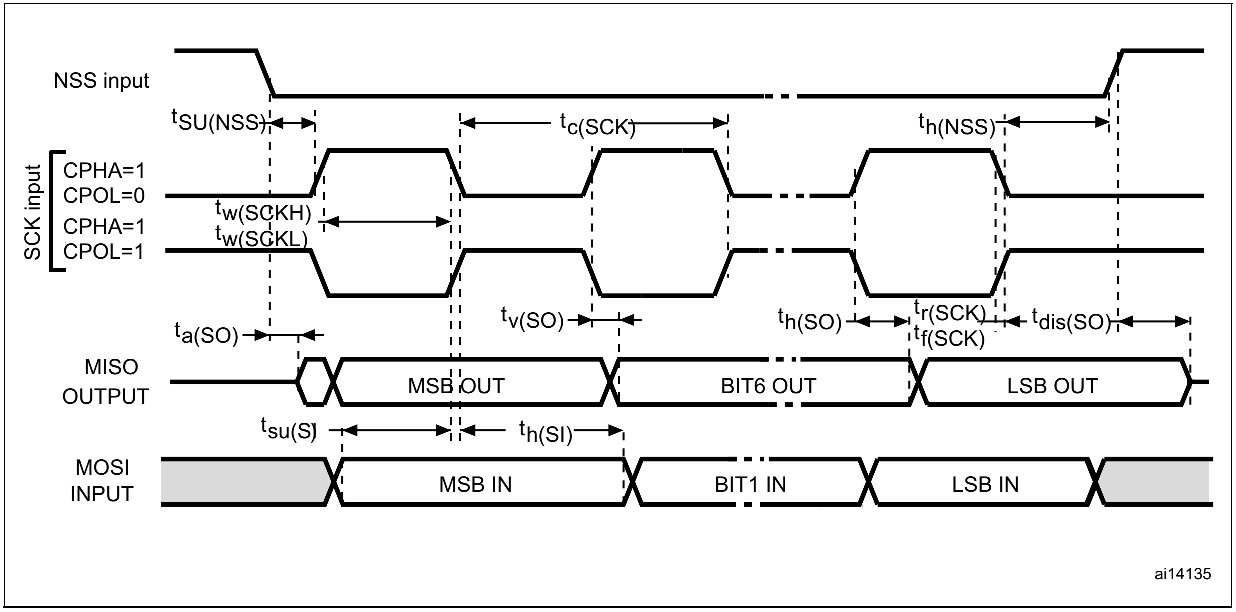


Figure 38. SPI timing diagram - slave mode and CPHA = 1[1]



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.9 I^2C interface characteristics

Table 43. I^2C characteristics

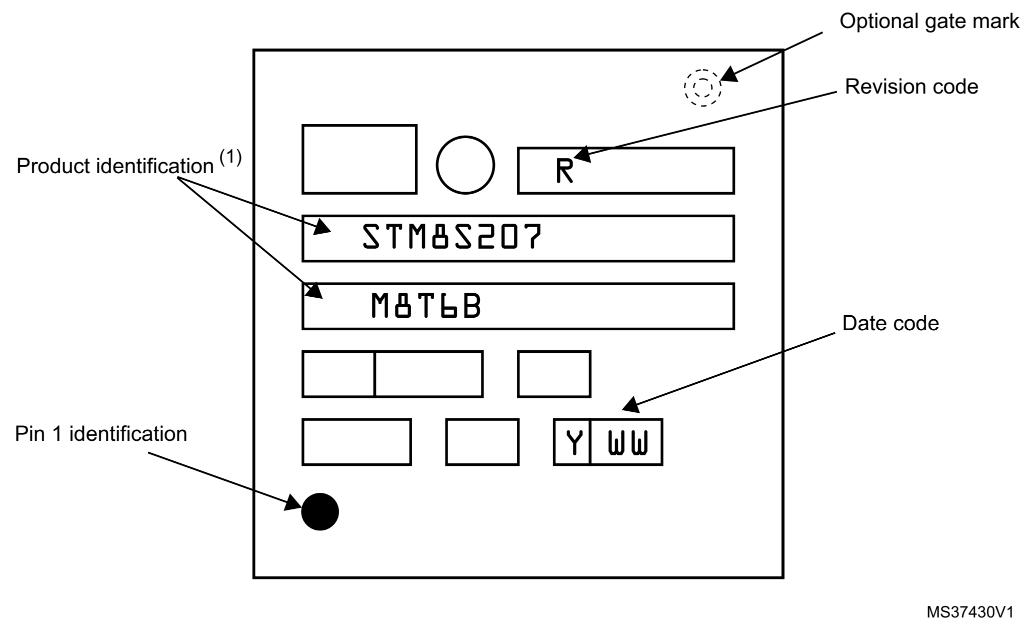
Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I^2C speed (400kHz)
2. Data based on standard I^2C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

Device marking

The following figure shows the marking for the LQFP80 package.

Figure 45. LQFP80 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

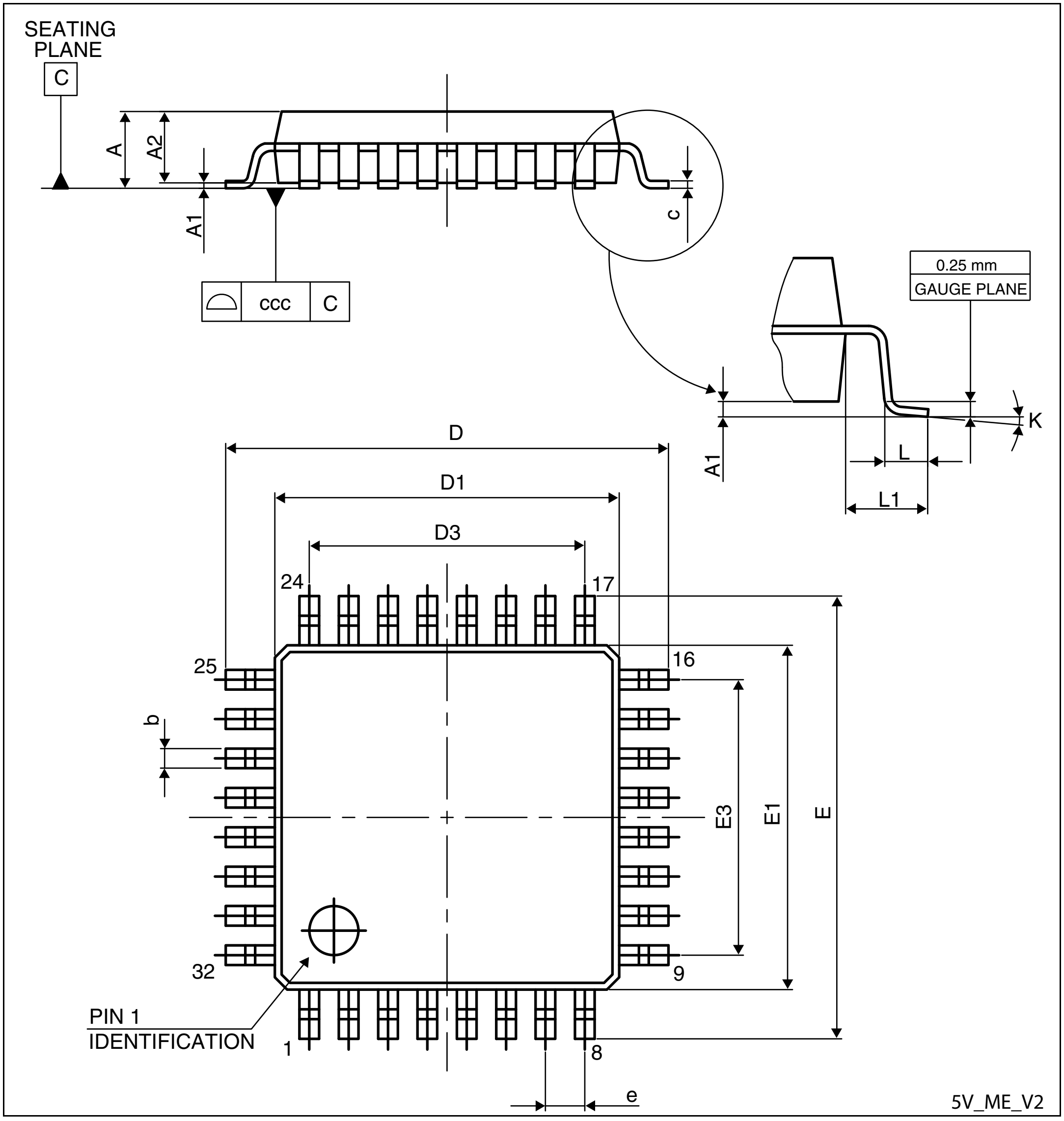
Table 55. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	8.000	-	-	0.3150	-
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	8.000	-	-	0.3150	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal places.

11.1.5 LQFP32 package information

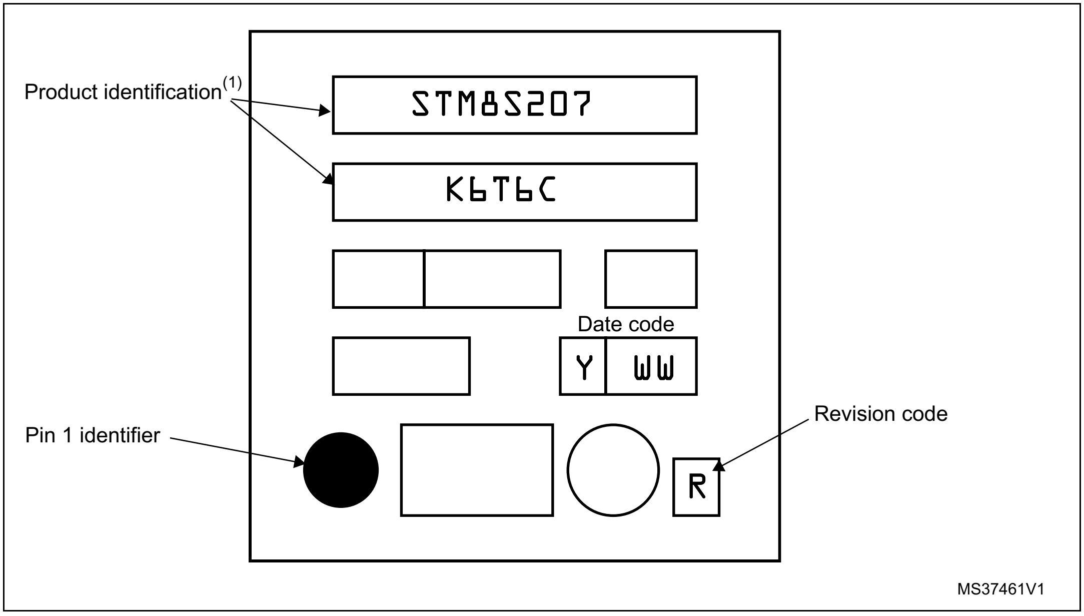
Figure 56. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



Device marking

The following figure shows the marking for the LQFP32 package.

Figure 58. LQFP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 18: General operating conditions on page 56*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where: $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$, and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 57. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 14 x 14 mm	45	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm	54	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet the development requirements and to adapt the emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet the development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.