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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s208c8t6

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on six vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- Up to 128 Kbytes of high density Flash program single voltage Flash memory
- Up to 2K bytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory.
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 2*.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

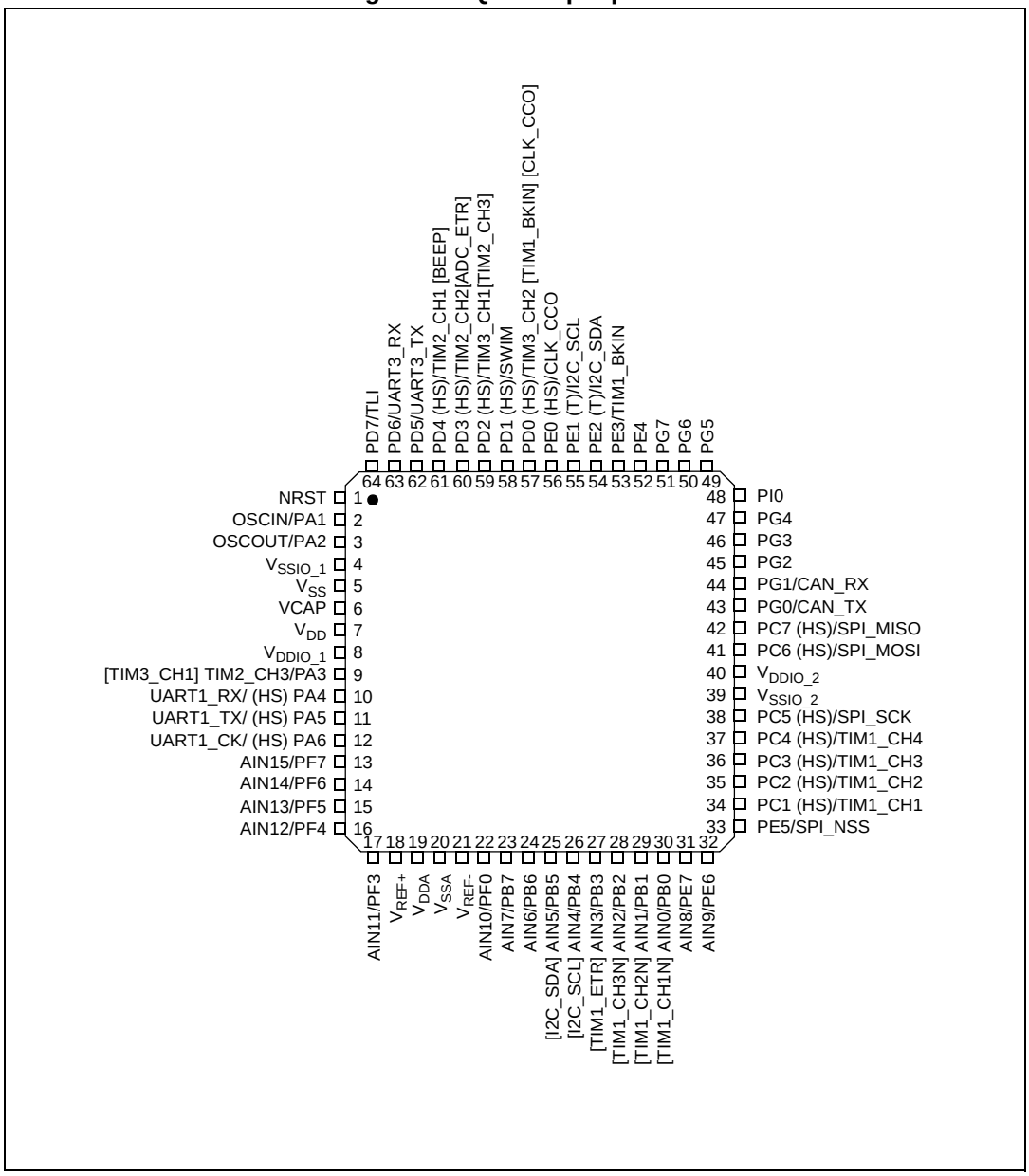
This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 5. Legend/abbreviations for pinout table

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull
Reset state	Bold **X** (pin state after internal reset release) Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Table 6. Pin description

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	1	1	NRST	I/O		**X**						Reset		
2	2	2	2	2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	3	3	3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	4	4	4	-	V_{SSIO_1}	S								I/O ground		
5	5	5	5	4	V_{SS}	S								Digital ground		
6	6	6	6	5	VCAP	S								1.8 V regulator capacitor		
7	7	7	7	6	V_{DD}	S								Digital power supply		
8	8	8	8	7	V_{DDIO_1}	S								I/O power supply		
9	9	9	-	-	PA3/TIM2_CH3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CH1 [AFR1]
10	10	10	9	-	PA4/UART1_RX (1)	I/O	**X**	X	X	HS	O3	X	X	**Port A4**	UART1 receive	
11	11	11	10	-	PA5/UART1_TX	I/O	**X**	X	X	HS	O3	X	X	**Port A5**	UART1 transmit	

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
31	27	19	18	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
32	28	20	19	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input 2	TIM1_ CH3N [AFR5]
33	29	21	20	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]
34	30	22	21	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ CH1N [AFR5]
35	-	-	-	-	PH4/TIM1_ETR	I/O	**X**	X			O1	X	X	**Port H4**	Timer 1 - trigger input	
36	-	-	-	-	PH5/ TIM1_CH3N	I/O	**X**	X			O1	X	X	**Port H5**	Timer 1 - inverted channel 3	
37	-	-	-	-	PH6/ TIM1_CH2N	I/O	**X**	X			O1	X	X	**Port H6**	Timer 1 - inverted channel 2	
38	-	-	-	-	PH7/ TIM1_CH1N	I/O	**X**	X			O1	X	X	**Port H7**	Timer 1 - inverted channel 2	
39	31	23	-	-	PE7/AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	
40	32	24	22	-	PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E6**	Analog input 9	
41	33	25	23	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
42	-	-	-	-	PC0/ADC_ETR	I/O	**X**	X	X		O1	X	X	**Port C0**	ADC trigger input	
43	34	26	24	18	PC1/TIM1_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
44	35	27	25	19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
45	36	28	26	20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
69	55	39	35	-	PE1/I^{2}C_SCL	I/O	**X**		X		O1	T(3)		**Port E1**	I^{2}C clock	
70	56	40	36	-	PE0/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port E0**	Configurable clock output	
71	-	-	-	-	PI6	I/O	**X**	X			O1	X	X	**Port I6**		
72	-	-	-	-	PI7	I/O	**X**	X			O1	X	X	**Port I7**		
73	57	41	37	25	PD0/TIM3_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
74	58	42	38	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
75	59	43	39	27	PD2/TIM3_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
76	60	44	40	28	PD3/TIM2_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
77	61	45	41	29	PD4/TIM2_CH1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
78	62	46	42	30	PD5/ UART3_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART3 data transmit	
79	63	47	43	31	PD6/ UART3_RX(1)	I/O	**X**	X	X		O1	X	X	**Port D6**	UART3 data receive	
80	64	48	44	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CH4 [AFR4](5)

1. The default state of UART1_RX and UART3_RX pins is controlled by the ROM bootloader. These pins are pulled up as part of the bootloader activation process and returned to the floating state before a return from the bootloader.
2. The beCAN interface is available on STM8S208xx devices only
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.
5. Available in 44-pin package only. On other packages, the AFR4 bit is reserved and must be kept at 0.

5.2 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function

remap) option bits. Refer to *Section 8: Option bytes on page 47*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

Table 13. Option byte description (continued)

Option byte no.	Description
OPTBL	**BL[7:0]** *Bootloader option byte* For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details. For STM8L products, the bootloader option bytes are on addresses 0xXXXX and 0xXXXX+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

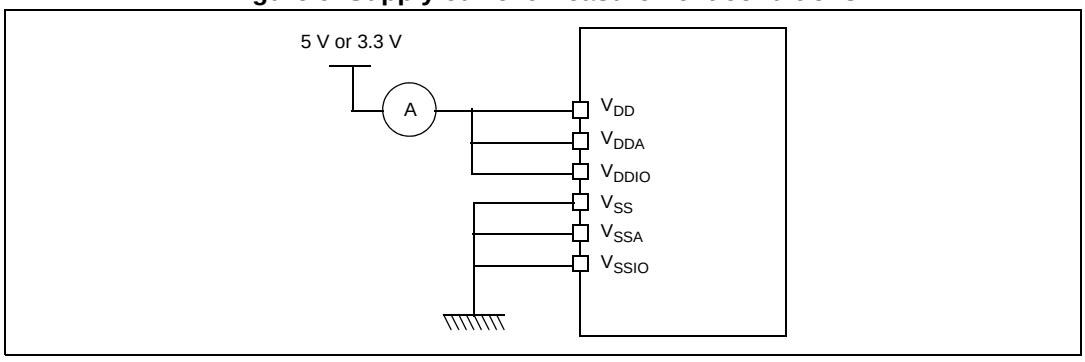
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Typical current consumption

For typical current consumption measurements, V_{DD}, V_{DDIO} and V_{DDA} are connected together in the configuration shown in *Figure 9*.

Figure 9. Supply current measurement conditions

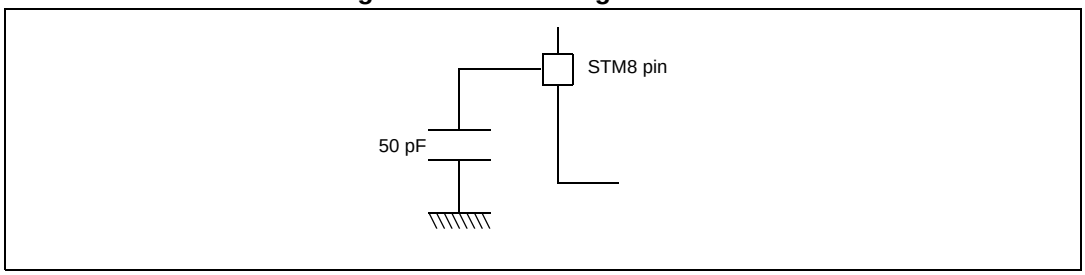


10.1.5 Pin loading conditions

10.1.6 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

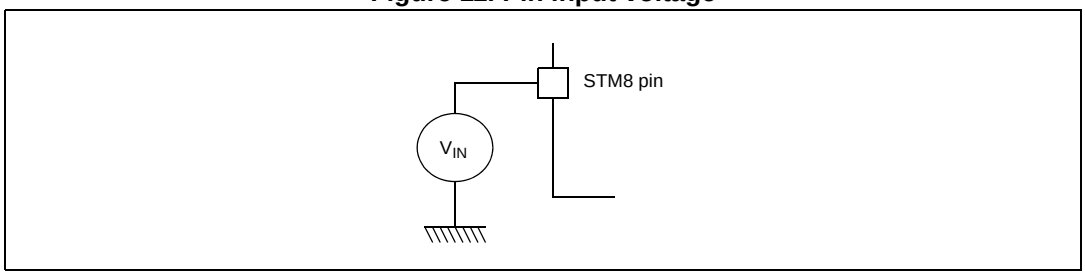
Figure 10. Pin loading conditions



10.1.7 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage



10.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 18*. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	$T_A \leq$ 105 °C	0	24	MHz
			0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor		470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85° C for suffix 6 or T_A = 125° C for suffix 3	44, 48, 64, and 80-pin devices, with output on 8 standard ports, 2 high sink ports and 2 open drain ports simultaneously(4)		443	mW
		32-pin package, with output on 8 standard ports and 2 high sink ports simultaneously(4)		360	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	
		3 suffix version	-40	130(5)	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 11.2: Thermal characteristics on page 108*) with the value for T_{Jmax} given in *Table 18* above and the value for Θ_{JA} given in *Table 57: Thermal characteristics*.
4. Refer to *Section 11.2: Thermal characteristics on page 108* for the calculation method.
5. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.4		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.0		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 23. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.0		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Low speed internal RC oscillator (LSI)

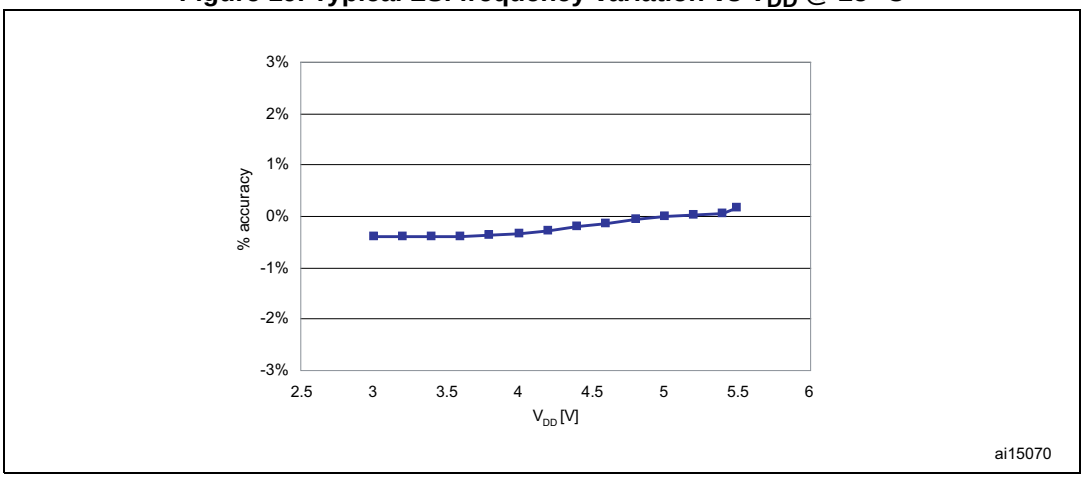
Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		110	128	146	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				7(1)	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			5		µA

1. Guaranteed by design, not tested in production.

Figure 19. Typical LSI frequency variation vs V_{DD} @ 25 °C



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram - slave mode and CPHA = 0

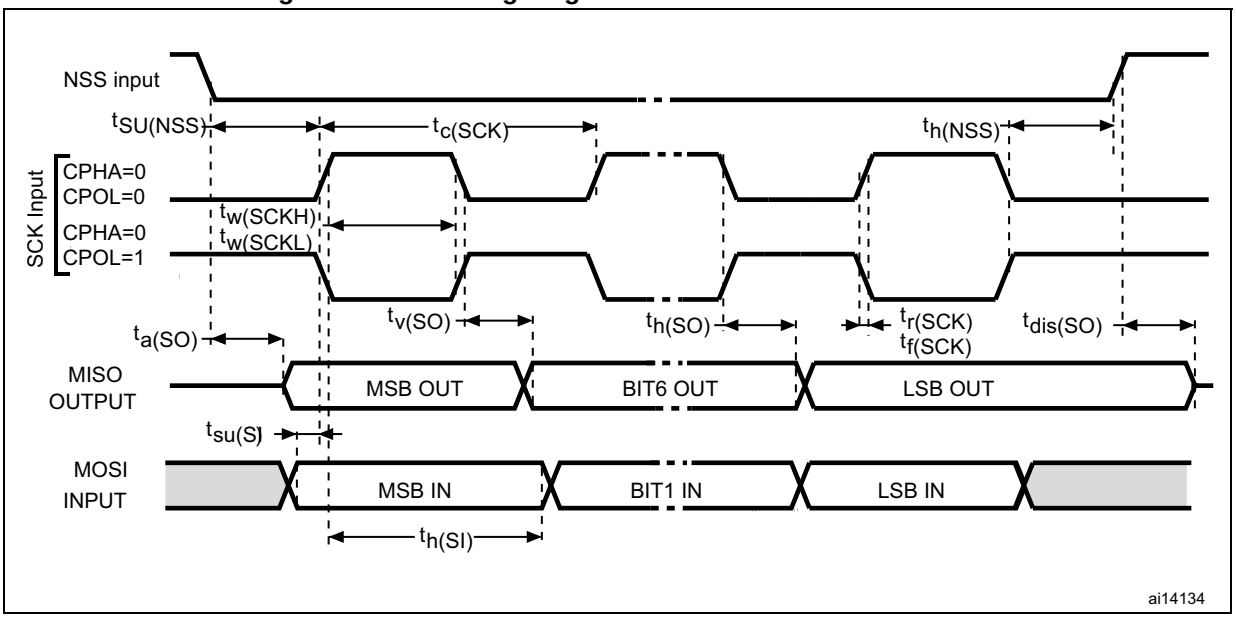
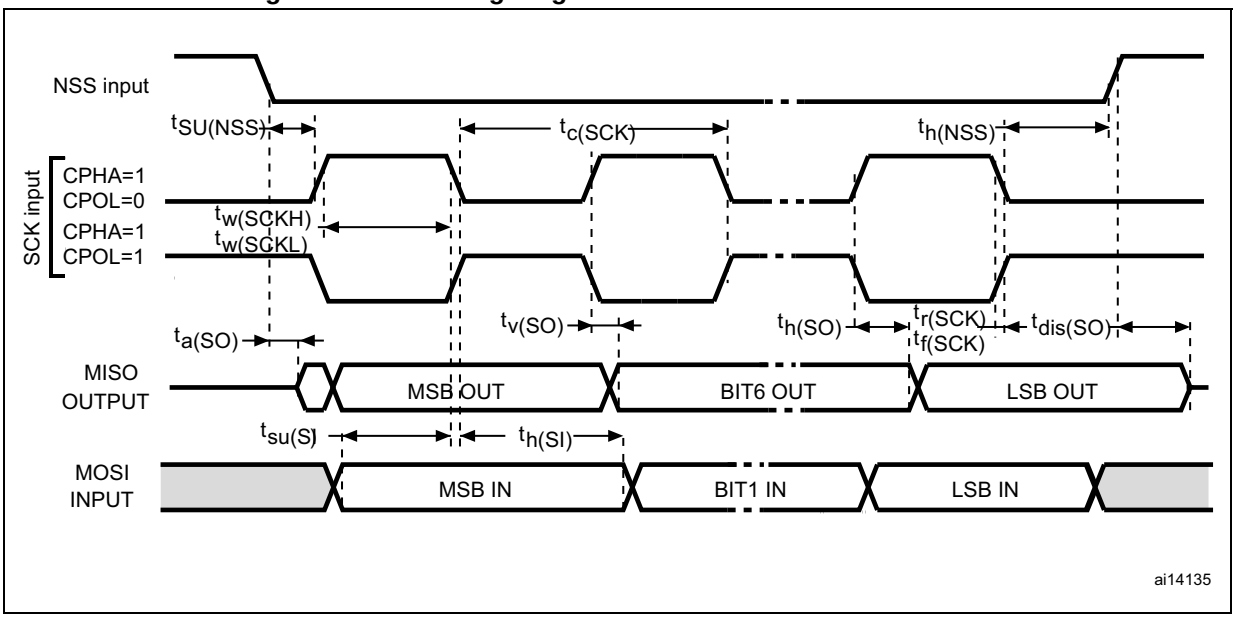
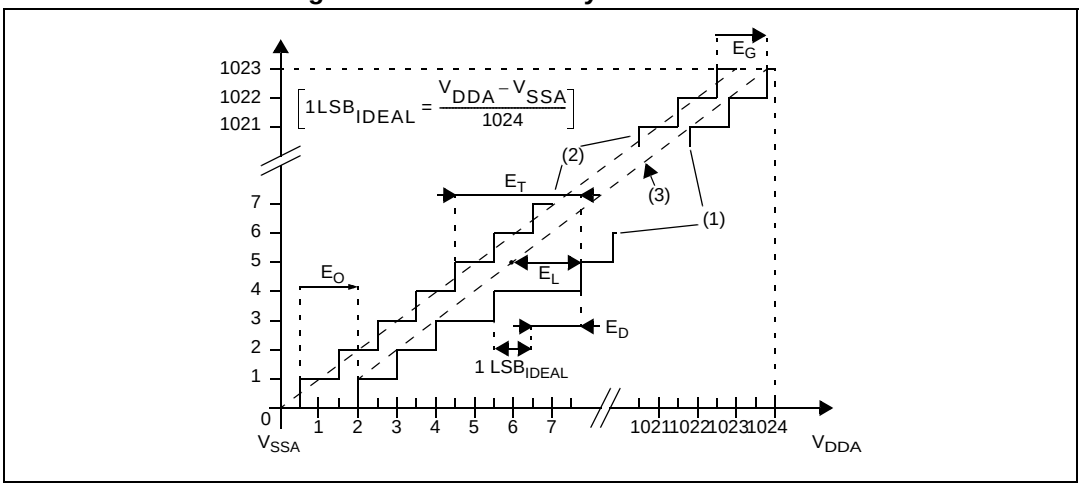


Figure 38. SPI timing diagram - slave mode and CPHA = 1(1)



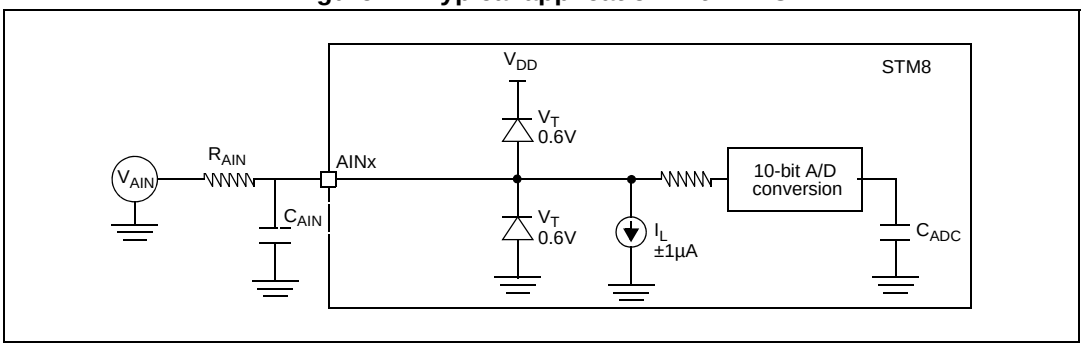
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical application with ADC



10.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 47. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-4	4A

Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

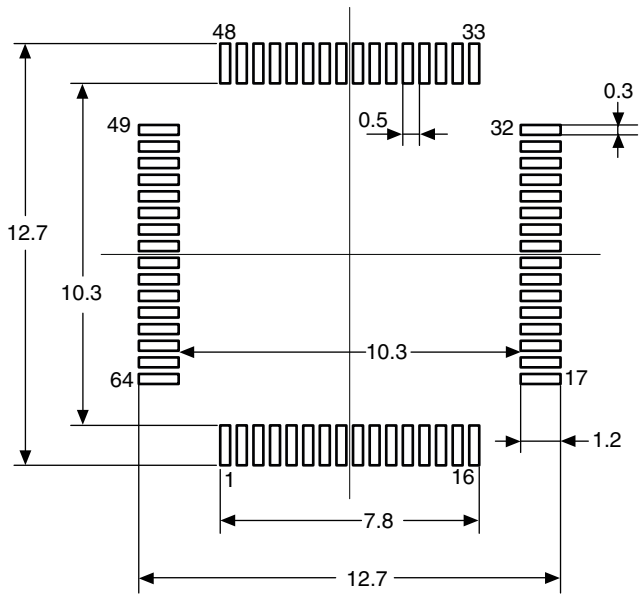
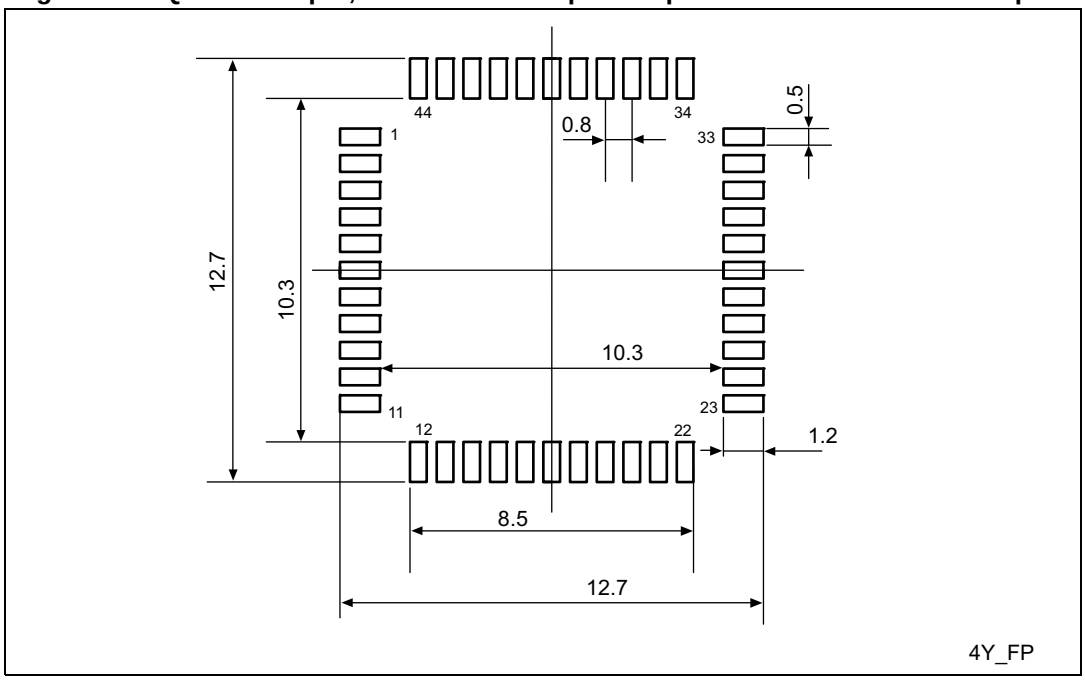


Figure 54. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat recommended footprint

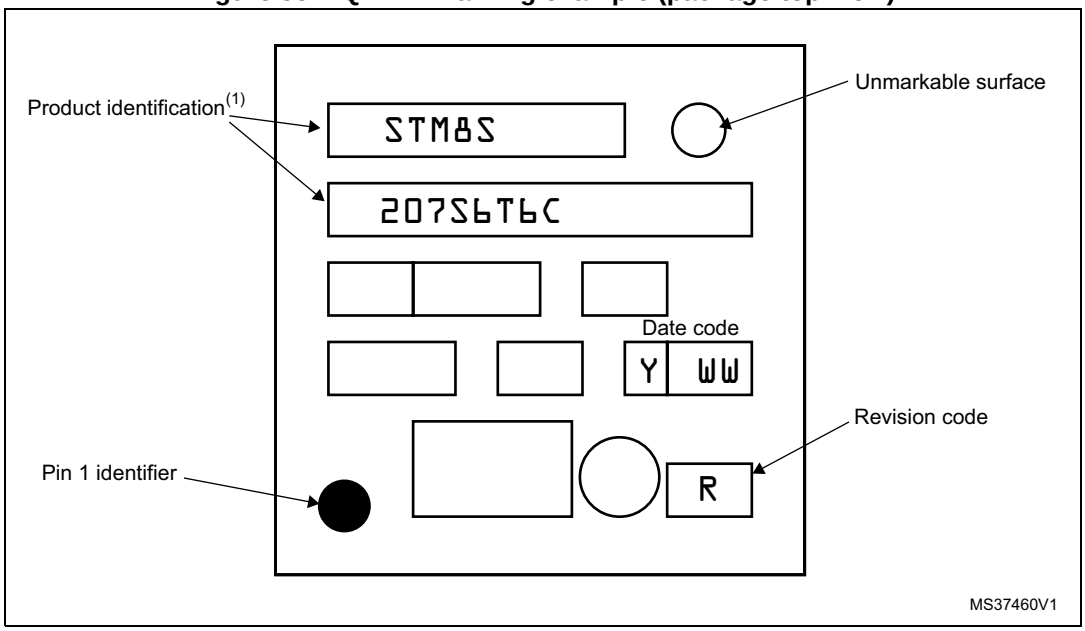


1. Dimensions are expressed in millimeters.

Device marking

The following figure shows the marking for the LQFP44 package.

Figure 55. LQFP44 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

14 Revision history

Table 58. Document revision history

Date	Revision	Changes
23-May-2008	1	Initial release.
05-Jun-2008	2	Added part numbers on page 1 and in *Table 2 on page 11*. Updated *Section 4: Product overview*. Updated *Section 10: Electrical characteristics*.
22-Jun-2008	3	Added part numbers on page 1 and in *Table 2 on page 11*.
12-Aug-2008	4	Added 32 pin device pinout and ordering information. Updated UBC option description in *Table 13 on page 48*. USART renamed UART1, LINUART renamed UART3. Max. ADC frequency increased to 6 MHz.
20-Oct-2008	5	Removed STM8S207K4 part number. Removed LQFP64 14 x 14 mm package. Added medium and high density Flash memory categories. Added *Section 6: Memory and register map on page 34*. Replaced beCAN3 by beCAN in *Section 4.14.5: beCAN*. Updated *Section 10: Electrical characteristics on page 52*. Updated LQFP44 (*Figure 53* and *Table 55*), and LQFP32 outline and mechanical data (*Figure 56*, and *Table 56*).
08-Dec-2008	6	Changed V_{DD} minimum value from 3.0 to 2.95 V. Updated number of High Sink I/Os in pinout. Removed FLASH _NFPR and FLASH _FPR registers in *Table 9: General hardware register map*.
30-Jan-2009	7	Removed preliminary status. Removed VQFN32 package. Added STM8S207C6, STM8S207S6. Updated external interrupts in *Table 2 on page 11*. Updated *Section 10: Electrical characteristics*.
10-Jul-2009	8	Document status changed from “preliminary data” to “datasheet”. Added LQFP64 14 x 14 mm package. Added STM8S207M8, STM8S207SB, STM8S208R8, STM8S208R6, STM8S208C8, and STM8S208C6, STM8S208SB, STM8S208S8, and STM8S208S6. Replaced “CAN” with “beCAN”. Added *Table 3* to *Section 4.5: Clock controller*. Updated *Section 4.8: Auto wakeup counter*. Added beCAN peripheral (impacting *Table 1* and *Figure 6*). Added footnote about CAN_RX/TX to pinout figures *5*, *4*, and *6*. *Table 6*: Removed ‘X’ from wpu column of I^2C pins (no wpu available). Added *Table 11: Interrupt mapping*.