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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s208c8t6tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Asynchronous communication (UART mode)

- Full duplex communication NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
 - Two receiver wakeup modes:
 - Address bit (MSB)
 - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

LIN slave mode

- Autonomous header handling one single interrupt per valid message header
- Automatic baud rate synchronization maximum tolerated initial clock deviation ±15%
- Sync delimiter checking
- 11-bit LIN sync break detection break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin



4.14.4 I²C

- I²C master features:
 - Clock generation
 - Start and stop generation
 - I²C slave features:
 - Programmable I²C address detection
 - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
 - Supports different communication speeds:
 - Standard speed (up to 100 kHz)
 - Fast speed (up to 400 kHz)

4.14.5 beCAN

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the beCAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

Reception

- 8-, 11- and 29-bit ID
- One receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- Six filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
 - Mask mode permitting ID range filtering
 - ID list mode
- Time triggered communication option
 - Disable automatic retransmission mode
 - 16-bit free running timer
 - Configurable timer resolution
 - Time stamp sent in last two data bytes



remap) option bits. Refer to Section 8: Option bytes on page 47. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).



Address	Block	Register label	Register name	Reset status
0x00 5216		I2C_DR	l ² C data register	0x00
0x00 5217		I2C_SR1	I ² C status register 1	0x00
0x00 5218	-	I2C_SR2	l ² C status register 2	0x00
0x00 5219	I ² C	I2C_SR3	l ² C status register 3	0x00
0x00 521A	- FC	I2C_ITR	I ² C interrupt control register	0x00
0x00 521B		I2C_CCRL	I ² C clock control register low	0x00
0x00 521C		I2C_CCRH	I ² C clock control register high	0x00
0x00 521D		I2C_TRISER	I ² C TRISE register	0x02
0x00 521E to 0x00 522F			Reserved area (18 bytes)	-
0x00 5230		UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235	UART1	UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00 523F			Reserved area (5 bytes)	
0x00 5240		UART3_SR	UART3 status register	C0h
0x00 5241		UART3_DR	UART3 data register	0xXX
0x00 5242		UART3_BRR1	UART3 baud rate register 1	0x00
0x00 5243		UART3_BRR2	UART3 baud rate register 2	0x00
0x00 5244		UART3_CR1	UART3 control register 1	0x00
0x00 5245	UARIS	UART3_CR2	UART3 control register 2	0x00
0x00 5246		UART3_CR3	UART3 control register 3	0x00
0x00 5247		UART3_CR4	UART3 control register 4	0x00
0x00 5248]		Reserved	
0x00 5249]	UART3_CR6	UART3 control register 6	0x00
0x00 524A to 0x00 524F	Reserved area (6 bytes)			

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Table 9.	General	nardware	register	map ((continuea))



Address	Block	Register Label	Register Name	Reset Status		
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10		
0x00 7F99 DM		DM_CSR2	DM debug module control/status register 2	0x00		
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF		
0x00 7F9B to 0x00 7F9F		Reserved area (5 bytes)				

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

1. Accessible by debug module only

2. Product dependent value, see Figure 8: Memory map.



9 Unique ID

The devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Address	Content	ntent Unique ID bits							
Address	description	7	6	5	4	3	2	1	0
0x48CD	X co-ordinate on the				U_	_ID[7:0]			
0x48CE	wafer				U_	ID[15:8]			
0x48CF	Y co-ordinate on the	U_ID[23:16]							
0x48D0	wafer				U_I	D[31:24]			
0x48D1	Wafer number	U_ID[39:32]							
0x48D2		U_ID[47:40]							
0x48D3					U_I	D[55:48]			
0x48D4					U_I	D[63:56]			
0x48D5	Lot number	U_ID[71:64]							
0x48D6					U_I	D[79:72]			
0x48D7		U_ID[87:80]							
0x48D8		U_ID[95:88]							

Table 14. Unique ID registers (96 bits)



10.1.5 Pin loading conditions

10.1.6 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 10.

Figure 10. Pin loading conditions



10.1.7 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 11. Pin input voltage





10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit
V _{DDx} - V _{SS}	Supply voltage (including $V_{DDA and} V_{DDIO}$) ⁽¹⁾	-0.3	6.5	
V	Input voltage on true open drain pins (PE1, PE2) ⁽²⁾	V _{SS} - 0.3	6.5	V
⊻ IN	Input voltage on any other pin ⁽²⁾	V _{SS} - 0.3	V _{DD} + 0.3	
V _{DDx} - V _{DD}	Variations between different power pins		50	m\/
V _{SSx} - V _{SS}	- V _{SS} Variations between all the different ground pins		50	IIIV
V _{ESD}	Electrostatic discharge voltage see Absolute maximum ratings (electrical sensitivity) on page 89			

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply

2. I_{INJ(PIN)} must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the I_{INJ(PIN)} value. A positive injection is induced by V_{IN}>V_{DD} while a negative injection is induced by V_{IN}<V_{SS}. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected



10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 52*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at $V_{DD} \, \text{or} \, V_{SS}$ (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \le 105$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A .

Symbol	Parameter	Conditions			Max	Unit
		f _{CPU} = f _{MASTER} = 24 MHz,	HSE crystal osc. (24 MHz)	4.4		
		$T_A \leq 105 \ ^{\circ}C$	HSE user ext. clock (24 MHz)	3.7	7.3 ⁽¹⁾	
			HSE crystal osc. (16 MHz)	3.3		
	Supply current in	f _{CPU} = f _{MASTER} = 16 MHz	HSE user ext. clock (16 MHz)	2.7	5.8	
	run mode,		HSI RC osc. (16 MHz)	2.5	3.4	
	code executed	f _ f /129 _ 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1 ⁽¹⁾	
	from RAM	$T_{CPU} = T_{MASTER}/128 = 125 \text{ KHz}$	HSI RC osc. (16 MHz)	1.0	1.3 ⁽¹⁾	
		f _{CPU} = f _{MASTER} /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.55		
1		f _{CPU} = f _{MASTER} = 128 kHz	LSI RC osc. (128 kHz)	0.45		m۸
'DD(RUN)	Supply	f _{CPU} = f _{MASTER} = 24 MHz,	HSE crystal osc. (24 MHz)	11.4		mA
		$T_A \leq 105 \ ^{\circ}C$	HSE user ext. clock (24 MHz)	10.8	18 ⁽¹⁾	
		f _{CPU} = f _{MASTER} = 16 MHz	HSE crystal osc. (16 MHz)	9.0		
			HSE user ext. clock (16 MHz)	8.2	15.2 ⁽¹⁾	
	run mode,		HSI RC osc.(16 MHz)	8.1	13.2 ⁽¹⁾	
	code executed	f _{CPU} = f _{MASTER} = 2 MHz.	HSI RC osc. (16 MHz/8) ⁽²⁾	1.5		
	from Flash	f _{CPU} = f _{MASTER} /128 = 125 kHz	HSI RC osc. (16 MHz)	1.1		
		f _{CPU} = f _{MASTER} /128 = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6		
		f _{CPU} = f _{MASTER} = 128 kHz	LSI RC osc. (128 kHz)	0.55		

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

1. Data based on characterization results, not tested in production.

2. Default clock configuration measured with all peripherals off.



Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
f _{HSE}	External high speed oscillator frequency		1		24	MHz
R _F	Feedback resistor			220		kΩ
C ⁽¹⁾	Recommended load capacitance (2)				20	pF
		C = 20 pF, f _{OSC} = 24 MHz			6 (startup) 2 (stabilized) ⁽³⁾	m۸
IDD(HSE)		C = 10 pF, f _{OSC} = 24 MHz			6 (startup) 1.5 (stabilized) ⁽³⁾	IIIA
9 _m	Oscillator transconductance		5			mA/V
t _{SU(HSE)} ⁽⁴⁾	Startup time	V _{DD} is stabilized		1		ms

Table 32. HS	E oscillator	characteristics
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1. C is approximately equivalent to 2 x crystal Cload.

2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details

3. Data based on characterization results, not tested in production.

 t_{SU(HSE)} is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.



Figure 17. HSE oscillator circuit diagram

HSE oscillator critical g_m formula

 $g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m (2Co + C)^2$

 $\begin{array}{l} {\sf R}_m: \mbox{ Notional resistance (see crystal specification)} \\ {\sf L}_m: \mbox{ Notional inductance (see crystal specification)} \\ {\sf C}_m: \mbox{ Notional capacitance (see crystal specification)} \\ {\sf Co: Shunt capacitance (see crystal specification)} \\ {\sf C}_{L1} = {\sf C}_{L2} = {\sf C}: \mbox{ Grounded external capacitance } \\ {\sf g}_m >> {\sf g}_{mcrit} \end{array}$

DocID14733 Rev 13



10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit	
V _{IL}	Input low level voltage		-0.3		0.3 x V _{DD}	V	
V _{IH}	Input high level voltage	V _{DD} = 5 V	0.7 x V _{DD}		V _{DD} + 0.3 V	v	
V _{hys}	Hysteresis ⁽¹⁾			700		mV	
R _{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ	
		Fast I/Os Load = 50 pF			20 ⁽²⁾		
t _R , t _F Rise and fall time (10% - 90%)	Rise and fall time	Standard and high sink I/Os Load = 50 pF			125 ⁽²⁾		
	(10% - 90%)	Fast I/Os Load = 20 pF			35 ⁽³⁾	ns	
		Standard and high sink I/Os Load = 20 pF			125 ⁽³⁾		
I _{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	μA	
I _{lkg ana}	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±250 ⁽²⁾	nA	
I _{lkg(inj)}	Leakage current in adjacent I/O ⁽²⁾	Injection current ±4 mA			±1 ⁽²⁾	μΑ	

Table 37.	I/O	static	characteristics
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1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

2. Data based on characterization results, not tested in production.

3. Guaranteed by design.



Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Symbol	Parameter	Conditions	Class ⁽¹⁾
		$T_A = 25 \ ^{\circ}C$	А
LU	Static latch-up class	T _A = 85 °C	А
		T _A = 125 °C	А

Table	50.	Electrical	sensitivities
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1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).



11 Package characteristics

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.



Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical
data (continued)

Symbol	mm			inches ⁽¹⁾			
	Min	Тур	Max	Min	Тур	Max	
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °	
CCC			0.100			0.0039	

1. Values in inches are converted from mm and rounded to four decimal places.



Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	mm			inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
А	-	-	1.600	-	-	0.0630		
A1	0.050	-	0.150	0.0020	-	0.0059		
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571		
b	0.170	0.220	0.270	0.0067	0.0087	0.0106		
С	0.090	-	0.200	0.0035	-	0.0079		

Device marking

The following figure shows the marking for the LQFP64 package.



Figure 49. LQFP64 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



11.1.4 LQFP44 package information

Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline







Figure 54. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

Device marking

The following figure shows the marking for the LQFP44 package.



Figure 55. LQFP44 marking example (package top view)

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

DocID14733 Rev 13



13 Ordering information

Figure 59. STM8S207xx/208xx performance line ordering information scheme ⁽¹⁾										
Example:		STM8	S	208	М	В	Т	6	В	TR
Product class STM8 microcontroller										
Family type S = Standard										
Sub-family type ⁽²⁾										
208 = Full peripheral set										
207 = Intermediate peripheral set	t									
Pin count										
K = 32 pins										
S = 44 pins										
C = 48 pins										
R = 64 pins										
M = 80 pins										
Program memory size										
6 = 32 Kbyte										
8 = 64 Kbyte										
B = 128 Kbyte										
Package type										
T = LQFP										
Temperature range 3 = -40 °C to 125 °C 6 = -40 °C to 85 °C										
Package pitch No character = 0.5 mm B = 0.65 mm C = 0.8 mm										
Packing No character = Tray or tube TR = Tape and reel										

 For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to <u>www.st.com</u> or contact the ST Sales Office nearest to you.

2. Refer to Table 2: STM8S20xxx performance line features for detailed description.



14 Revision history

Date Revision		Changes			
23-May-2008	1	Initial release.			
05-Jun-2008	2	Added part numbers on page 1 and in <i>Table 2 on page 11</i> . Updated <i>Section 4: Product overview</i> . Updated <i>Section 10: Electrical characteristics</i> .			
22-Jun-2008	3	Added part numbers on page 1 and in Table 2 on page 11.			
12-Aug-2008	4	Added 32 pin device pinout and ordering information. Updated UBC option description in <i>Table 13 on page 48.</i> USART renamed UART1, LINUART renamed UART3. Max. ADC frequency increased to 6 MHz.			
20-Oct-2008	5	Removed STM8S207K4 part number. Removed LQFP64 14 x 14 mm package. Added medium and high density Flash memory categories. Added Section 6: Memory and register map on page 34. Replaced beCAN3 by beCAN in Section 4.14.5: beCAN. Updated Section 10: Electrical characteristics on page 52. Updated LQFP44 (Figure 53 and Table 55), and LQFP32 outline and mechanical data (Figure 56, and Table 56).			
08-Dec-2008	6	Changed V _{DD} minimum value from 3.0 to 2.95 V. Updated number of High Sink I/Os in pinout. Removed FLASH _NFPR and FLASH _FPR registers in <i>Table 9:</i> <i>General hardware register map</i> .			
30-Jan-2009	7	Removed preliminary status. Removed VQFN32 package. Added STM8S207C6, STM8S207S6. Updated external interrupts in <i>Table 2 on page 11</i> . Updated <i>Section 10: Electrical characteristics</i> .			
10-Jul-2009	8	Document status changed from "preliminary data" to "datasheet". Added LQFP64 14 x 14 mm package. Added STM8S207M8, STM8S207SB, STM8S208R8, STM8S208R6, STM8S208C8, and STM8S208C6, STM8S208SB, STM8S208S8, and STM8S208S6. Replaced "CAN" with "beCAN". Added <i>Table 3</i> to <i>Section 4.5: Clock controller</i> . Updated <i>Section 4.8: Auto wakeup counter</i> . Added beCAN peripheral (impacting <i>Table 1</i> and <i>Figure 6</i>). Added footnote about CAN_RX/TX to pinout figures 5, 4, and 6. <i>Table 6</i> : Removed 'X' from wpu column of I ² C pins (no wpu available). Added <i>Table 11: Interrupt mapping</i> .			

Table 58. Document re	evision	history
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DocID14733 Rev 13