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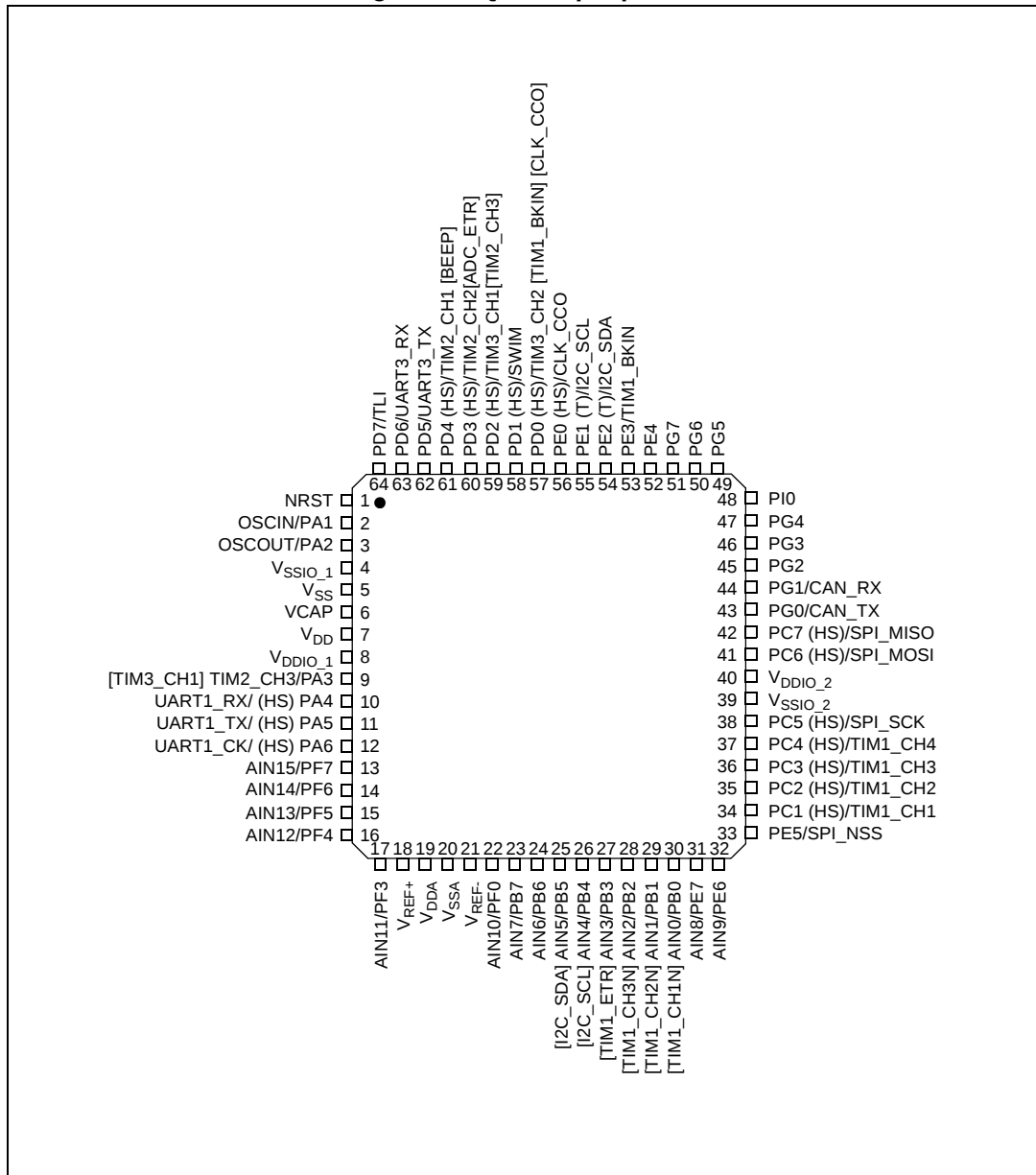
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s208cbt6

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Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	pp			
12	12	12	11	-	PA6/UART1_CK	I/O	X	X	X	HS	O3	X	X	Port A6	UART1 synchronous clock	
13	-	-	-	-	PH0	I/O	X	X		HS	O3	X	X	Port H0		
14	-	-	-	-	PH1	I/O	X	X		HS	O3	X	X	Port H1		
15	-	-	-	-	PH2	I/O	X	X			O1	X	X	Port H2		
16	-	-	-	-	PH3	I/O	X	X			O1	X	X	Port H3		
17	13	-	-	-	PF7/AIN15	I/O	X	X			O1	X	X	Port F7	Analog input 15	
18	14	-	-	-	PF6/AIN14	I/O	X	X			O1	X	X	Port F6	Analog input 14	
19	15	-	-	-	PF5/AIN13	I/O	X	X			O1	X	X	Port F5	Analog input 13	
20	16	-	-	8	PF4/AIN12	I/O	X	X			O1	X	X	Port F4	Analog input 12	
21	17	-	-	-	PF3/AIN11	I/O	X	X			O1	X	X	Port F3	Analog input 11	
22	18	-	-	-	V _{REF+}	S								ADC positive reference voltage		
23	19	13	12	9	V _{DDA}	S								Analog power supply		
24	20	14	13	10	V _{SSA}	S								Analog ground		
25	21	-	-	-	V _{REF-}	S								ADC negative reference voltage		
26	22	-	-	-	PF0/AIN10	I/O	X	X			O1	X	X	Port F0	Analog input 10	
27	23	15	14	-	PB7/AIN7	I/O	X	X	X		O1	X	X	Port B7	Analog input 7	
28	24	16	15	-	PB6/AIN6	I/O	X	X	X		O1	X	X	Port B6	Analog input 6	
29	25	17	16	11	PB5/AIN5	I/O	X	X	X		O1	X	X	Port B5	Analog input 5	I ² C_SDA [AFR6]
30	26	18	17	12	PB4/AIN4	I/O	X	X	X		O1	X	X	Port B4	Analog input 4	I ² C_SCL [AFR6]

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xFF ⁽²⁾
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I ² C	I2C_CR1	I ² C control register 1	0x00
0x00 5211		I2C_CR2	I ² C control register 2	0x00
0x00 5212		I2C_FREQR	I ² C frequency register	0x00
0x00 5213		I2C_OARL	I ² C own address register low	0x00
0x00 5214		I2C_OARH	I ² C own address register high	0x00
0x00 5215		Reserved		

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 Interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00
0x00 525F		TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU ⁽¹⁾	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17 ⁽²⁾
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00

Table 13. Option byte description

Option byte no.	Description
OPT0	ROP[7:0] Memory readout protection (ROP) 0xAA: Enable readout protection (write access via SWIM protocol) <i>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.</i>
OPT1	UBC[7:0] User boot code area 0x00: no UBC, no write-protection 0x01: Pages 0 to 1 defined as UBC, memory write-protected 0x02: Pages 0 to 3 defined as UBC, memory write-protected 0x03: Pages 0 to 4 defined as UBC, memory write-protected ... 0xFE: Pages 0 to 255 defined as UBC, memory write-protected 0xFF: Reserved <i>Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.</i>
OPT2	AFR7 Alternate function remapping option 7 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP AFR6 Alternate function remapping option 6 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I ² C_SDA, port B4 alternate function = I ² C_SCL AFR5 Alternate function remapping option 5 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N AFR4 Alternate function remapping option 4 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CH4 AFR3 Alternate function remapping option 3 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN AFR2 Alternate function remapping option 2 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO <i>Note: AFR2 option has priority over AFR3 if both are activated</i> AFR1 Alternate function remapping option 1 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function = TIM3_CH1 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function = TIM2_CH3 AFR0 Alternate function remapping option 0 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

Figure 12. f_{CPUmax} versus V_{DD}

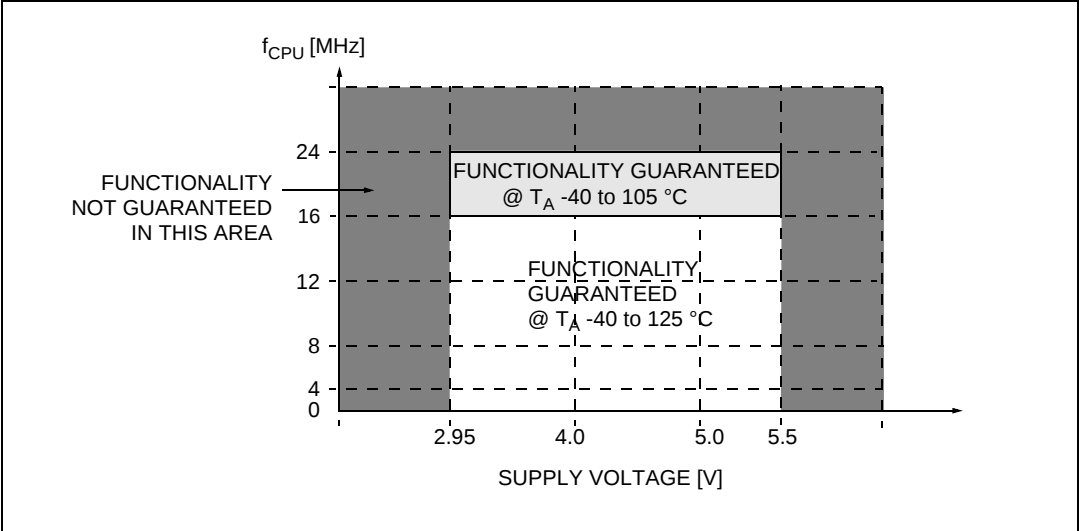


Table 19. Operating conditions at power-up/power-down

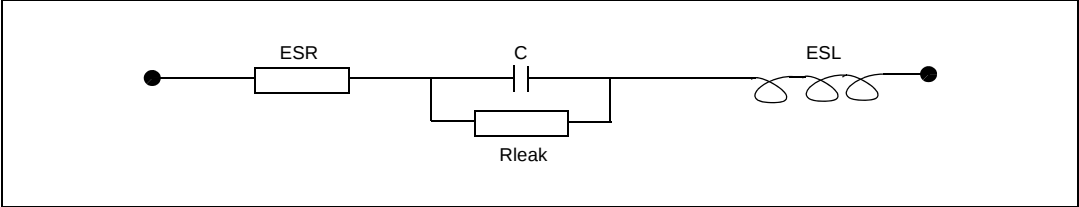
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		2 ⁽¹⁾		∞	$\mu s/V$
	V_{DD} fall time rate		2 ⁽¹⁾		∞	
t_{TEMP}	Reset release delay	V_{DD} rising			1.7 ⁽¹⁾	ms
V_{IT+}	Power-on reset threshold		2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold		2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis			70		mV

1. Guaranteed by design, not tested in production.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in [Table 18](#). Care should be taken to limit the series inductance to less than 15 nH.

Figure 13. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

Current consumption curves

Figure 14 and Figure 15 show typical current consumption measured with code executing in RAM.

Figure 14. Typ. $I_{DD(RUN)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz

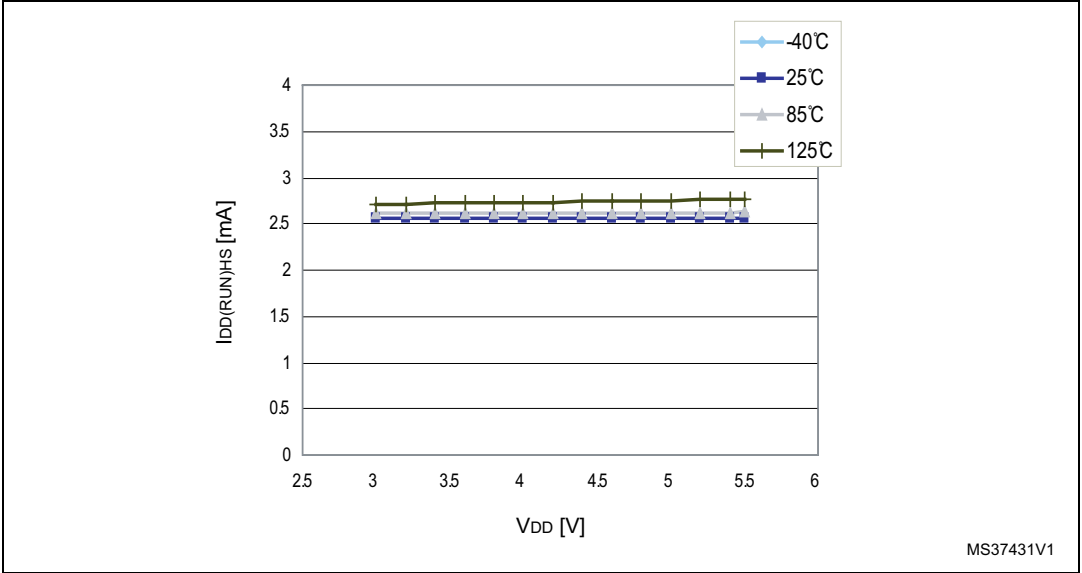


Figure 15. Typ. $I_{DD(WFI)}$ vs V_{DD} , HSI RC osc, $f_{CPU} = 16$ MHz

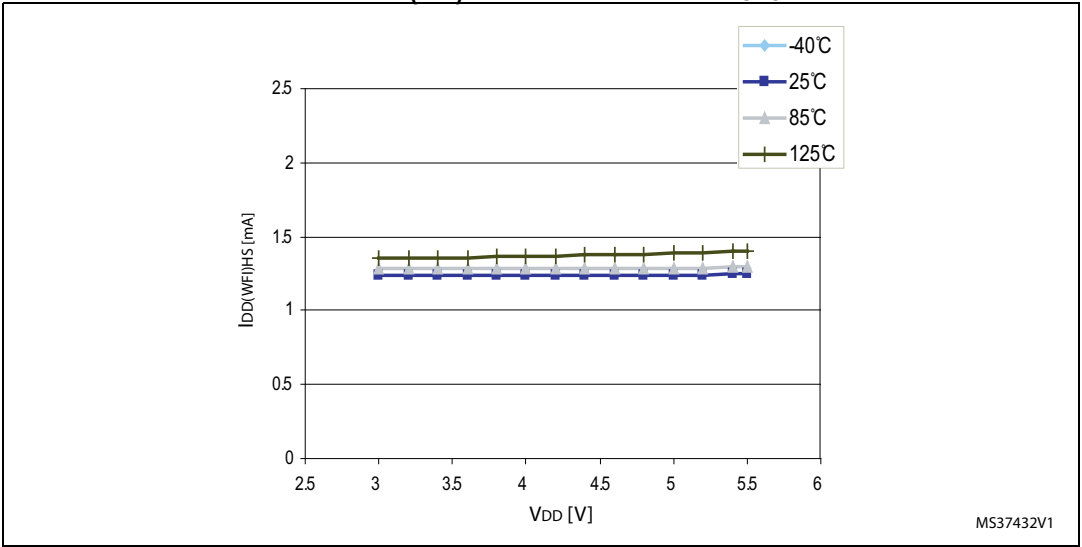
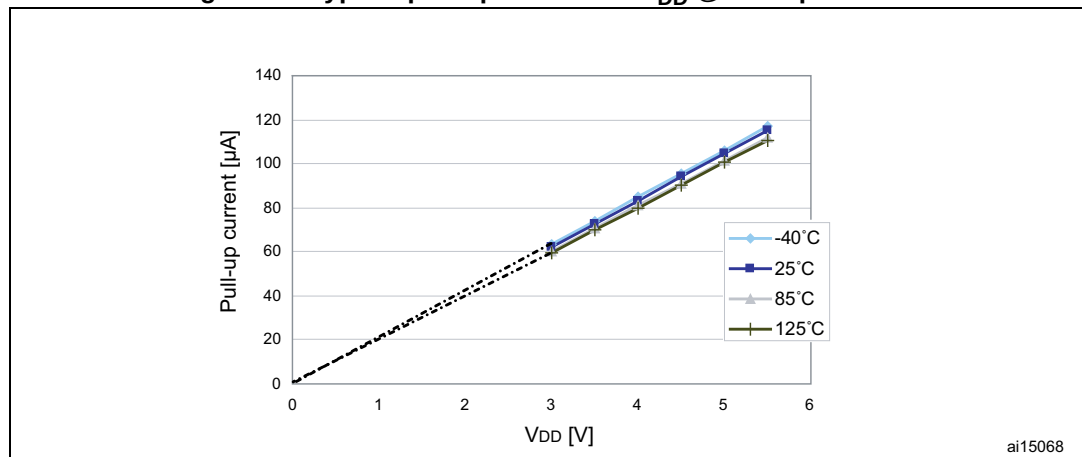


Figure 22. Typical pull-up current vs V_{DD} @ 4 temperatures

1. The pull-up is a pure resistor (slope goes through 0).

Table 38. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$		2	V
	Output low level with 4 pins sunk	$I_{IO} = 4 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$		1 ⁽¹⁾	
V_{OH}	Output high level with 8 pins sourced	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$	2.8		V
	Output high level with 4 pins sourced	$I_{IO} = 4 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$	2.1 ⁽¹⁾		

1. Data based on characterization results, not tested in production

Table 39. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Max	Unit
V_{OL}	Output low level with 2 pins sunk	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$	1	V
		$I_{IO} = 10 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$	1.5 ⁽¹⁾	
		$I_{IO} = 20 \text{ mA}$, $V_{DD} = 5 \text{ V}$	2 ⁽¹⁾	

1. Data based on characterization results, not tested in production

Table 40. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$		0.8	V
	Output low level with 4 pins sunk	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$		1 ⁽¹⁾	
	Output low level with 4 pins sunk	$I_{IO} = 20 \text{ mA}$, $V_{DD} = 5 \text{ V}$		1.5 ⁽¹⁾	
V_{OH}	Output high level with 8 pins sourced	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 5 \text{ V}$	4.0		
	Output high level with 4 pins sourced	$I_{IO} = 10 \text{ mA}$, $V_{DD} = 3.3 \text{ V}$	2.1 ⁽¹⁾		
	Output high level with 4 pins sourced	$I_{IO} = 20 \text{ mA}$, $V_{DD} = 5 \text{ V}$	3.3 ⁽¹⁾		

1. Data based on characterization results, not tested in production

10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 41. NRST pin characteristics

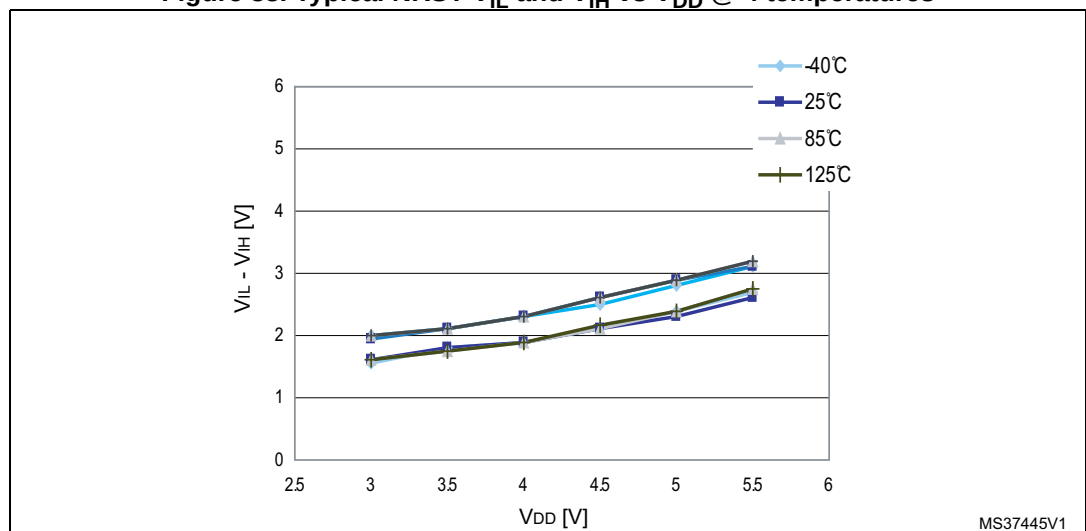
Symbol	Parameter	Conditions	Min	Typ ¹⁾	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage ⁽¹⁾		-0.3 V		$0.3 \times V_{DD}$	V
$V_{IH(NRST)}$	NRST Input high level voltage ⁽¹⁾		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	
$V_{OL(NRST)}$	NRST Output low level voltage ⁽¹⁾	$I_{OL} = 2 \text{ mA}$			0.5	
$R_{PU(NRST)}$	NRST Pull-up resistor ⁽²⁾		30	55	80	k Ω
$t_{IFP(NRST)}$	NRST Input filtered pulse ⁽³⁾				75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse ⁽³⁾		500			ns
$t_{OP(NRST)}$	NRST output pulse ⁽¹⁾		15			μs

1. Data based on characterization results, not tested in production.

2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor

3. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

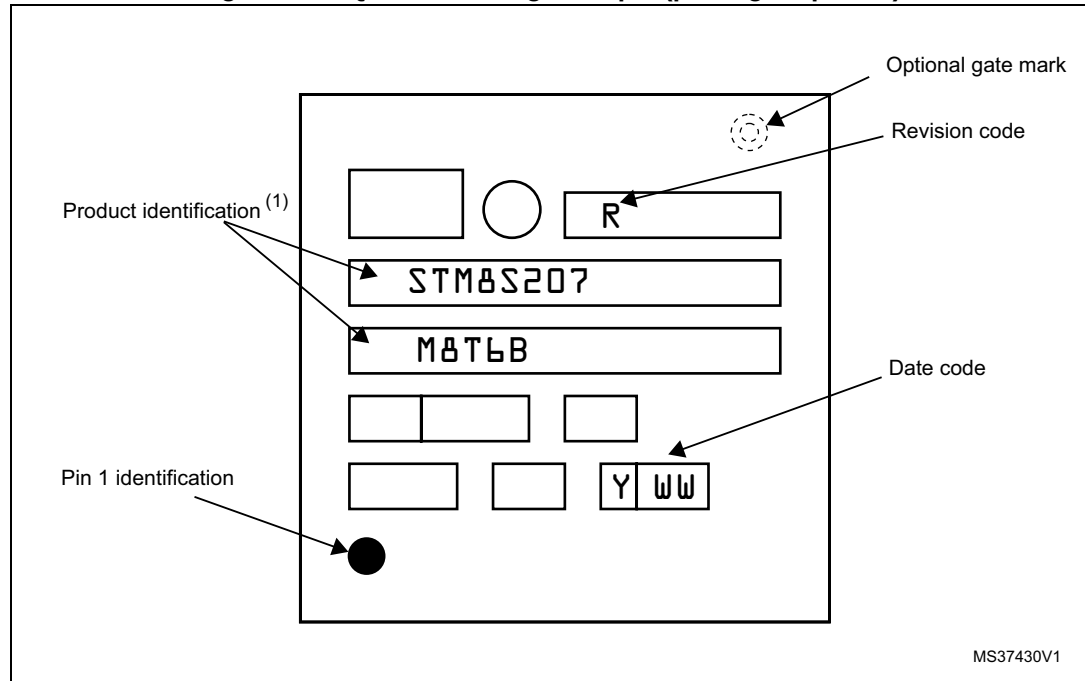


MS37445V1

Device marking

The following figure shows the marking for the LQFP80 package.

Figure 45. LQFP80 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.1.2 LQFP64 package information

Figure 46. LQFP64 - 64-pin 14 mm x 14 mm low-profile quad flat package outline

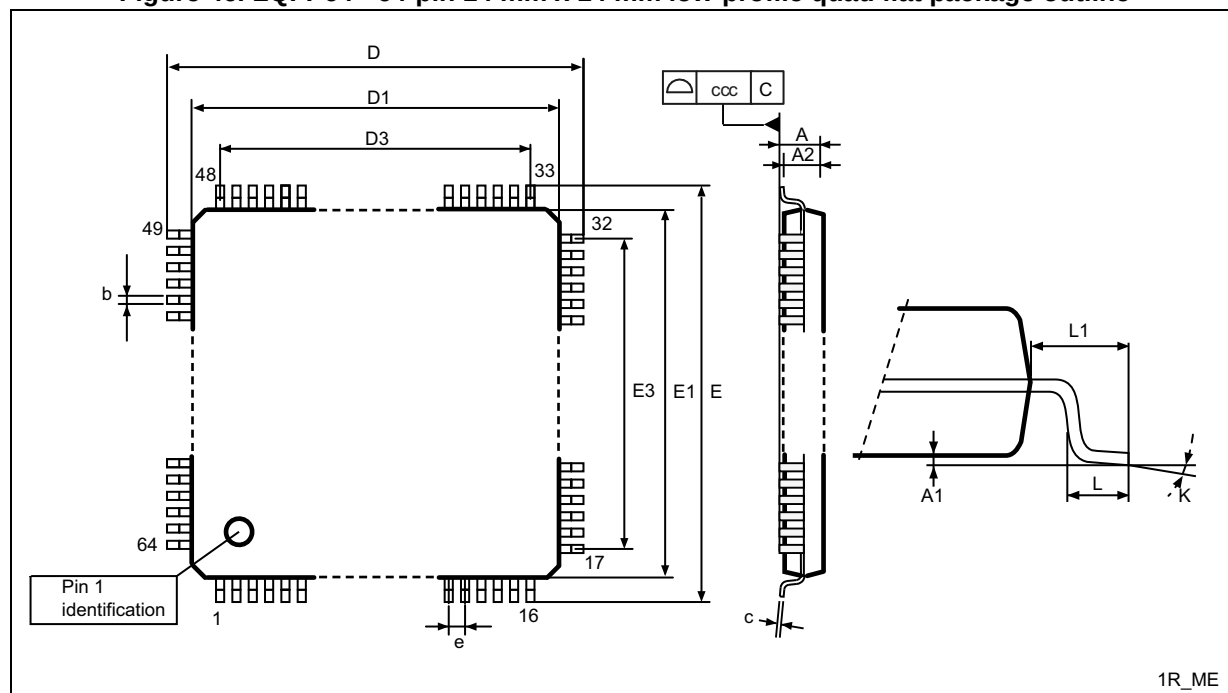


Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
ccc			0.100			0.0039

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

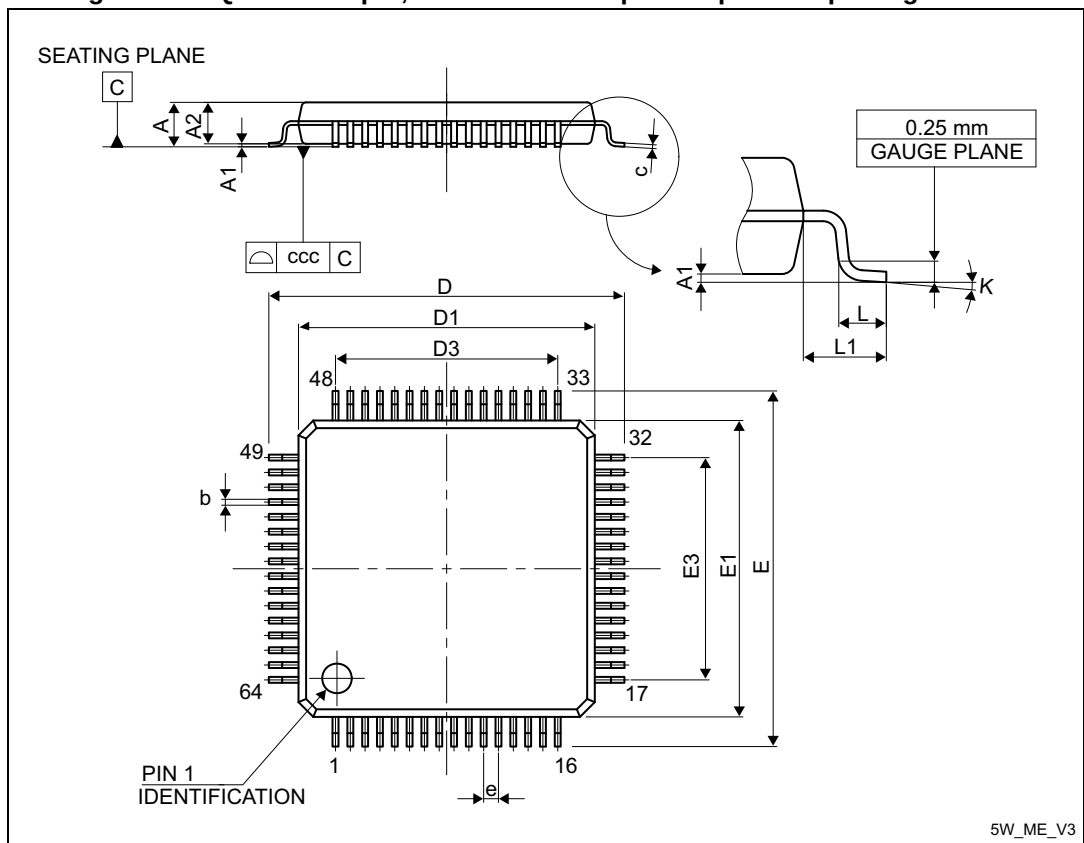


Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

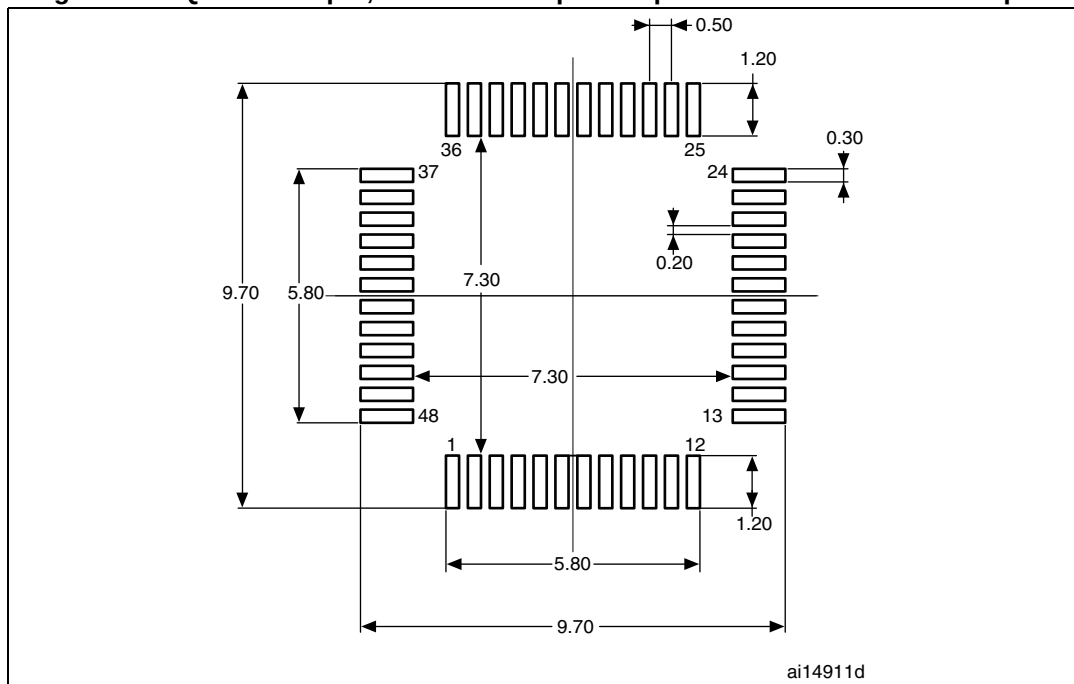
Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079

Table 54. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical (continued)

Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal places.

Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 55. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package mechanical data

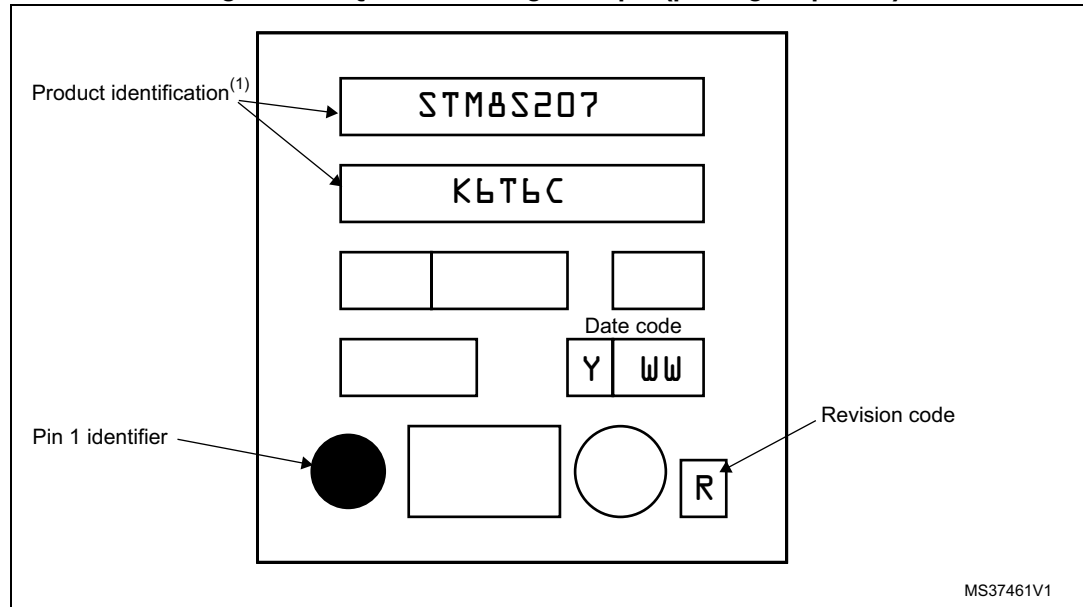
Symbol	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D3	-	8.000	-	-	0.3150	-
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E3	-	8.000	-	-	0.3150	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal places.

Device marking

The following figure shows the marking for the LQFP32 package.

Figure 58. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 18: General operating conditions on page 56](#).

The maximum chip-junction temperature, T_{Jmax} , in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins, where:
 $P_{I/Omax} = \Sigma (V_{OL} \cdot I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \cdot I_{OH})$, and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 57. Thermal characteristics⁽¹⁾

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm	38	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 14 x 14 mm	45	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm	46	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 44 - 10 x 10 mm	54	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

- **Cosmic C compiler for STM8** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- **Raisonance C compiler for STM8** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- **STM8 assembler linker** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link the application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Sep-2010	10	Added part number STM8S208M8 to Table 1: Device summary. Updated “reset state” of Table 5: Legend/abbreviations for pinout table. Added footnote 4 to Table 6: Pin description. Table 9: General hardware register map: standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers; added the reset values of the CAN pagged registers. Figure 36: Recommended reset pin protection: replaced 0.01 μF with 0.1 μF. Figure 40: Typical application with I2C bus and timing diagram: $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{r(SCK)}$, and $t_{f(SCK)}$ replaced by $t_{w(SCLH)}$, $t_{w(SCLL)}$, $t_{r(SCL)}$, and $t_{f(SCL)}$ respectively.
22-Mar-2011	11	Table 1: Device summary: added STM8S207K8. Table 2: STM8S20xxx performance line features: added STM8S207K8 device and changed the RAM value of all other devices to 6 Kbytes. Figure 5, Figure 4, Figure 5, and Figure 7: removed TIM1_CH4 from pins 80, 64, 48, and 32 respectively. Table 6: Pin description: updated note 3 and added note 5. Table 9: General hardware register map: removed I2C_PECR register. Section 10.3.7: Reset pin characteristics: added text regarding the rest network.
10-Feb-2012	12	Figure 1: STM8S20xxx block diagram: updated POR/PDR and BOR; updated LINUART input; added legend. Table 18: General operating conditions: updated V_{CAP}. Table 26: Total current consumption in halt mode at VDD = 5 V: updated title, modified existing max column, and added new max column (at 125 °C) with data. Table 37: I/O static characteristics: added new condition and new max values for rise and fall time; added footnote 3; updated Typ and max pull-up resistor values. Section 10.3.7: Reset pin characteristics: updated cross reference in text below Figure 35 Table 41: NRST pin characteristics: updated Typ and max values of the NRST pull-up resistor.