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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s208mbt6b

1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

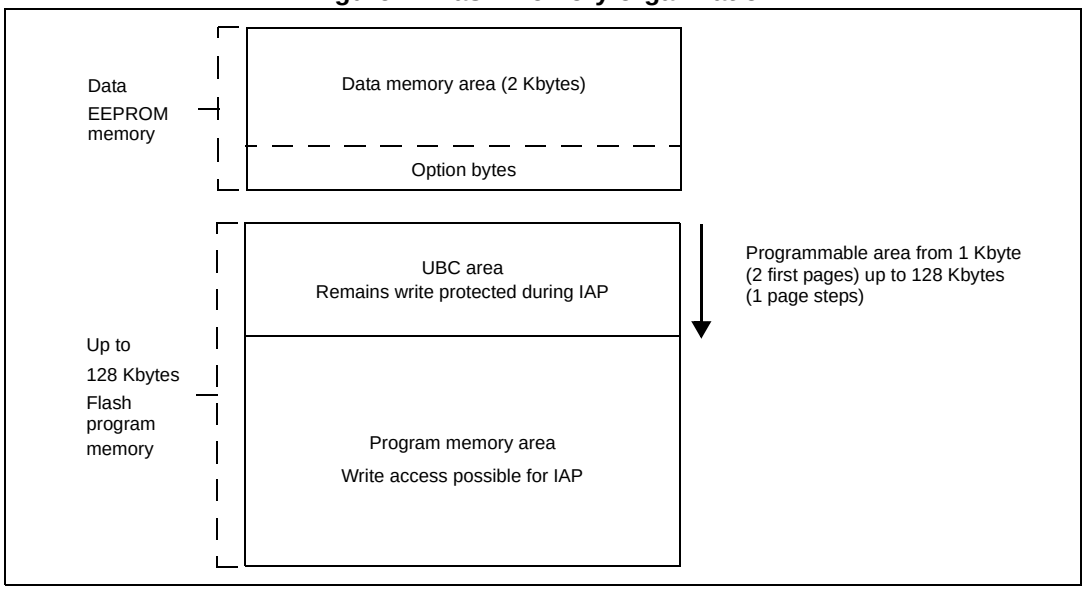
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



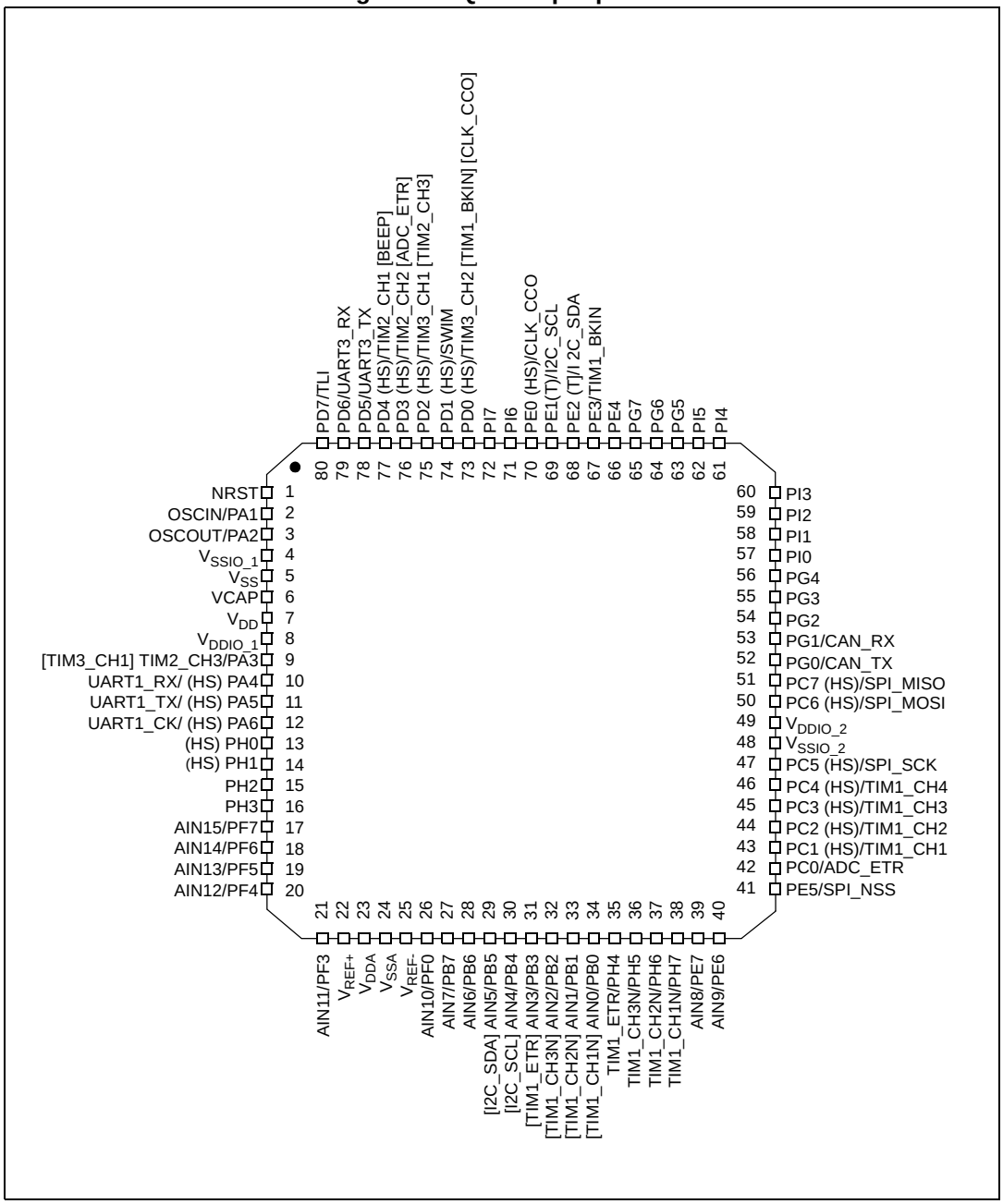
Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

5 Pinouts and pin description

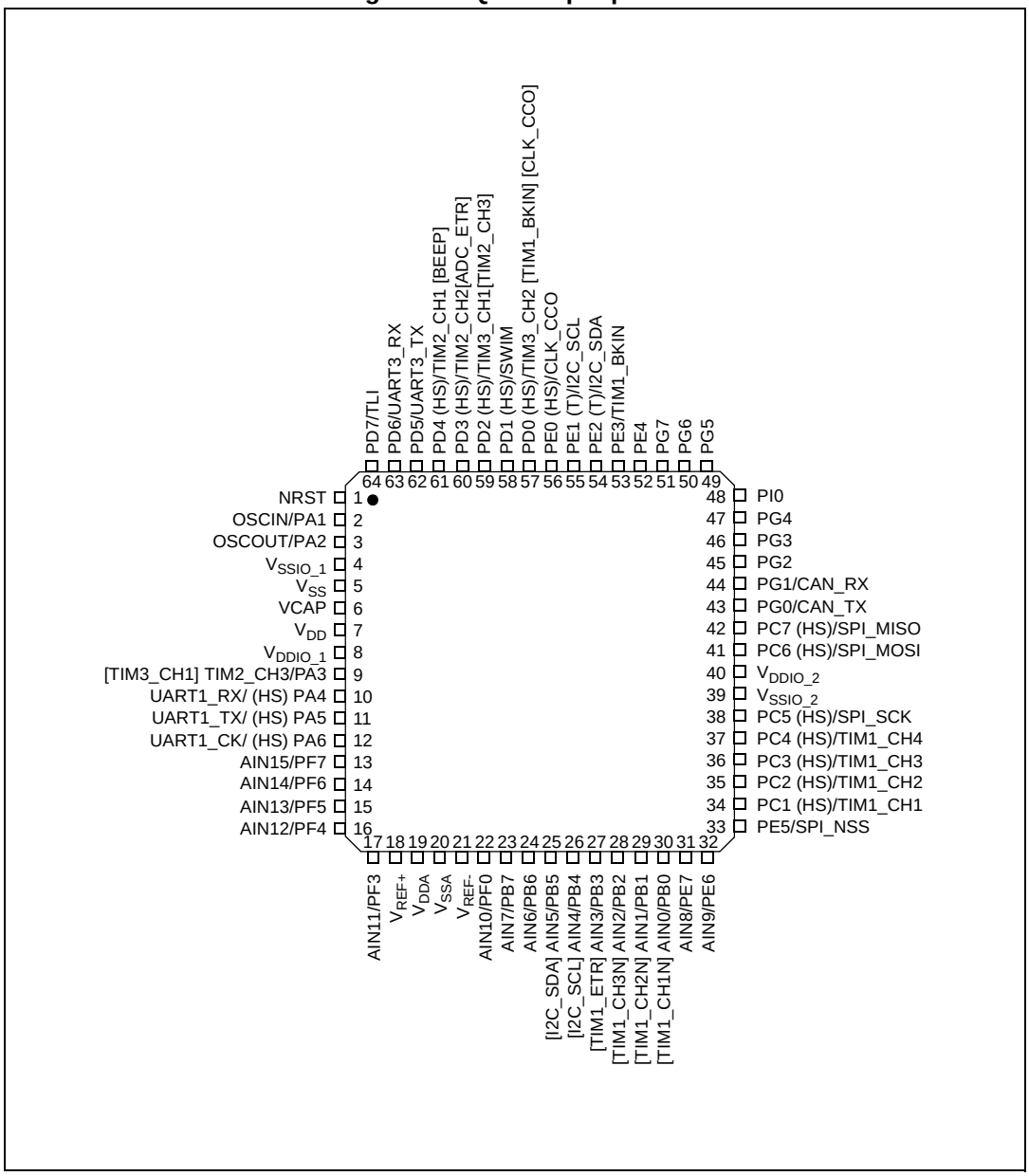
5.1 Package pinouts

Figure 3. LQFP 80-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 6. Pin description (continued)

Pin number					Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP80	LQFP64	LQFP48	LQFP44	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
12	12	12	11	-	PA6/UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port A6**	UART1 synchronous clock	
13	-	-	-	-	PH0	I/O	**X**	X		HS	O3	X	X	**Port H0**		
14	-	-	-	-	PH1	I/O	**X**	X		HS	O3	X	X	**Port H1**		
15	-	-	-	-	PH2	I/O	**X**	X			O1	X	X	**Port H2**		
16	-	-	-	-	PH3	I/O	**X**	X			O1	X	X	**Port H3**		
17	13	-	-	-	PF7/AIN15	I/O	**X**	X			O1	X	X	**Port F7**	Analog input 15	
18	14	-	-	-	PF6/AIN14	I/O	**X**	X			O1	X	X	**Port F6**	Analog input 14	
19	15	-	-	-	PF5/AIN13	I/O	**X**	X			O1	X	X	**Port F5**	Analog input 13	
20	16	-	-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
21	17	-	-	-	PF3/AIN11	I/O	**X**	X			O1	X	X	**Port F3**	Analog input 11	
22	18	-	-	-	V_{REF+}	S								ADC positive reference voltage		
23	19	13	12	9	V_{DDA}	S								Analog power supply		
24	20	14	13	10	V_{SSA}	S								Analog ground		
25	21	-	-	-	V_{REF-}	S								ADC negative reference voltage		
26	22	-	-	-	PF0/AIN10	I/O	**X**	X			O1	X	X	**Port F0**	Analog input 10	
27	23	15	14	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
28	24	16	15	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
29	25	17	16	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
30	26	18	17	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port G data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0x00
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0x00
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0x00
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5428	beCAN	CAN_P0	CAN paged register 0	0xXX(3)
0x00 5429		CAN_P1	CAN paged register 1	0xXX(3)
0x00 542A		CAN_P2	CAN paged register 2	0xXX(3)
0x00 542B		CAN_P3	CAN paged register 3	0xXX(3)
0x00 542C		CAN_P4	CAN paged register 4	0xXX(3)
0x00 542D		CAN_P5	CAN paged register 5	0xXX(3)
0x00 542E		CAN_P6	CAN paged register 6	0xXX(3)
0x00 542F		CAN_P7	CAN paged register 7	0xXX(3)
0x00 5430		CAN_P8	CAN paged register 8	0xXX(3)
0x00 5431		CAN_P9	CAN paged register 9	0xXX(3)
0x00 5432		CAN_PA	CAN paged register A	0xXX(3)
0x00 5433		CAN_PB	CAN paged register B	0xXX(3)
0x00 5434		CAN_PC	CAN paged register C	0xXX(3)
0x00 5435		CAN_PD	CAN paged register D	0xXX(3)
0x00 5436		CAN_PE	CAN paged register E	0xXX(3)
0x00 5437		CAN_PF	CAN paged register F	0xXX(3)
0x00 5438 to 0x00 57FF	Reserved area (968 bytes)			

1. Depends on the previous reset source.
2. Write only register.
3. If the bootloader is enabled, it is initialized to 0x00.

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17(2)
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00

Table 13. Option byte description (continued)

Option byte no.	Description
OPT3	**LSI_EN:** *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wakeup unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0] AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles
OPT6	Reserved
OPT7	**WAITSTATE** *Wait state configuration* This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 1 wait state is required if f_{CPU} > 16 MHz. 0: No wait state 1: 1 wait state

10.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 18*. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	$T_A \leq$ 105 °C	0	24	MHz
			0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor		470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85° C for suffix 6 or T_A = 125° C for suffix 3	44, 48, 64, and 80-pin devices, with output on 8 standard ports, 2 high sink ports and 2 open drain ports simultaneously(4)		443	mW
		32-pin package, with output on 8 standard ports and 2 high sink ports simultaneously(4)		360	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	
		3 suffix version	-40	130(5)	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 11.2: Thermal characteristics on page 108*) with the value for T_{Jmax} given in *Table 18* above and the value for Θ_{JA} given in *Table 57: Thermal characteristics*.
4. Refer to *Section 11.2: Thermal characteristics on page 108* for the calculation method.
5. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Figure 12. f_{CPUmax} versus V_{DD}

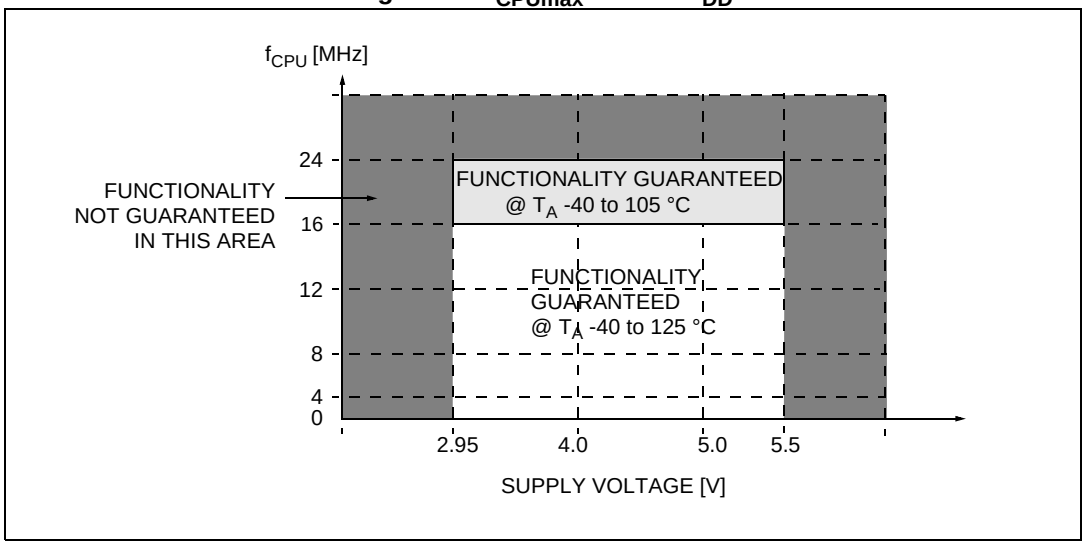


Table 19. Operating conditions at power-up/power-down

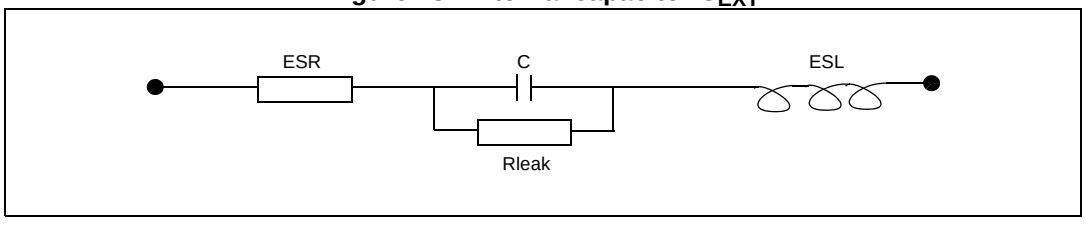
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		2(1)		∞	µs/V
	V_{DD} fall time rate		2(1)		∞	
t_{TEMP}	Reset release delay	V_{DD} rising			1.7(1)	ms
V_{IT+}	Power-on reset threshold		2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold		2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis			70		mV

1. Guaranteed by design, not tested in production.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 18*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 13. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 9 on page 52*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \leq 105$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A.

Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	4.4		mA
			HSE user ext. clock (24 MHz)	3.7	7.3(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.3		
			HSE user ext. clock (16 MHz)	2.7	5.8	
			HSI RC osc. (16 MHz)	2.5	3.4	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.2	4.1(1)	
			HSI RC osc. (16 MHz)	1.0	1.3(1)	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.45		
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	11.4		
			HSE user ext. clock (24 MHz)	10.8	18(1)	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	9.0		
			HSE user ext. clock (16 MHz)	8.2	15.2(1)	
			HSI RC osc.(16 MHz)	8.1	13.2(1)	
		$f_{CPU} = f_{MASTER}$ = 2 MHz.	HSI RC osc. (16 MHz/8)(2)	1.5		
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.1		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.6		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

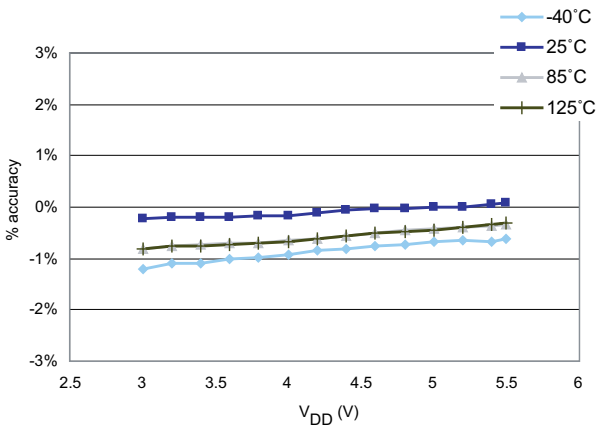
High speed internal RC oscillator (HSI)

Table 33. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions	-1.0(1)		1.0	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-1.5		1.5	
		V_{DD} = 5 V, 25 °C ≤ T_A ≤ 85 °C	-2.2		2.2	
		2.95 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C	-3.0(2)		3.0(2)	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration				1.0(1)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(2)	µA

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production

Figure 18. Typical HSI frequency variation vs V_{DD} at 4 temperatures



10.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

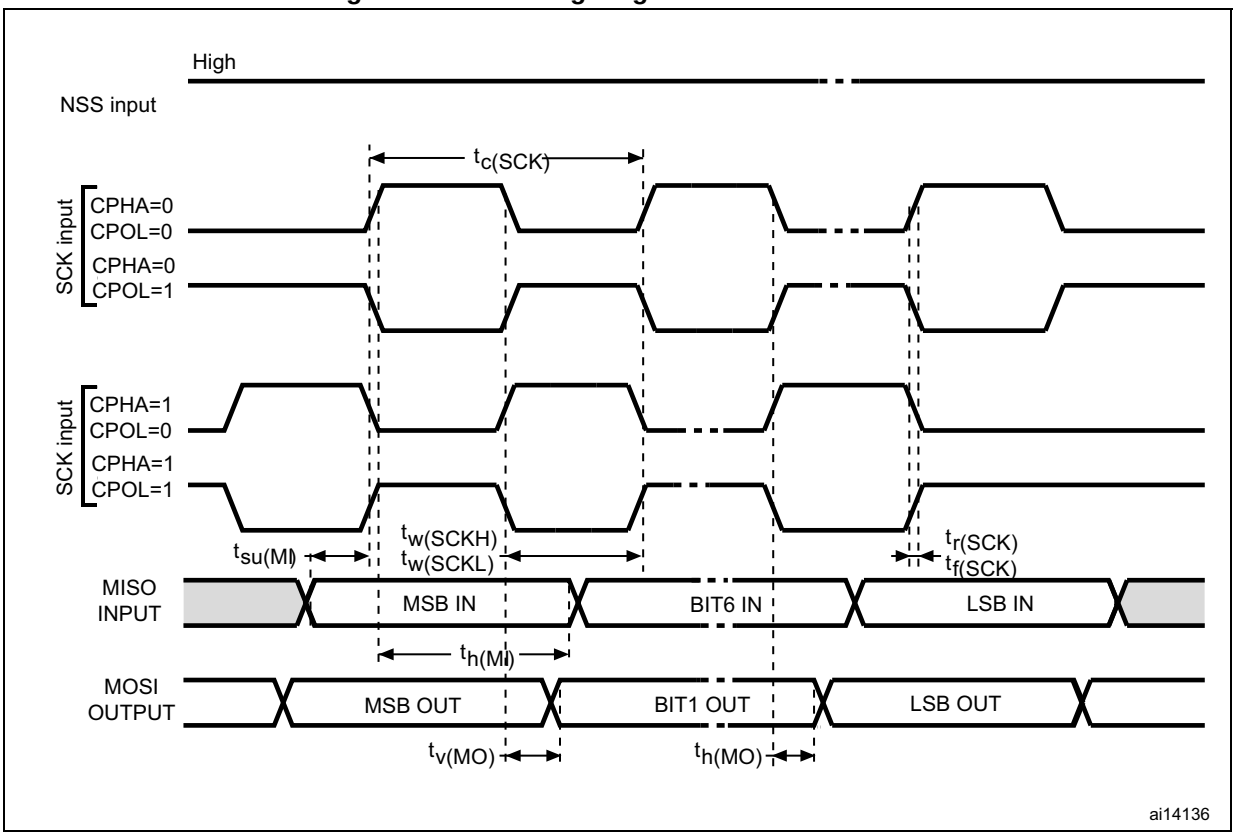
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	10	MHz
		Slave mode	0	6	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ + 15	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		75	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	31		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	12		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 39. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

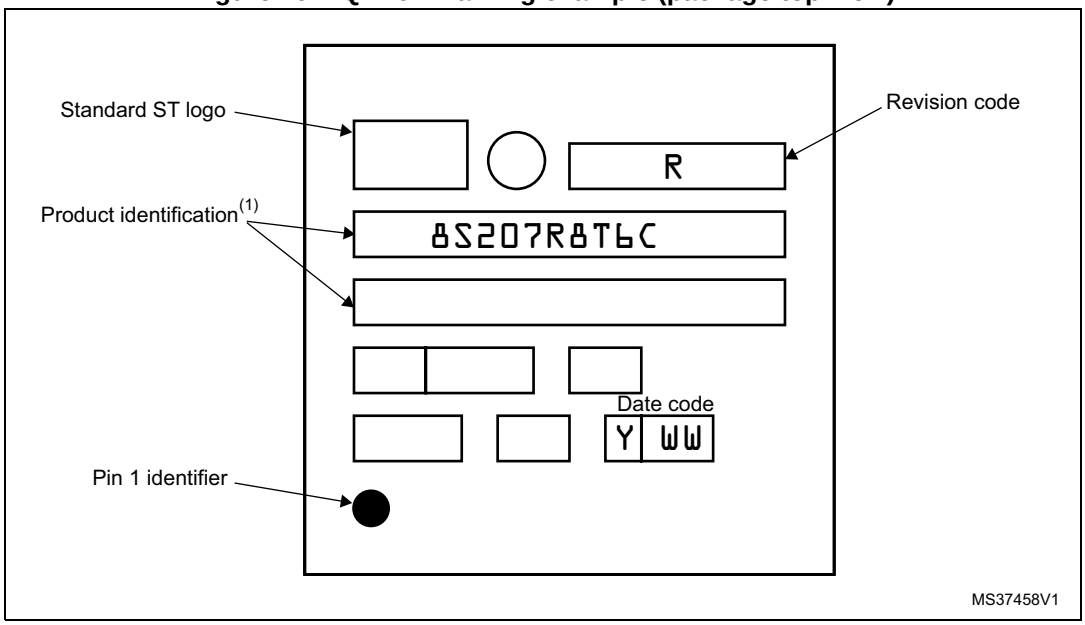
11 Package characteristics

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.

Device marking

The following figure shows the marking for the LQFP64 package.

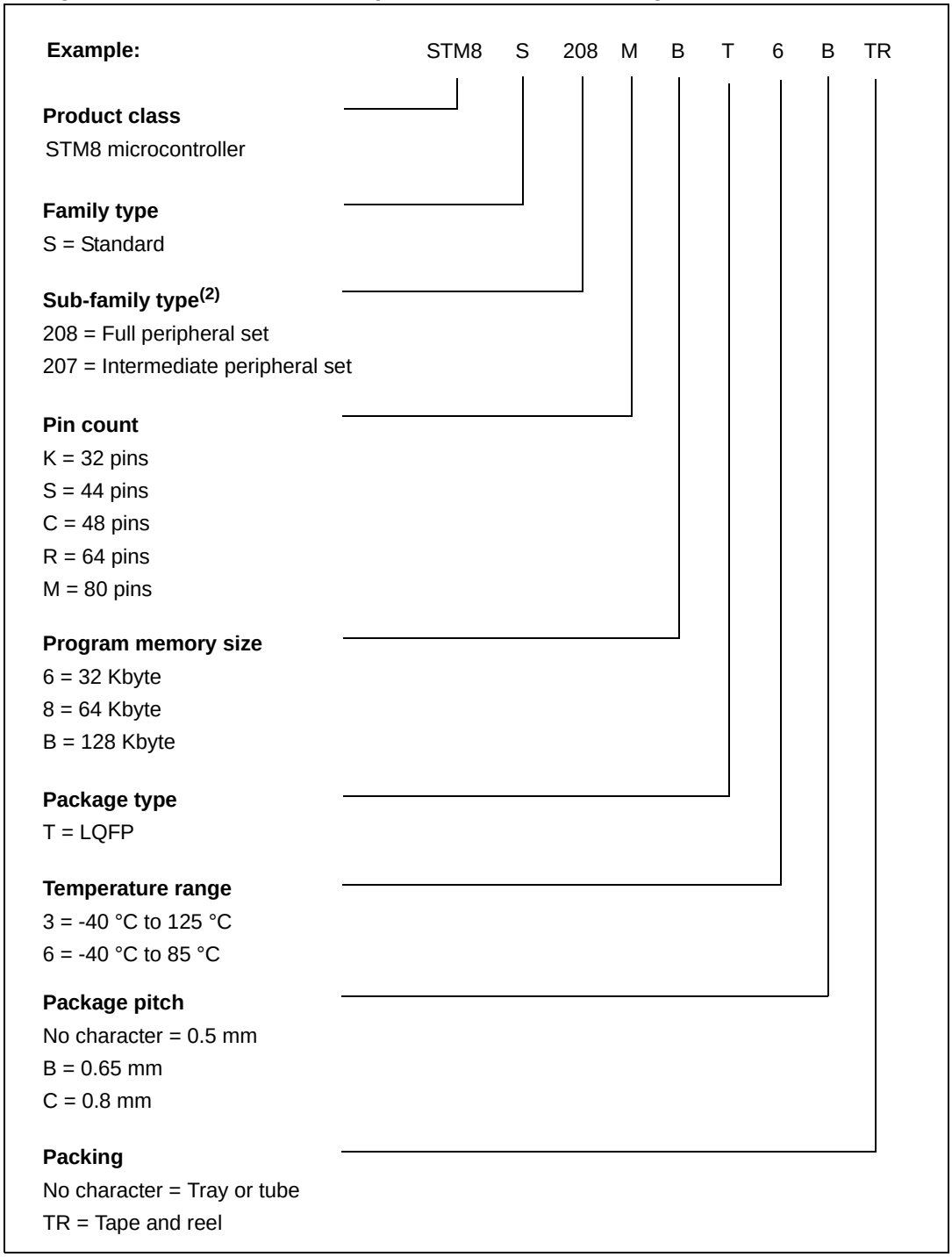
Figure 49. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

13 Ordering information

Figure 59. STM8S207xx/208xx performance line ordering information scheme(1)



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Refer to *Table 2: STM8S20xxx performance line features* for detailed description.