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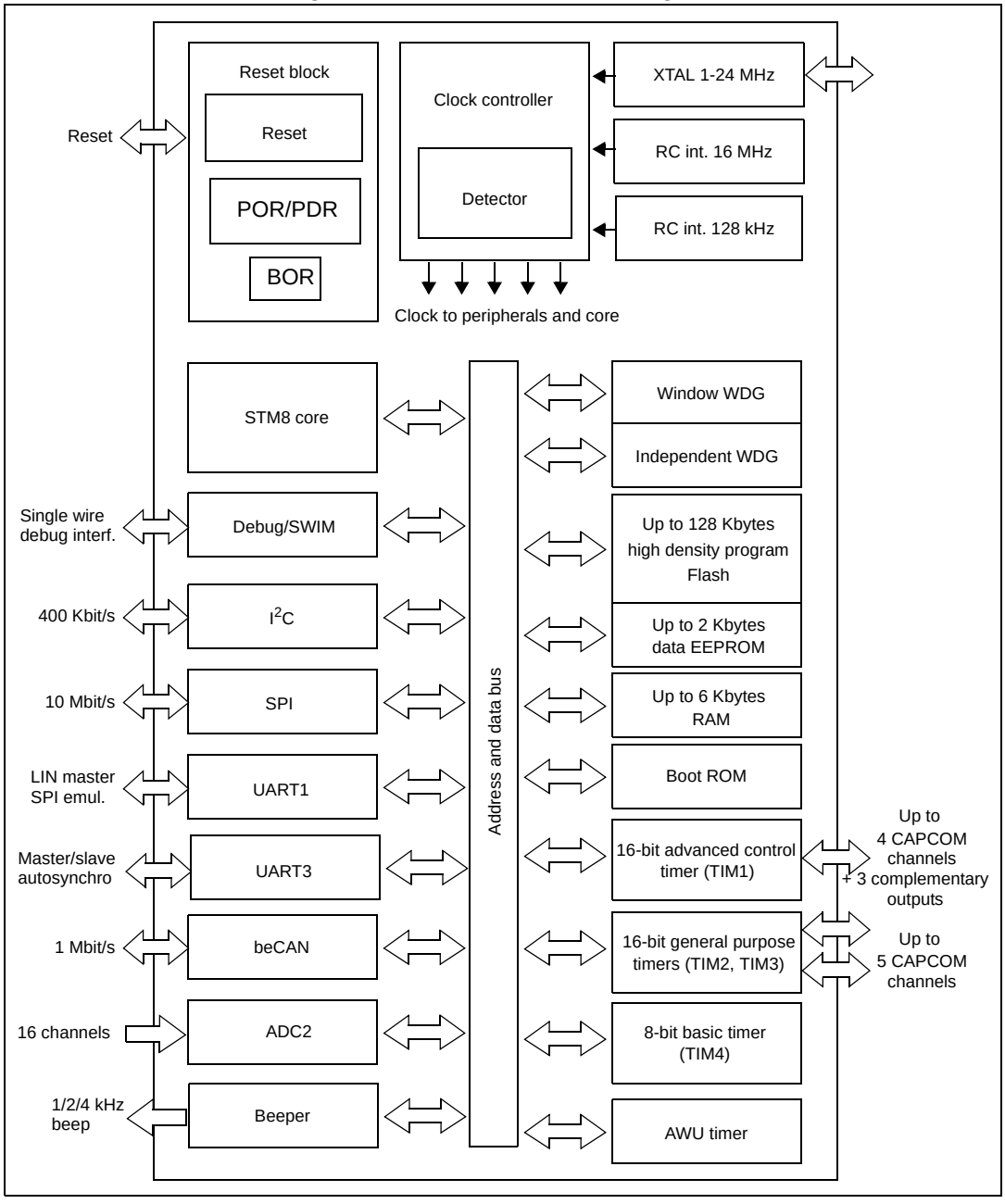
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s208rbt3

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
ADC: Analog-to-digital converter
beCAN: Controller area network
BOR: Brownout reset
I²C: Inter-integrated circuit multimaster interface
Independent WDG: Independent watchdog
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
UART: Universal asynchronous receiver transmitter
Window WDG: Window watchdog

4 Product overview

The following section intends to give an overview of the basic features of the STM8S20xxx functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

4.14.1 UART1

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

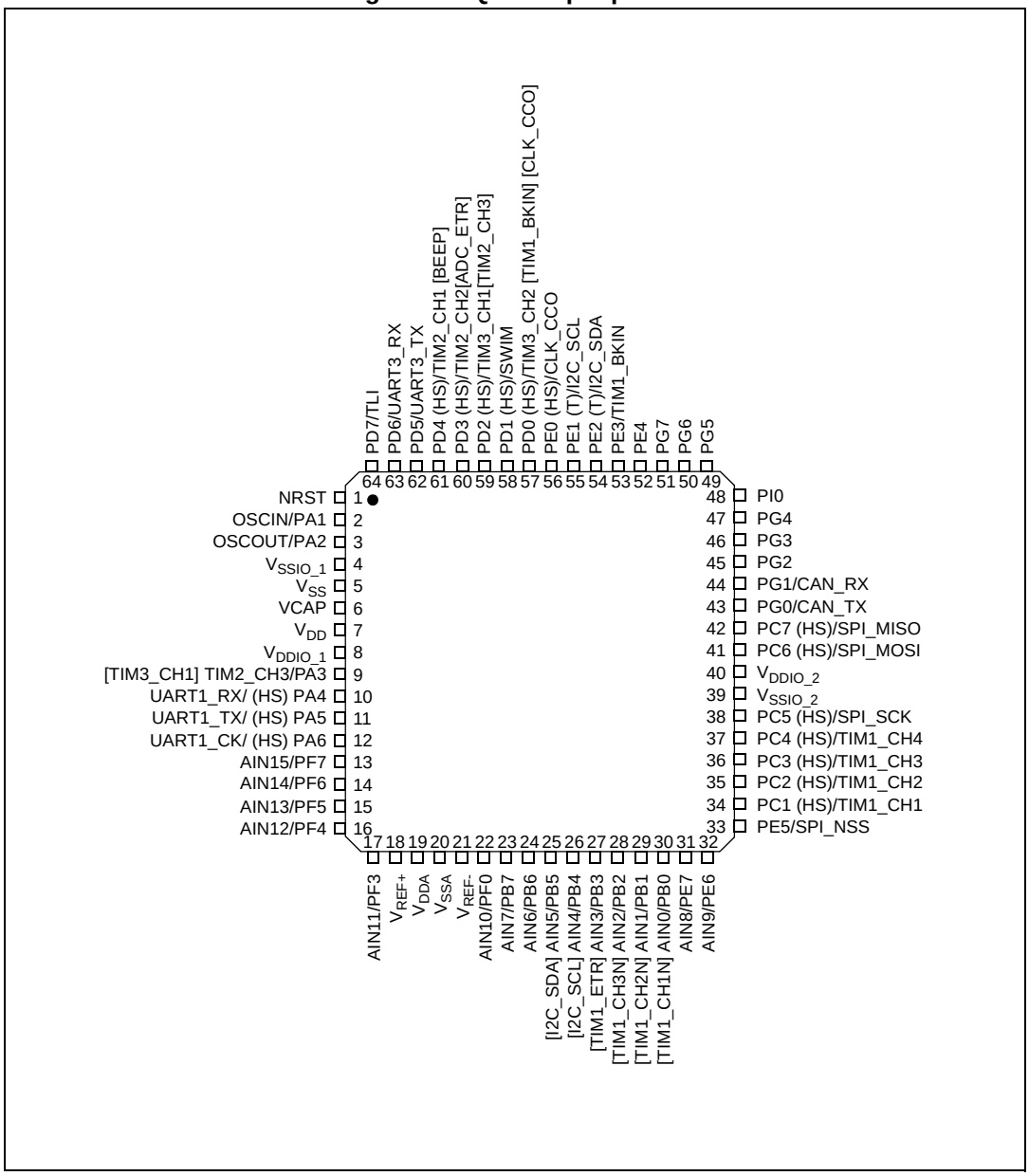
LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15%
- Sync delimiter checking
- 11-bit LIN sync break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050 to 0x00 5059	Reserved area (10 bytes)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	0xXX(1)
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0xXX
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		CLK_CANCCR	CAN clock control register	0x00

Table 13. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 0x00: no UBC, no write-protection 0x01: Pages 0 to 1 defined as UBC, memory write-protected 0x02: Pages 0 to 3 defined as UBC, memory write-protected 0x03: Pages 0 to 4 defined as UBC, memory write-protected ... 0xFE: Pages 0 to 255 defined as UBC, memory write-protected 0xFF: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7***Alternate function remapping option 7* 0: Port D4 alternate function = TIM2_CH1 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CH4 **AFR3** *Alternate function remapping option 3* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: Port D0 alternate function = TIM3_CH2 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: Port A3 alternate function = TIM2_CH3, port D2 alternate function TIM3_CH1 1: Port A3 alternate function = TIM3_CH1, port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: Port D3 alternate function = TIM2_CH2 1: Port D3 alternate function = ADC_ETR

10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 89*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

10.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 18*. In addition, full account must be taken of all physical capacitor characteristics and tolerances.

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	$T_A \leq$ 105 °C	0	24	MHz
			0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor		470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85° C for suffix 6 or T_A = 125° C for suffix 3	44, 48, 64, and 80-pin devices, with output on 8 standard ports, 2 high sink ports and 2 open drain ports simultaneously(4)		443	mW
		32-pin package, with output on 8 standard ports and 2 high sink ports simultaneously(4)		360	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	
		3 suffix version	-40	130(5)	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 11.2: Thermal characteristics on page 108*) with the value for T_{Jmax} given in *Table 18* above and the value for Θ_{JA} given in *Table 57: Thermal characteristics*.
4. Refer to *Section 11.2: Thermal characteristics on page 108* for the calculation method.
5. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Total current consumption in wait mode

Table 22. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.4		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.0		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5		

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 23. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 24 MHz, $T_A \leq$ 105 °C	HSE crystal osc. (24 MHz)	2.0		mA
			HSE user ext. clock (24 MHz)	1.8	4.7	
		$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6		
			HSE user ext. clock (16 MHz)	1.4	4.4	
			HSI RC osc. (16 MHz)	1.2	1.6	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.0		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.55		
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5		

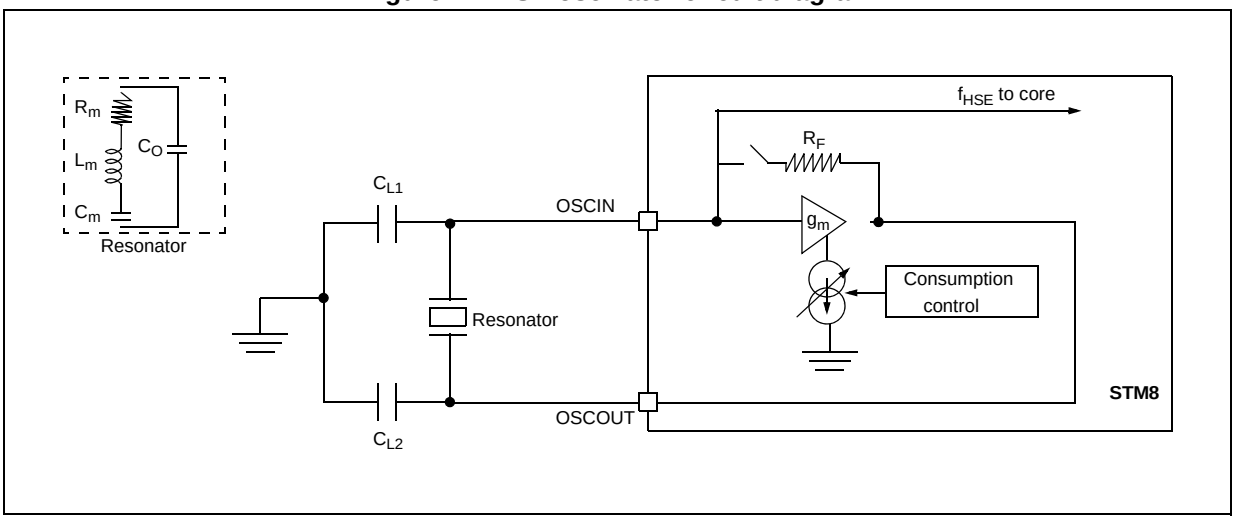
1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		24	MHz
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 24 MHz			6 (startup) 2 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 24 MHz			6 (startup) 1.5 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 34. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		110	128	146	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time				7(1)	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			5		µA

1. Guaranteed by design, not tested in production.

Figure 19. Typical LSI frequency variation vs V_{DD} @ 25 °C

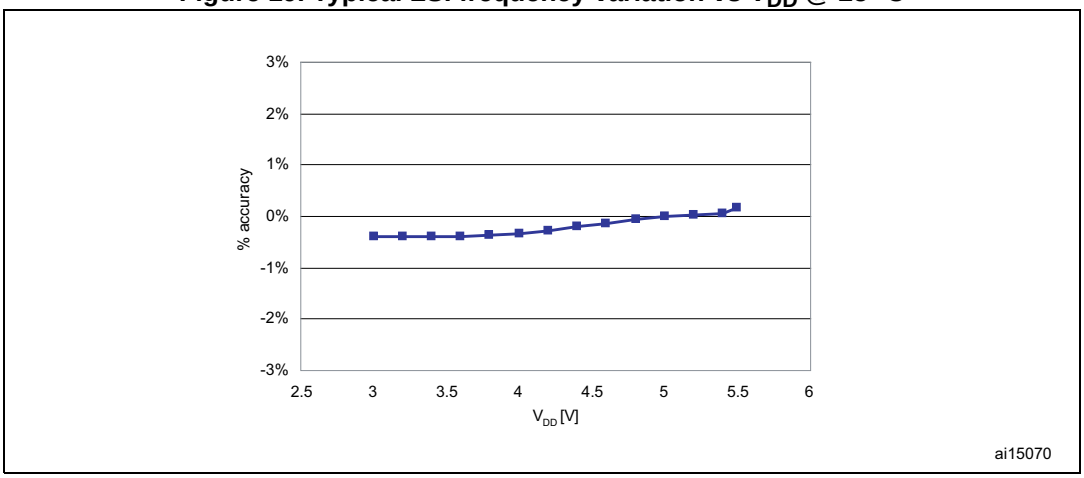


Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

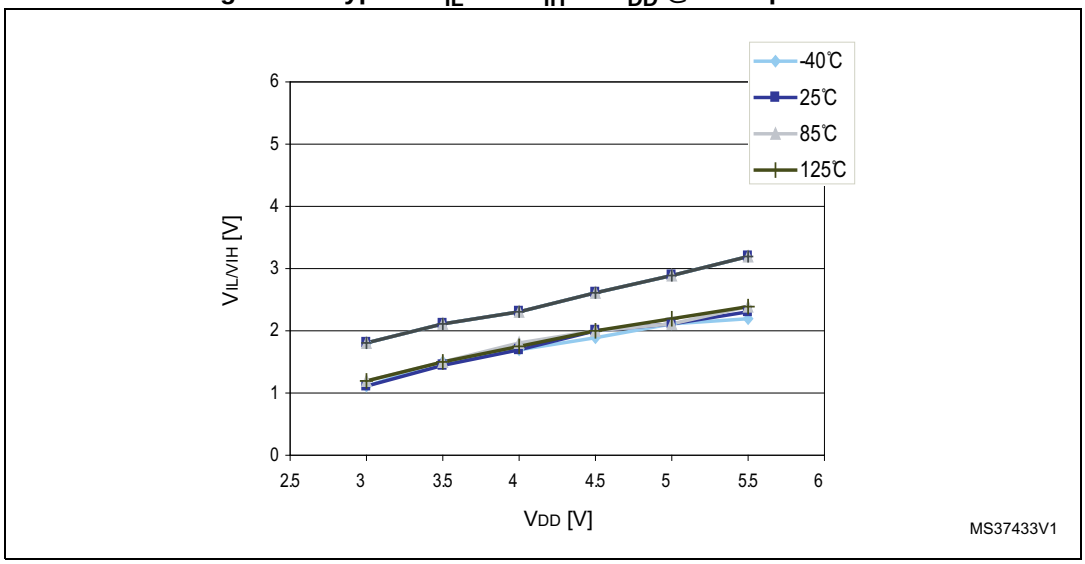
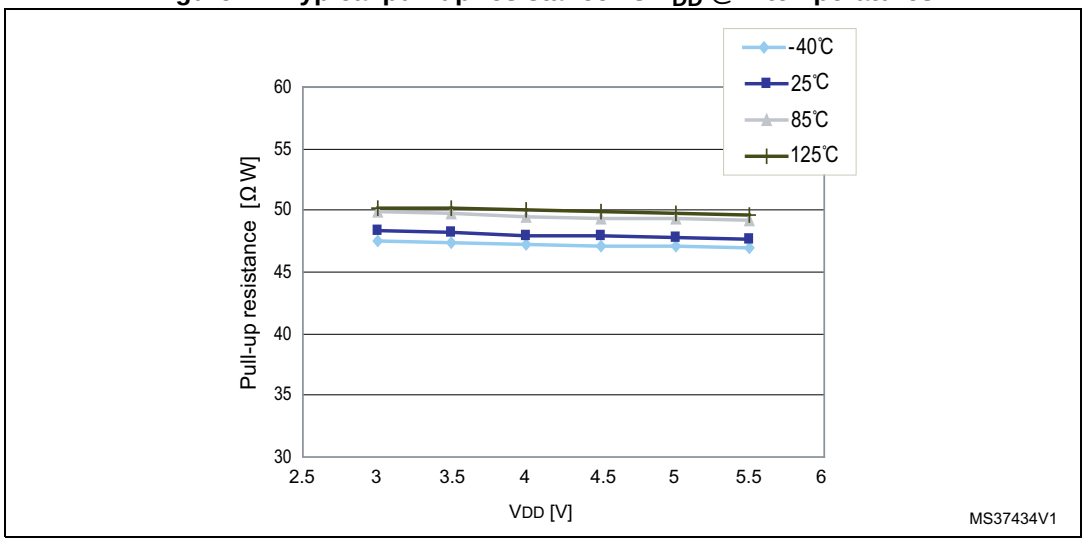


Figure 21. Typical pull-up resistance vs V_{DD} @ 4 temperatures



11.1.3 LQFP48 package information

Figure 50. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline

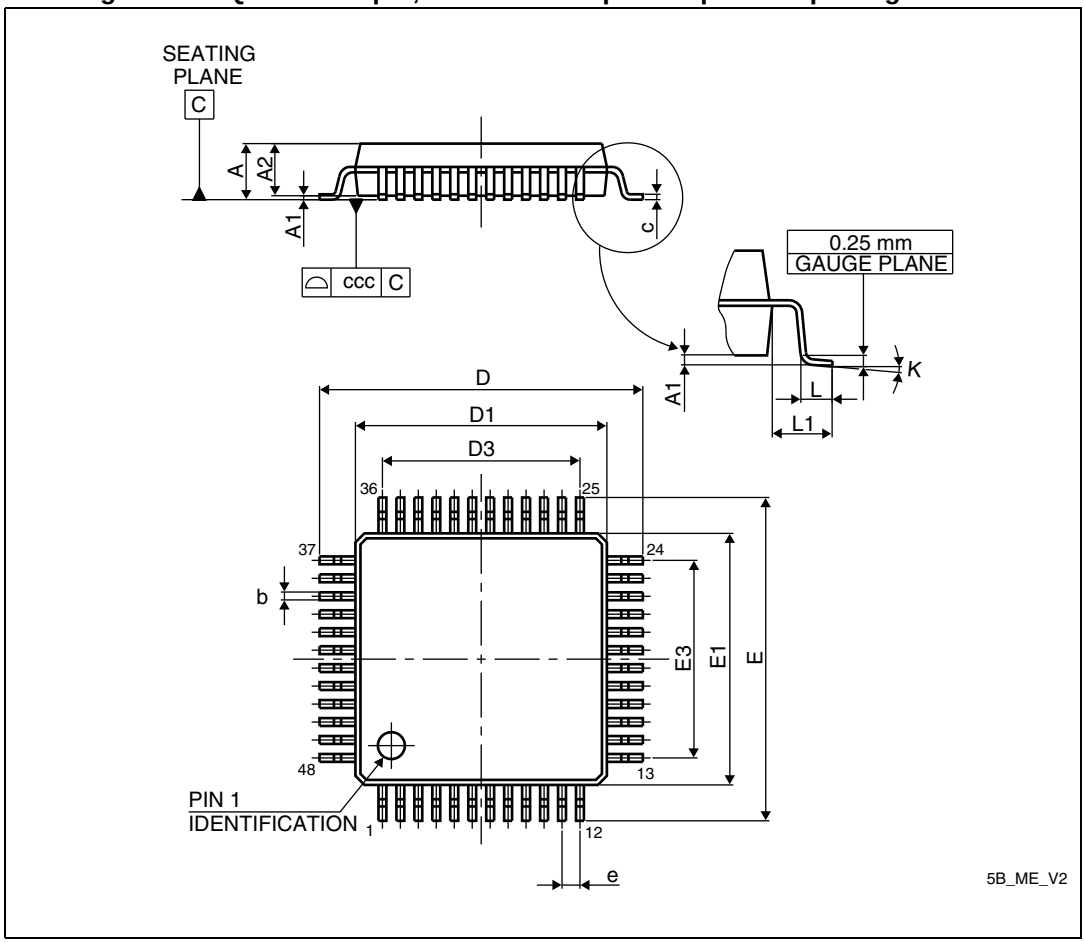


Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com/mcu*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of the application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link the application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 58. Document revision history (continued)

Date	Revision	Changes
10-Jul-2009	8 cont'd	*Section 10: Electrical characteristics*: Added data for TBD values; updated *Table 15: Voltage characteristics* and *Table 18: General operating conditions*; updated VCAP specifications in *Table 18* and in *Section 10.3.1: VCAP external capacitor*; updated *Figure 18*; replaced *Figure 19*; updated *Table 35: RAM and hardware registers*; updated *Figure 22* and *Figure 35*; added *Figure 40: Typical application with I2C bus and timing diagram*. Removed *Table 56: Junction temperature range.* Added link between ordering information *Figure 59* and STM8S20xx features *Table 2*.
13-Apr-2010	9	Document status changed from "preliminary data" to "datasheet". *Table 2: STM8S20xxx performance line features*: high sink I/O for STM8S207C8 is 16 (not 13). *Table 3: Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers*: updated bit positions for TIM2 and TIM3. *Figure 5: LQFP 48-pin pinout*: added CAN_TX and CAN_RX to pins 35 and 36; noted that these pins are available only in STM8S208xx devices. *Figure 7: LQFP 32-pin pinout*: replaced uart2 with uart3. *Table 6: Pin description*: added footnotes concerning beCAN availability and UART1_RX and UART3_RX pins. *Table 13: Option byte description*: added description of STM8L bootloader option bytes to the option byte description table. Added *Section 9: Unique ID* (and listed this attribute in *Features*). *Section 10.3: Operating conditions*: added introductory text. *Table 18: General operating conditions*: replaced "C_{EXT}" with "VCAP" and added data for ESR and ESL; removed "low power dissipation" condition for T_A. *Table 26: Total current consumption in halt mode at VDD = 5 V*: replaced max value of $I_{DD(H)}$ at 85 °C from 30 µA to 35 µA for the condition "Flash in power-down mode, HSI clock after wakeup". *Table 33: HSI oscillator characteristics*: updated the ACC_{HSI} factory calibrated values. *Functional EMS (electromagnetic susceptibility)* and *Table 47*: replaced "IEC 1000" with "IEC 61000". *Electromagnetic interference (EMI)* and *Table 48*: replaced "SAE J1752/3" with "IEC 61967-2". *Table 57: Thermal characteristics*: changed the thermal resistance junction-ambient value of LQFP32 (7x7 mm) from 59 °C/W to 60 °C/W.

Table 58. Document revision history (continued)

Date	Revision	Changes
14-Sep-2010	10	Added part number STM8S208M8 to *Table 1: Device summary*. Updated “reset state” of *Table 5: Legend/abbreviations for pinout table*. Added footnote *4* to *Table 6: Pin description*. *Table 9: General hardware register map*: standardized all reset state values; updated the reset state values of RST_SR, CLK_SWCR, CLK_HSITRIMR, CLK_SWIMCCR, IWDG_KR, and ADC_DRx registers; added the reset values of the CAN paged registers. *Figure 36: Recommended reset pin protection*: replaced 0.01 µF with 0.1 µF. *Figure 40: Typical application with I2C bus and timing diagram*: $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{r(SCK)}$, and $t_{f(SCK)}$ replaced by $t_{w(SCLH)}$, $t_{w(SCLL)}$, $t_{r(SCL)}$, and $t_{f(SCL)}$ respectively.
22-Mar-2011	11	*Table 1: Device summary*: added STM8S207K8. *Table 2: STM8S20xxx performance line features*: added STM8S207K8 device and changed the RAM value of all other devices to 6 Kbytes. *Figure 5*, *Figure 4*, *Figure 5*, and *Figure 7*: removed TIM1_CH4 from pins 80, 64, 48, and 32 respectively. *Table 6: Pin description*: updated note *3* and added note *5*. *Table 9: General hardware register map*: removed I2C_PECR register. *Section 10.3.7: Reset pin characteristics*: added text regarding the rest network.
10-Feb-2012	12	*Figure 1: STM8S20xxx block diagram*: updated POR/PDR and BOR; updated LINUART input; added legend. *Table 18: General operating conditions*: updated V_{CAP}. *Table 26: Total current consumption in halt mode at VDD = 5 V*: updated title, modified existing max column, and added new max column (at 125 °C) with data. *Table 37: I/O static characteristics*: added new condition and new max values for rise and fall time; added footnote *3*; updated Typ and max pull-up resistor values. *Section 10.3.7: Reset pin characteristics*: updated cross reference in text below *Figure 35* *Table 41: NRST pin characteristics*: updated Typ and max values of the NRST pull-up resistor.