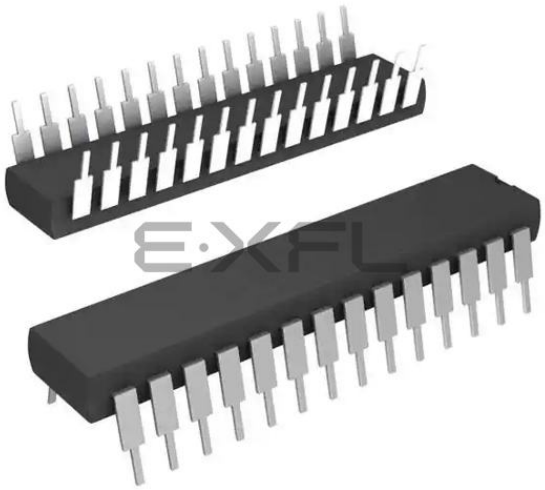

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316pec

PIN DESCRIPTION

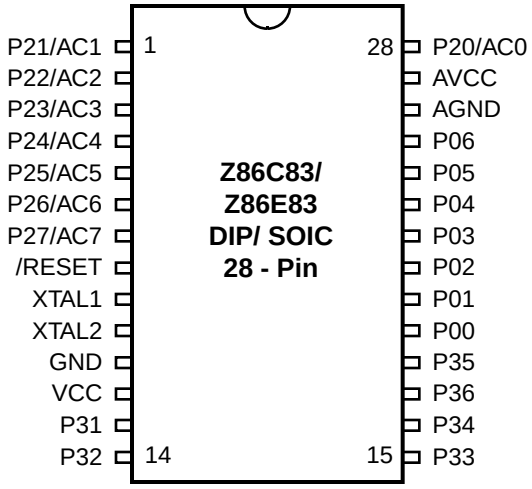

Figure 2. Z86C83 and Standard Mode Z86E83 28-Pin DIP and SOIC Pin Configuration*

Table 1. Z86C83 and Standard Mode Z86E83 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-25	P00-P06	Port 0, Bits 0-6	Input/Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP and SOIC Pin Description and Configuration are identical.

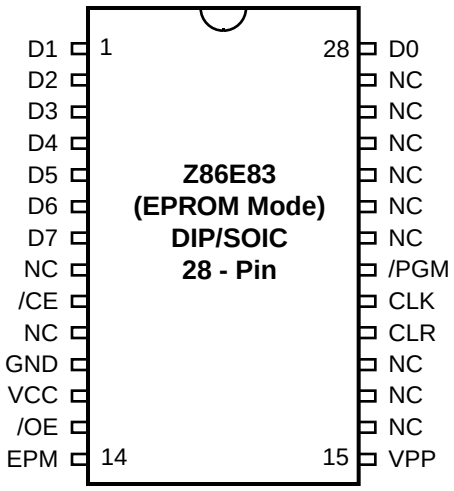

Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

DC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only

Sym	Parameter	V_{CC} Note 3	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC} -0.4		V_{CC} -0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC} -0.4		V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OL} = +10 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	1,4
		5.5V		25		25	20	mA	@ 16 MHz	1,4
		5.0V		7		7	3	mA	@ 3.58 MHz	1,4,15
		5.5V		10		10	5	mA	@ 8 MHz	1,4,15

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

AC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only. Low EMI Mode Only.

				T_A = 0°C to +70°C		T_A = -40° to +105°C			
				4 MHz		4 MHz			
No	**Symbol**	**Parameter**	**V_{CC} [6]**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		ns	1,7,8
			5.5V	3TpC		3TpC		ns	1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC		ns	1,3,7,8
			5.5V	3TpC		3TpC		ns	1,3,7,8
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		ns	1,2,7,8
			5.5V	3TpC		3TpC		ns	1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode
9. For LC oscillator and for oscillator driven by clock driver

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

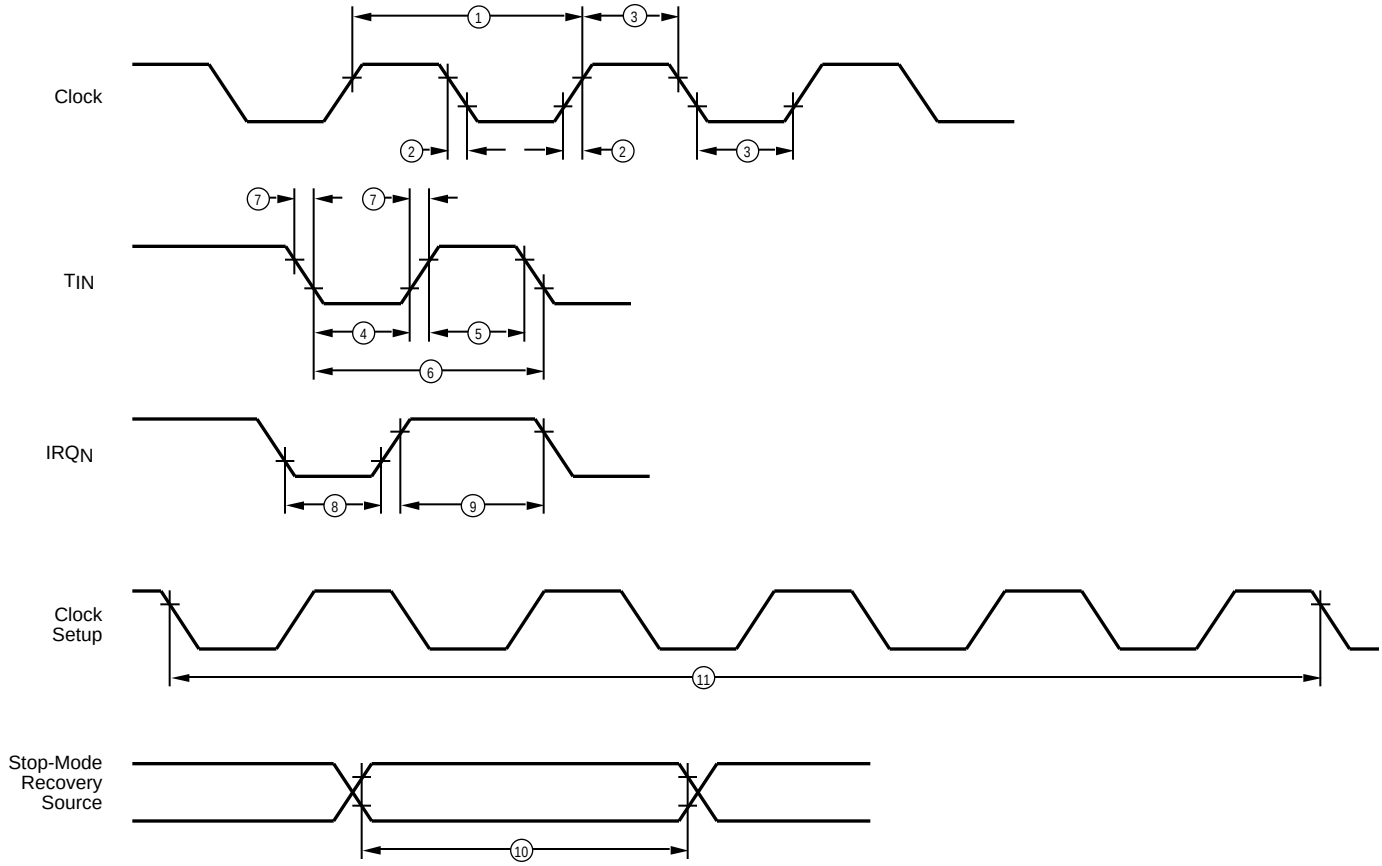

Figure 9. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2) For Z86E83 Only

No	Symbol	Parameter	V_{CC} Note 6	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		15	ns	1
			5.5V		15		15	ns	1
3	TwC	Input Clock Width	3.5V	41		31		ms	1
			5.5V	41		31		ns	1
4	TwTinL	Timer Input Low Width	3.5V	100		100		ms	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1
	TfTin		5.5V		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3
			5.5V	5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12		12		ns	
			5.5V	12		12		ns	
11	Tost	Oscillator Start-up Time	3.5V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time					**WDTMR**	**Reg**	**D1,D0**
			5.5V	6.25		6.25		ms	0,0,[7]
			5.5V	12.5		12.5		ms	0,1,[7]
			5.5V	25		25		ms	1,0,[7]
			5.5V	100		100		ms	1,1,[7]
13	T_{POR}	Power On Reset Delay	3.5V	7	24	7	25	ms	7
			5.5V	3	13	3	14	ms	7

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. Using internal on-board RC oscillator.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Low EMI Mode Only) For Z86E83 Only

No	Symbol	Parameter	V_{CC} [Note 6]	T_A = 0°C to +70°C 4 MHz Min	4 MHz Max	T_A = -40°C to +105°C 4 MHz Min	4 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC			ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25			ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	125				ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100				ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	3TpC					1,7,8
			5.5V	3TpC		3TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	4TpC					1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100			ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100				ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	3TpC					1,3,7,8
			5.5V	3TpC		3TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	3TpC					1,2,7,8
			5.5V	3TpC		2TpC			1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12				ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.5V		5TpC				4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For LC oscillator and for oscillator driven by clock driver

For Z86C84 Only

Table 4. D/A Converter Electrical Characteristics
V_{CC} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	3.0	3.3	3.6	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 3 volts	1.5	1.8	2.1	Volts
VDLO range at 3 volts	0.2	0.5	0.8	Volts
VDHI–VDLO, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 3.0V – 3.6V
Temp: 0–70°C

For Z86C84 Only

Table 5. D/A Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0†	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 5 volts	2.6		3.5	Volts
VDLO range at 5V volts	0.8		1.7	Volts
VDHI–VDLO, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 4.5V - 5.5V
Temp: 0-70°C
† The C86C84 Emulator has maximum setting time of 20 µsec. (10 µsec. typical).

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

PIN FUNCTIONS

EPROM Programming Mode (E83 Only)

D7-D0. *Data Bus.* The data can be read from or written to the EPROM through the data bus.

Clock. *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock signal.

Clear. *Clear.* (active High). This pin resets the internal address counter at the High Level.

$V_{CC.}$ *Power Supply.* This pin must supply 5V during the EPROM Read Mode and 6V during other modes.

/CE. *Chip Enable* (active Low). This pin is active during EPROM Read, Program, and Program Verify Modes.

/OE. *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM. *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

$V_{PP.}$ *Program Voltage.* This pin supplies the program voltage.

/PGM. *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges above V_{cc}*** occur on the /RESET pin.

Processor operation of Z8 OTP devices may be affected by excessive noise surges on the VPP, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to /RESET, VPP, /EPM, /OE
- Adding a capacitor to the affected pin

Z86C83, Z86C84, and Standard Mode Z86E83

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC network to the on-chip oscillator output.

Port 0 P00-P06 (P03-P06 is not available on the Z86C84). Port 0 is a 7-bit, bidirectional, CMOS-compatible I/O port. These seven I/O lines can be nibble programmable as P00-P03 input/output and P04-P06 input/output, separately (Figure 10). All input buffers are Schmitt-triggered and output drivers are push-pull.

Port 0 Auto Latch. (P03-P06 has the Auto Latches permanently enabled). The Auto Latch provides valid CMOS Levels when P03-P06 are selected as inputs and not externally driven. It is impossible to determine if a non-driven input is 1 or 0, however; the Auto Latch will sense the input condition and drive a valid CMOS level, thereby eliminating a floating mode that could cause excessive current.

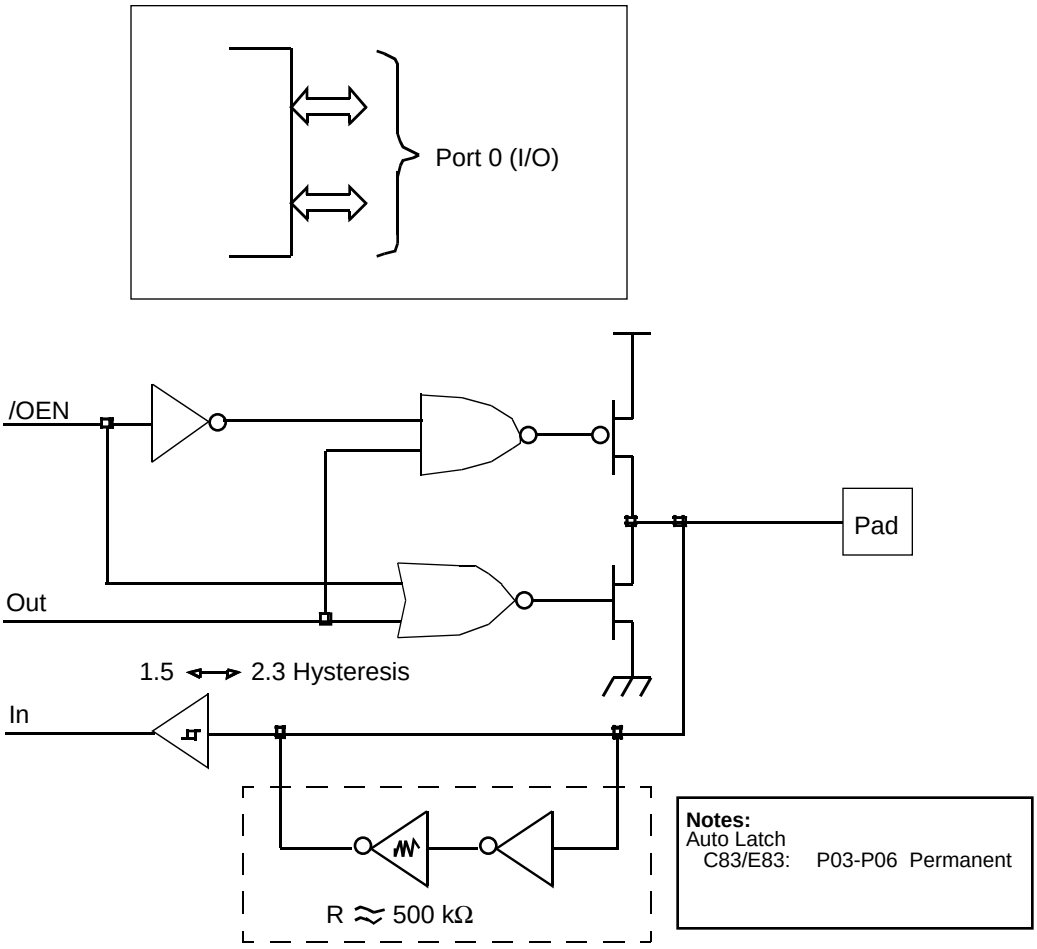

Figure 10. Port 0 Configuration

Port Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 13).

Bit 0 multiplexes comparator AN1 Output at P34. A "1" in this location brings the comparator output to P34 (Figure 14), and a "0" puts P34 into its standard I/O configuration.

Note: Only comparator output AN1 is multiplexed to a Port 3 output. Comparator AN2 output is not connected to any pins. Note that the PCON Register is reset upon the occurrence of a WDT RESET (not in STOP Mode), and Power-On Reset (POR).

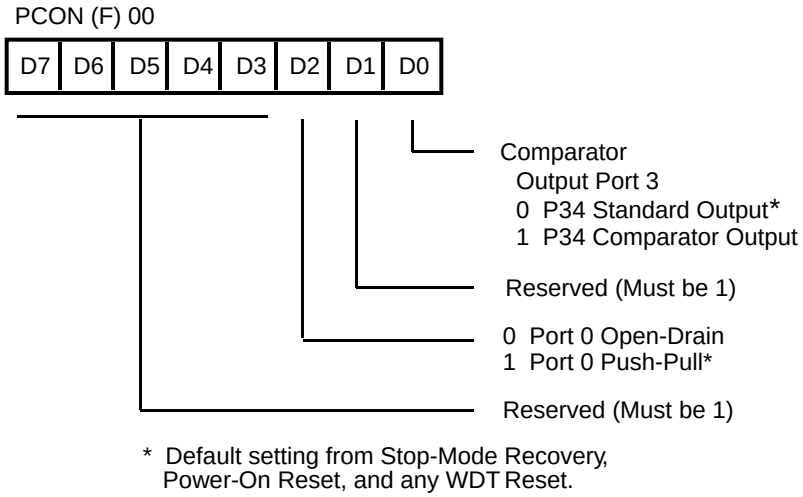

Figure 13. Port Configuration Register (PCON) (Write-Only)

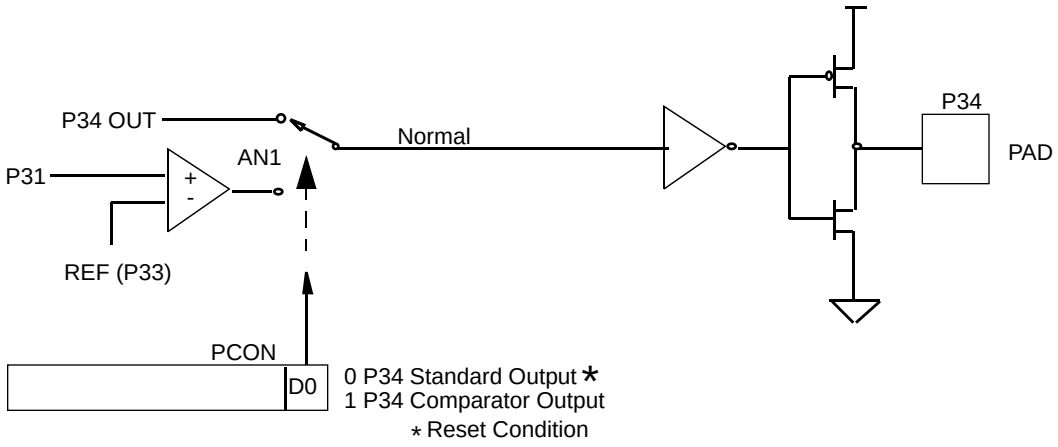

Figure 14. Port 3 P34 Output Configuration

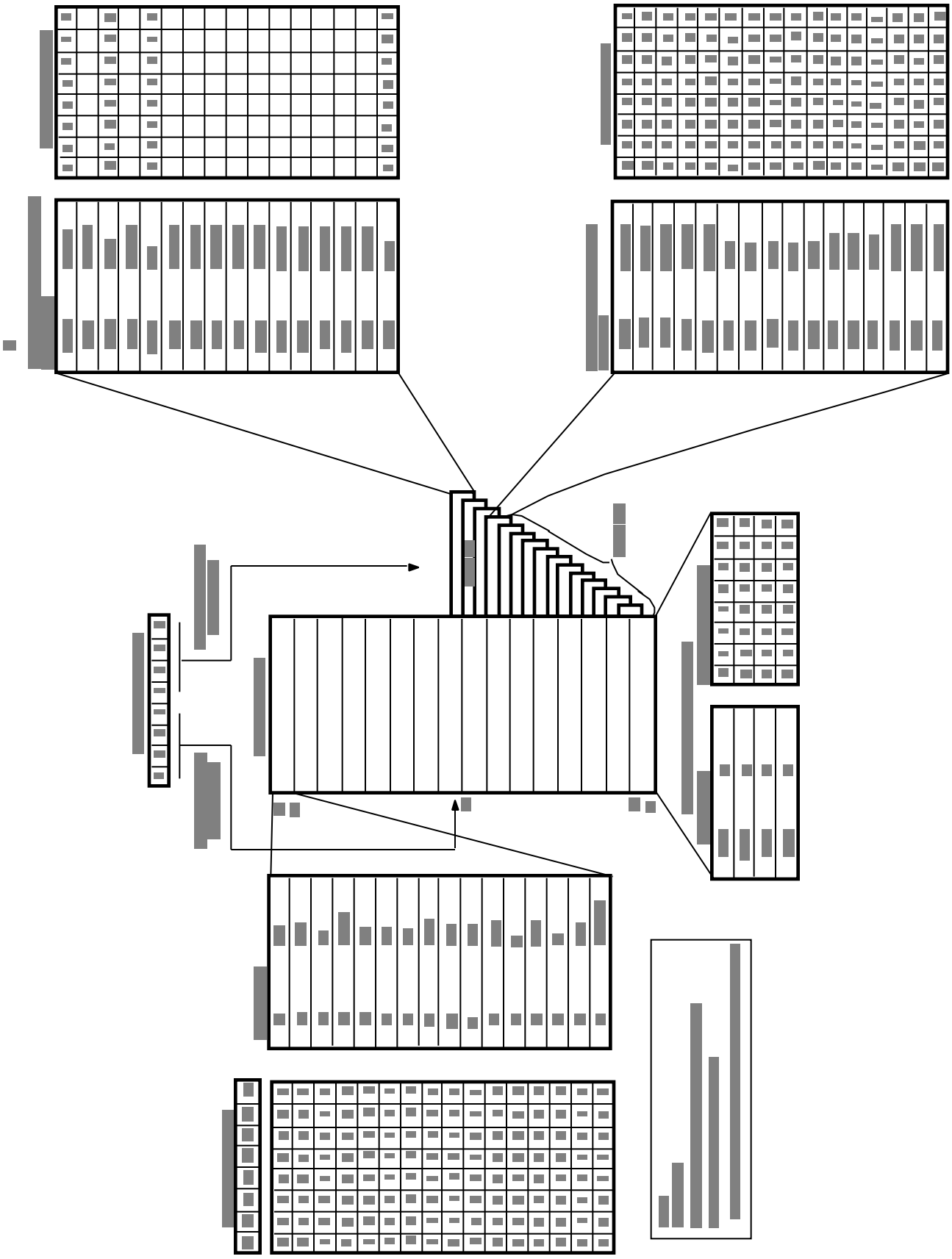

Figure 16. Expanded Register File Architecture

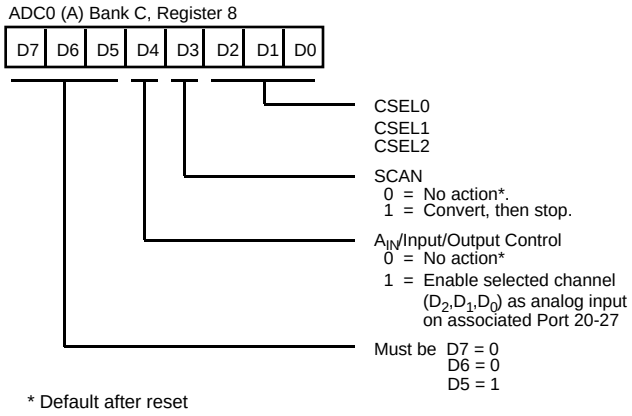

Figure 23. ADC Control Register 0 (Read/Write)

SCAN	
0	No action*
1	Convert channel then stop

Channel Select (bits 2, 1, 0)
* Default after reset

CSEL2	CSEL1	CSEL0	Channel
0	0	0	0 (P20)*
0	0	1	1 (P21)
0	1	0	2 (P22)
0	1	1	3 (P23)
1	0	0	4 (P24)
1	0	1	5 (P25)
1	1	0	6 (P26)
1	1	1	7 (P27)

Note: ADCO D4 must equal 1 to allow Port bit as ADC input.

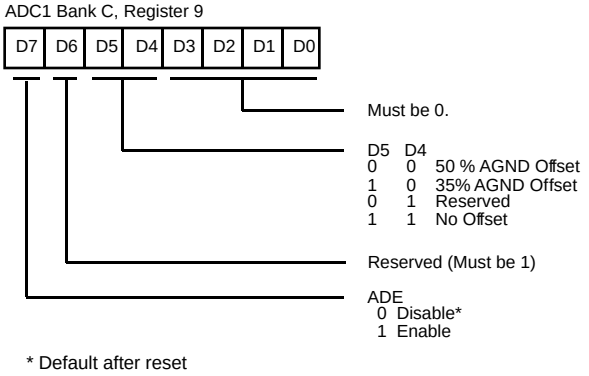

Figure 24. ADC Control Register 1 (Read/Write)

ADE (bit 7). A zero powers down and disables power and any A/D conversions or accessing any ADC registers except writing to ADE bit. A one Enables all ADC accesses. ADC result register is shown in Figure 25.

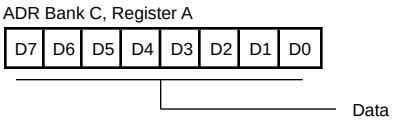

Figure 25. Result Register (Read-Only)

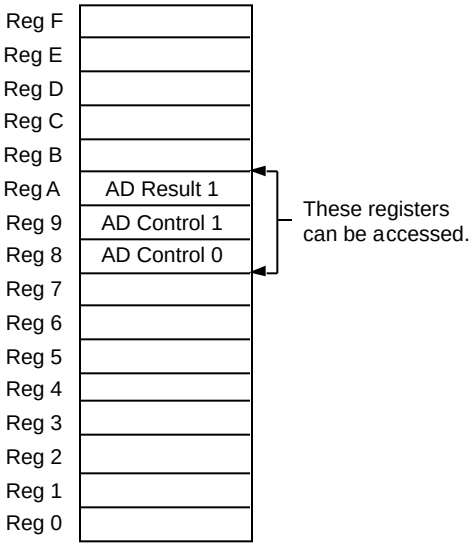

Figure 26. Bank C

FUNCTIONAL DESCRIPTION (Continued)

Figure 27 shows the input circuit of the ADC. When conversion starts the analog input voltage is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Effectively, shunting 31 parallel internal resistance of the analog switches and simultaneously charging 31 parallel 0.5 pF capacitors, which is equivalent to seeing a 400 Ohms input impedance in parallel with a 16 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. For input source resistances up to 2 Kohms can be used under normal operating condition without any degradation of the input settling time. For larger input source resistance, increasing conversion cycle time or adding a capacitor to the input may be required to compensate the input settling time problem.

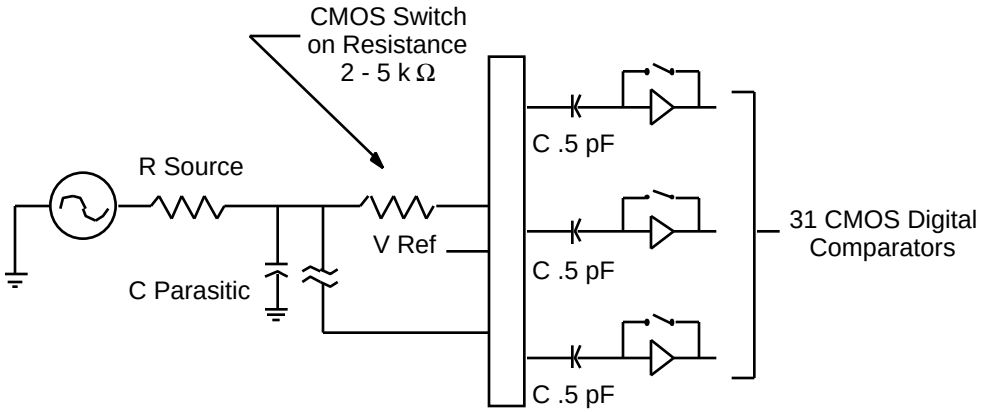

Figure 27. Input Impedance of ADC

Typical Z8 A/D Conversion Sequence

3. Set the register pointer to Extended Bank (C), that is, SRP #%0C instruction.

4. Next, set ADE flag by loading ADC1 Control Register Bank (C) Register 9, bit 7. Also, load bits 0-4 of this same register to select a AV_{CC} or A_{GND} offset value. A precision voltage divider connected to the A/D resistive ladder can offset conversion dynamic range to specified limits within the AV_{CC} and A_{GND} limits. By loading Bank (C) Register 9, bits 0-4, with the appropriate value it is possible to select from these groups:

   a. No Offset. The Converter Dynamic range is from 0V to 5.0V for AV_{CC} = 5.0V.

   b. 35 Percent A_{GND} Offset. The Converter Dynamic range is 1.75V - 5.0V for AV_{CC} = 5.0V.

   c. 50 Percent A_{GND} Offset. The Converter Dynamic range is 2.5V - 5.0V for AV_{CC} = 5.0V.

5. Select one of the eight A/D inputs for conversion by loading Bank (C) Register 8 with the desired attributes: Bits 0 - 2 select an A/D input, bits 3 and 4 select A/D conversion (or digital port I/O).

6. Set Bank (C) Register 8, bit 3 to enable A/D conversion. (This flag can be set concurrently with step 3.) This flag is automatically reset when the A/D conversion is completed, so a bit test can be performed to determine A/D readiness if necessary.

7. Read the A/D result in Bank (C) Register A. Please note that the A/D result is not valid (indeterminate) unless ADE flag (Register 9, bit 7) was previously set, otherwise A/D converter output is tri-stated.

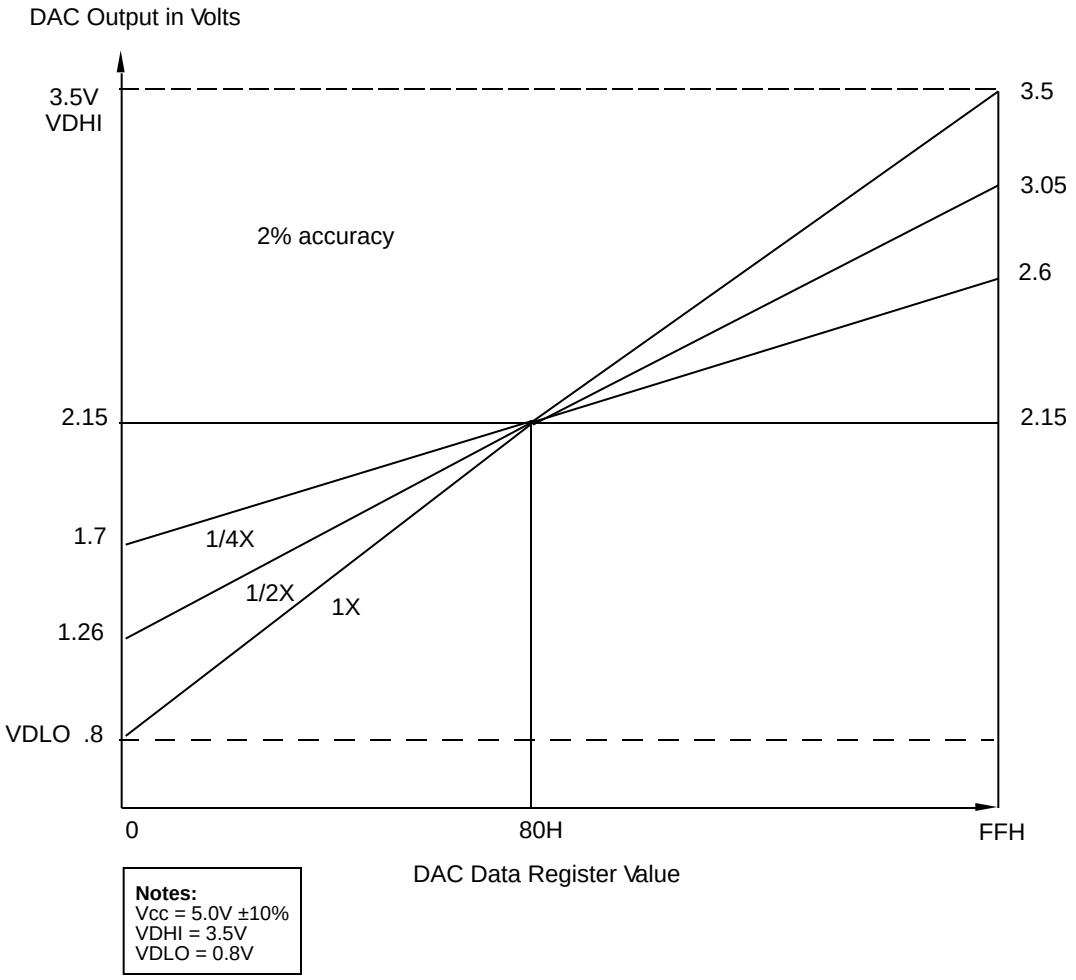

Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, that is**,**

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery (SMR) Register. This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 34 and Figure 35). All bits are Write-Only, except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR Register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR Register is located in Bank F of the Expanded Register Group at address 0BH. When the Stop-Mode Recovery sources are selected in this register, then SMR2 Register bits D0,D1 must be set to 0.

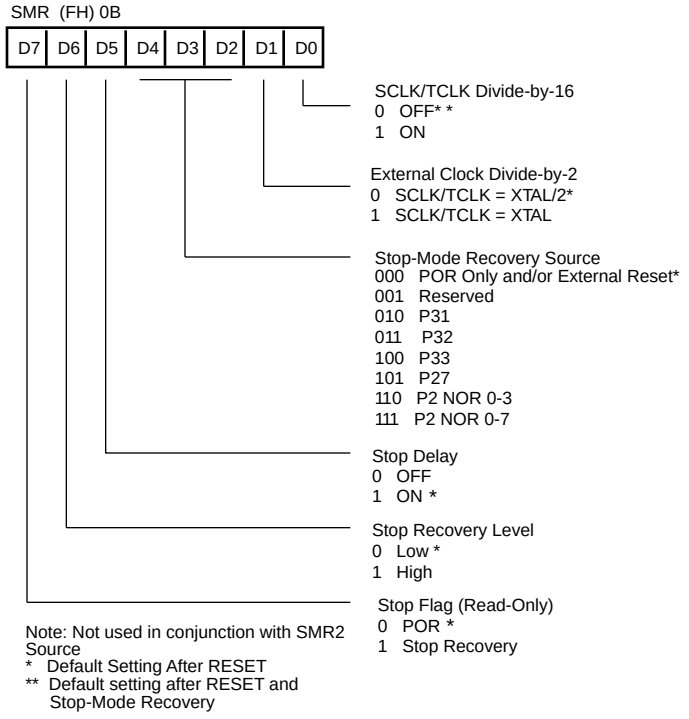

Figure 34. Stop-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

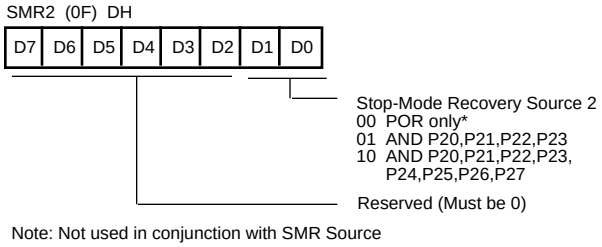

Figure 35. Stop-Mode Recovery Register 2 ([0F] DH: Write-Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery, WDT Time-out, and POR.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock HALT Mode frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 8 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

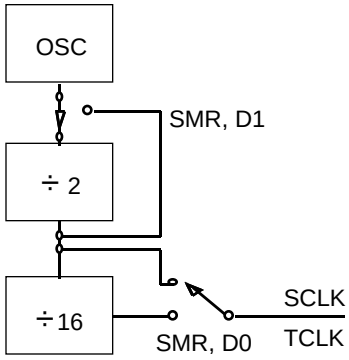

Figure 36. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake-up source of the STOP recovery (Figure 37 and Table 13). When the Stop-Mode Recovery Sources are selected in this register then SMR2 register bits D0,D1 must be set to zero. P33-P31 and Port 2 cannot wake up from STOP Mode if the input lines are configured as analog inputs to the Analog comparator or Analog-to-Digital Converter.

Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.

Table 13. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} /RESET delay after Stop-Mode Recovery. The default configuration of this bit is "1". A POR or WDT reset will override the selection and cause the reset delay to occur.

Stop-Mode Recovery Edge Select (D6). A "1" in this bit position indicates that a high level on the output to the exclusive Or-Gate input from the selected recovery source wakes the Z86C83/C84/E83 from STOP Mode. A "0" indicates low-level recovery. The default is 0 on POR. This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT reset. A "1" in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: A WDT reset out of STOP Mode will also set this bit to a "1".

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

Table 14. Stop-Mode Recovery Source

SMR:10		Operation
D1	D0	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

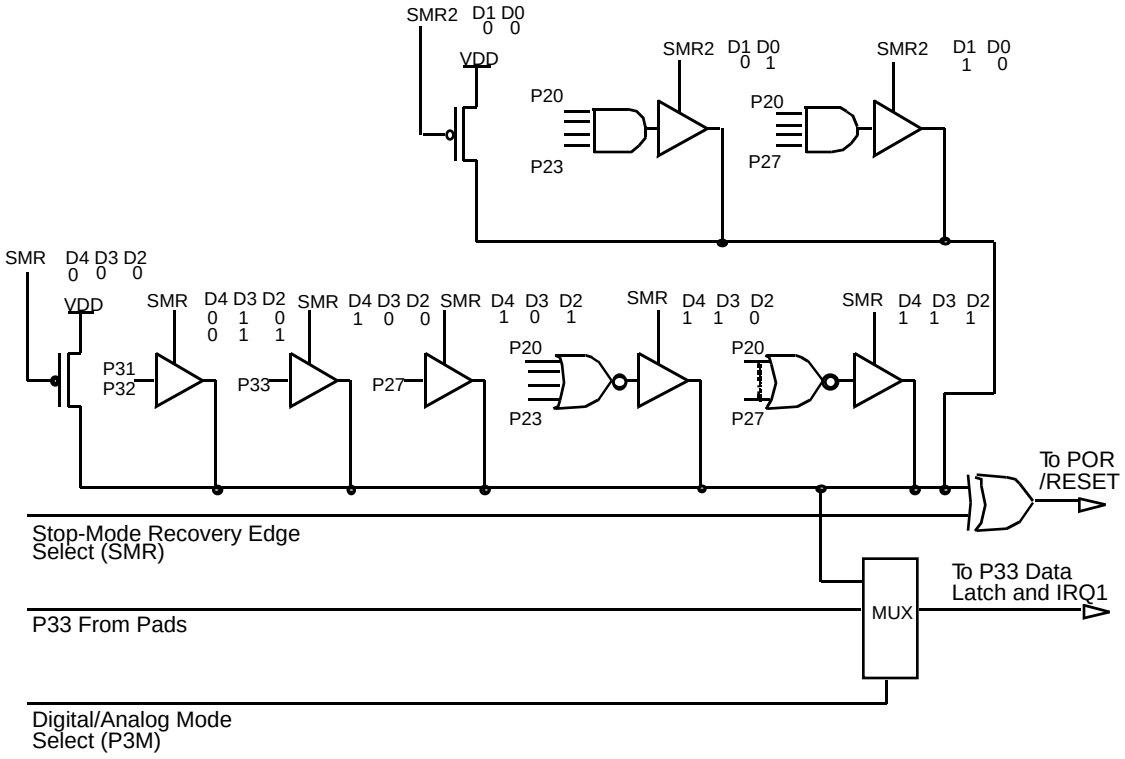

Figure 37. Stop-Mode Recovery Source