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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316sec

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

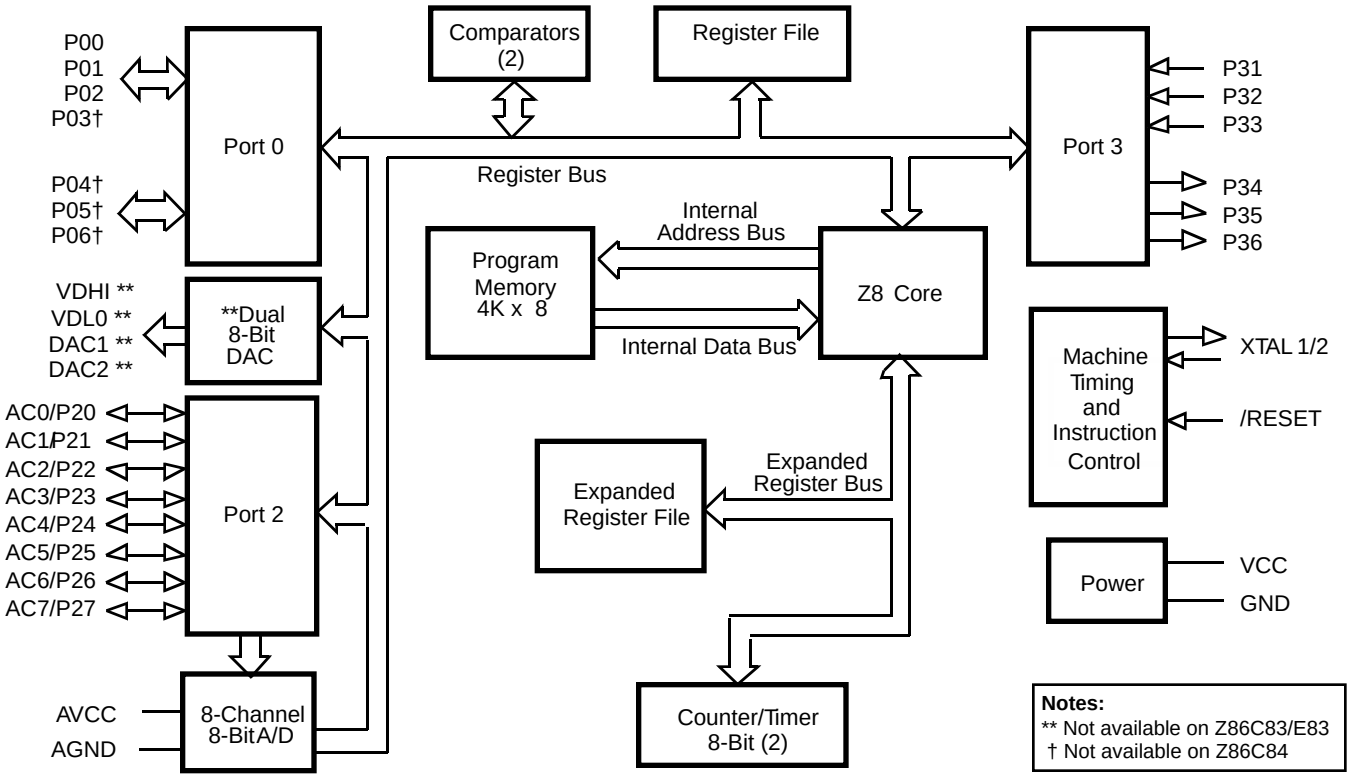


Figure 1. Z86C83/C84/E83 Functional Block Diagram

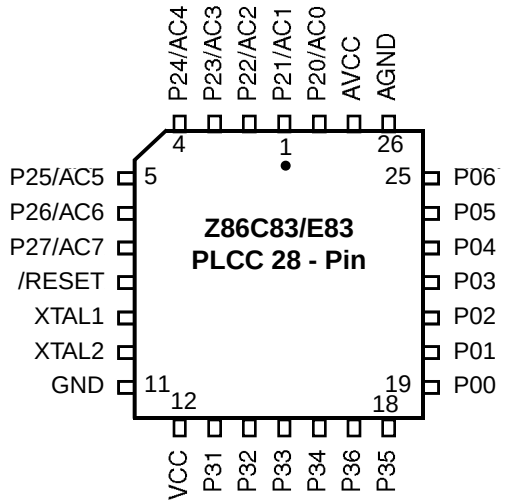


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

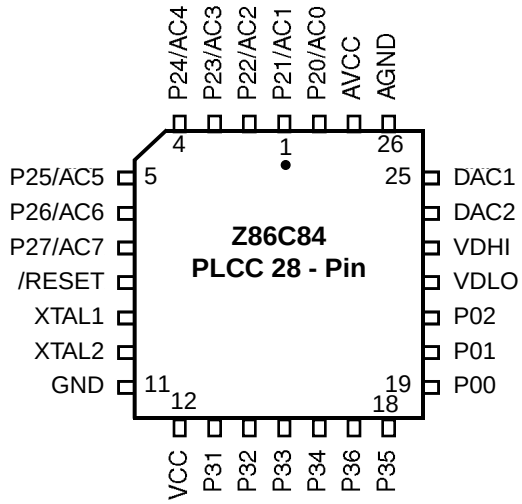


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

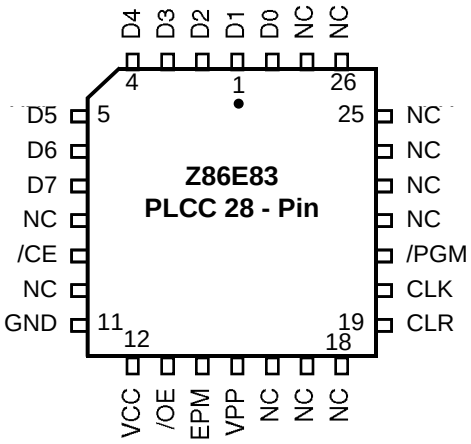


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 8).

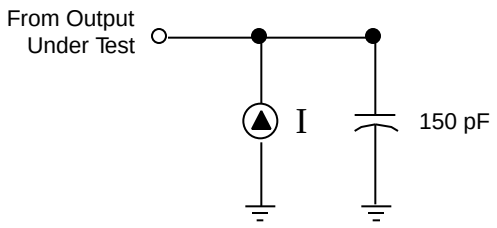


Figure 8. Test Load Diagram

V_{DD} SPECIFICATION

V_{DD} = 3.5V to 5.5V (Z86E83 only at 0° C to 70° C)

V_{DD} = 3.0V to 5.5V (Z86C83/C84)

V_{DD} = 4.5V to 5.5V (Z86E83 only at -40° C to 105° C)

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	15 pF
I/O capacitance	0	15 pF

DC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only

Sym	Parameter	V_{CC} Note 3	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC} -0.4		V_{CC} -0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC} -0.4		V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OL} = +10 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	1,4
		5.5V		25		25	20	mA	@ 16 MHz	1,4
		5.0V		7		7	3	mA	@ 3.58 MHz	1,4,15
		5.5V		10		10	5	mA	@ 8 MHz	1,4,15

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2) For Z86E83 Only

No	Symbol	Parameter	V_{CC} Note 6	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		15	ns	1
			5.5V		15		15	ns	1
3	TwC	Input Clock Width	3.5V	41		31		ms	1
			5.5V	41		31		ns	1
4	TwTinL	Timer Input Low Width	3.5V	100		100		ms	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1
	TfTin		5.5V		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3
			5.5V	5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12		12		ns	
			5.5V	12		12		ns	
11	Tost	Oscillator Start-up Time	3.5V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time					**WDTMR**	**Reg**	**D1,D0**
			5.5V	6.25		6.25		ms	0,0,[7]
			5.5V	12.5		12.5		ms	0,1,[7]
			5.5V	25		25		ms	1,0,[7]
			5.5V	100		100		ms	1,1,[7]
13	T_{POR}	Power On Reset Delay	3.5V	7	24	7	25	ms	7
			5.5V	3	13	3	14	ms	7

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. Using internal on-board RC oscillator.

For Z86C84 Only

Table 4. D/A Converter Electrical Characteristics
V_{CC} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	3.0	3.3	3.6	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 3 volts	1.5	1.8	2.1	Volts
VDLO range at 3 volts	0.2	0.5	0.8	Volts
VDHI–VDLO, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 3.0V – 3.6V
Temp: 0–70°C

For Z86C84 Only

Table 5. D/A Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0†	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 5 volts	2.6		3.5	Volts
VDLO range at 5V volts	0.8		1.7	Volts
VDHI–VDLO, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 4.5V - 5.5V
Temp: 0-70°C
† The C86C84 Emulator has maximum setting time of 20 µsec. (10 µsec. typical).

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

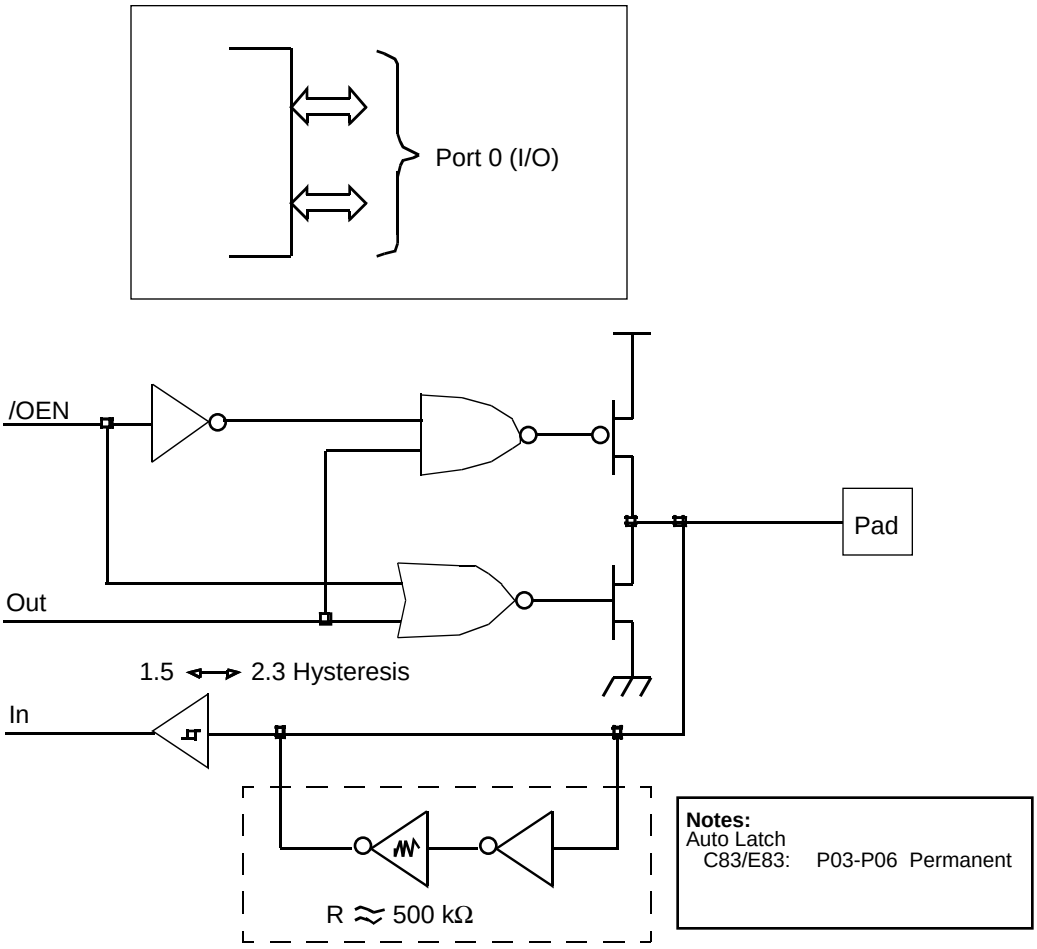


Figure 10. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20) Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port and an 8-channel muxed input to the 8-bit ADC. When configured as a digital input, by programming the Port2 Mode register, the Port 2 register can be evaluated to read digital data applied to Port 2, or the ADC result register can be read to evaluate the analog signals applied to Port 2 after configuring the ADC Control Registers. The direction of each of the eight Port 2 I/O lines can be configured individually (Figure 11).

In addition, all four versions of the device provide the capability of connecting 10K (±20%) pull-up resistors to each of the Port 2 I/O lines individually. The pull-ups are connected when activated through software control of P2RES register (Figure 67) when the corresponding Port 2 pin is configured to be an input. The pull-up resistor of a Port 2 I/O line is automatically disabled when the corresponding I/O is an output, regardless of the state of the corresponding P2RES bit value.

Note: The Z86C83/C84 Emulator does not emulate the P2RES Register. Selection of the pull-ups are done via jumper settings on the emulator.

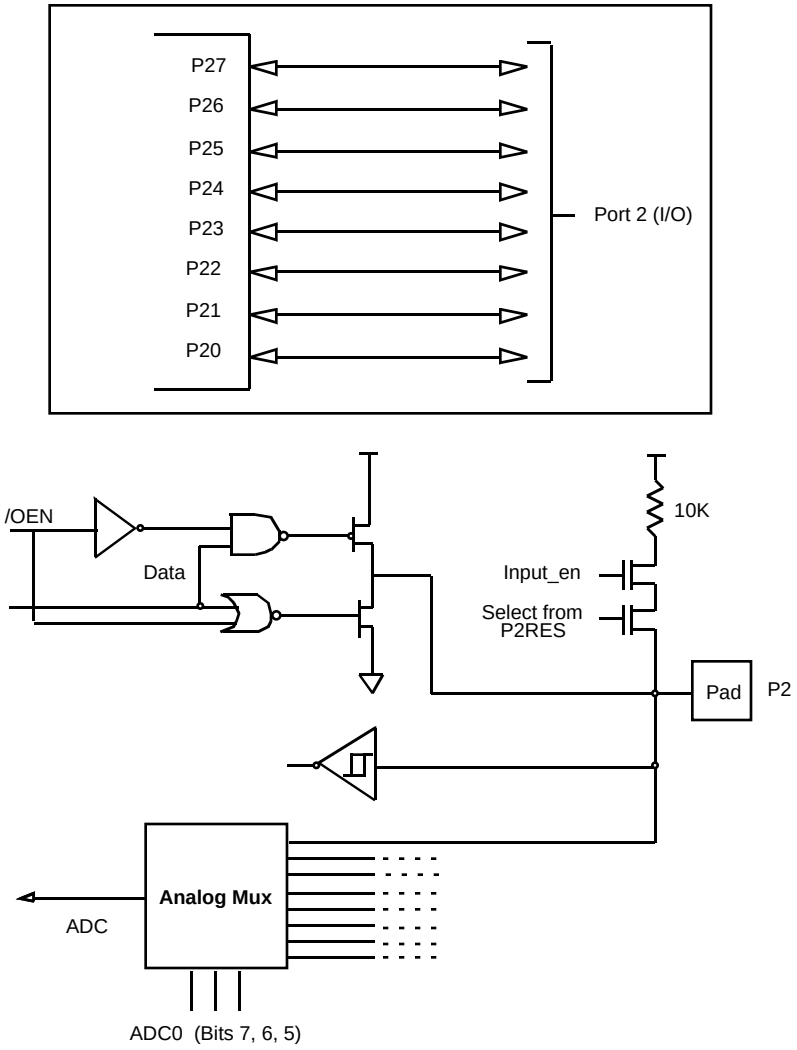


Figure 11. Port 2 Configuration

FUNCTIONAL DESCRIPTION

RESET. (Input, Active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) Reset, or external reset. During POR, and WDT Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. After the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000C (hex), 5-10 TpC cycles after the RST is released. For POR, the reset output time is T_{POR}.

Program Memory. C83/C84/E83/E84 can address up to 4 KB of internal Program Memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 4095 consist of on-chip, mask-programmed ROM.

ROM Protect. The 4 KB of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents from an external program outside the ROM.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 16). These register banks are known as the Expanded Register File (ERF). Bits 3-0 of the Register Pointer (RP) select the active ERF bank. Bits 7-4 of register RP select the working register group (Figure 16). Four system configuration registers reside in the ERF address space in Bank F and eight registers reside in Bank C. The rest of the ERF addressing space is not physically implemented, and is open for future expansion.

Note: When using Zilog's Cross Assembler version 2.1 or earlier, use the LD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

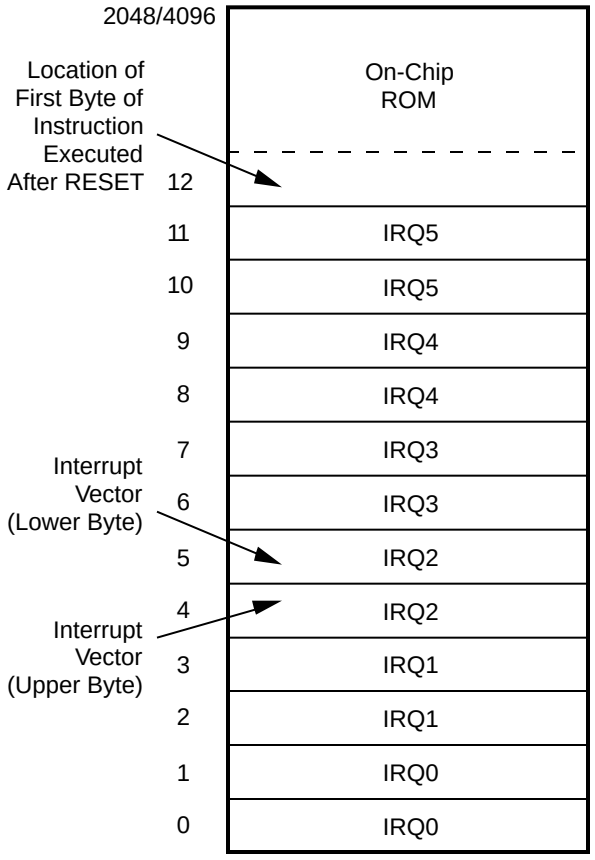


Figure 15. Program Memory Map

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

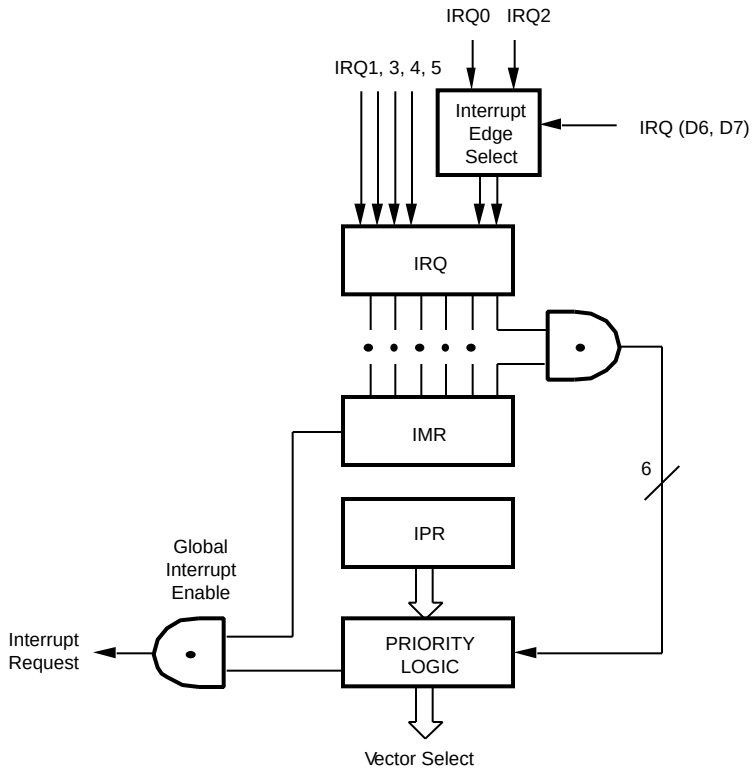


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 12.

Table 12. IRQ Register

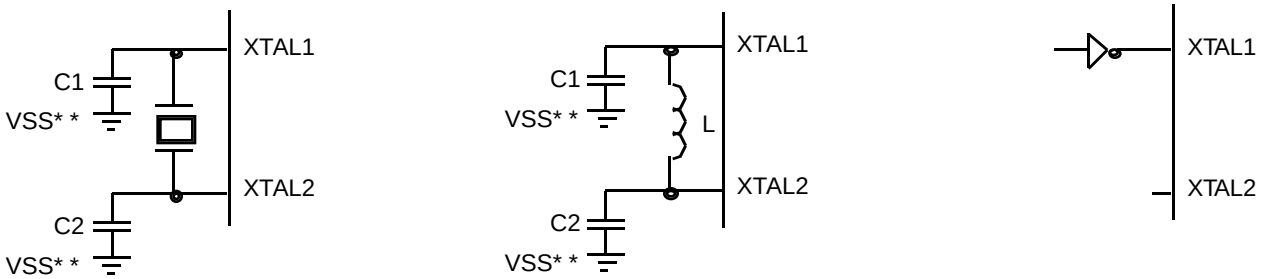
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when clocking from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator (Figure 21).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 21. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Analog-to-Digital Converter

The Analog-to-Digital (ADC) is an 8-bit half flash converter that uses two reference resistor ladders for its upper 4 bits (MSBs) and lower 4 bits (LSBs) conversion. Two reference voltage pins, AV_{CC} and A_{GND}, are provided for external reference voltage supplies. During the sampling period from one of the eight channel inputs, the converter is also being auto-zeroed before starting the conversion. The conversion time is dependent on the internal clock frequency. The minimum conversion time is 35 x SCLK (see Figure 22).

The ADC is controlled by the Z8 and its three registers (two Control and one Result) are mapped into the Extended Register File. A conversion can be initiated by writing to the ADC Control Register 0 after the ADC Control Register 1 is configured.

The start command is implemented in such a way as to begin a conversion at any time, if a conversion is in progress and a new start command is received, then the conversion in progress will be aborted and a new conversion will be initiated. This allows the programmed values to be changed without affecting a conversion-in-progress. The new values will take effect only after a new start command is received.

The ADC can be disabled (for low power) or enabled by a Control Register bit.

Though the ADC will function for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time may also take slightly longer due to smaller input signals.

ADC Calibration Offset

Specially matched resistors are program-enabled to allow 35 percent or 50 percent offset from A_{GND}. They may selectively enable these resistors to offset the A_{GND} by 50 percent (2.5V to 5V) or 35 percent (1.75V to 5V) thereby allowing the 8-bit ADC across a narrower voltage range. This will allow significant resolution improvement within the reduced voltage range.

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND.

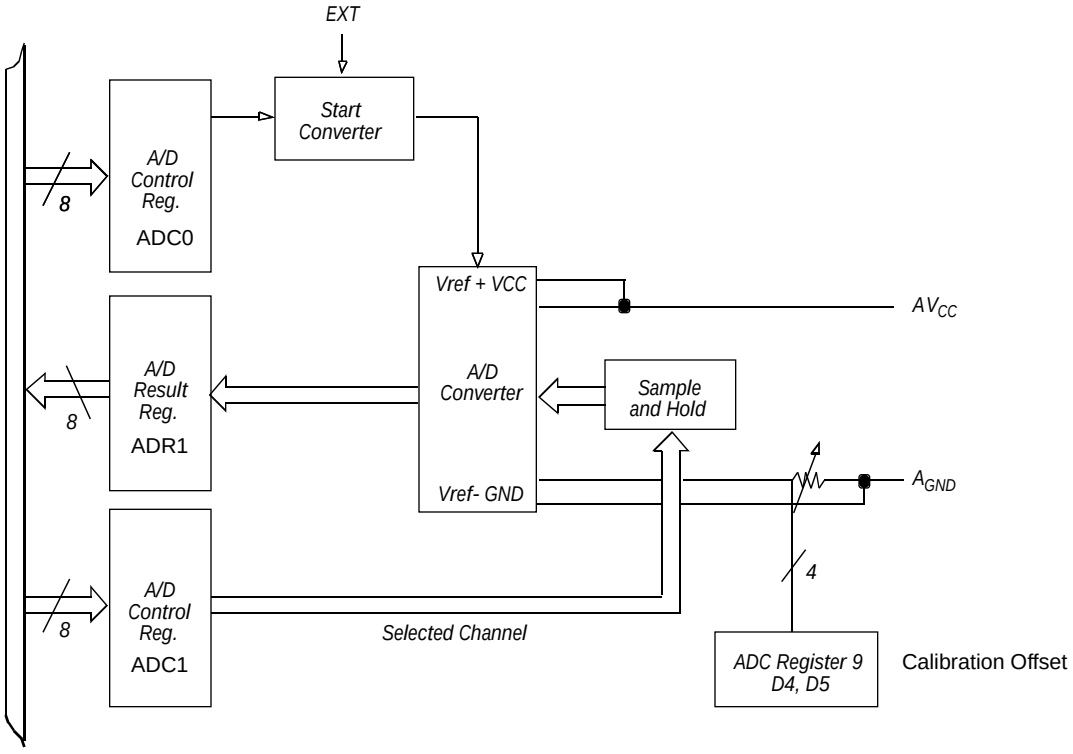


Figure 22. ADC Architecture

FUNCTIONAL DESCRIPTION (Continued)

Figure 27 shows the input circuit of the ADC. When conversion starts the analog input voltage is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Effectively, shunting 31 parallel internal resistance of the analog switches and simultaneously charging 31 parallel 0.5 pF capacitors, which is equivalent to seeing a 400 Ohms input impedance in parallel with a 16 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. For input source resistances up to 2 Kohms can be used under normal operating condition without any degradation of the input settling time. For larger input source resistance, increasing conversion cycle time or adding a capacitor to the input may be required to compensate the input settling time problem.

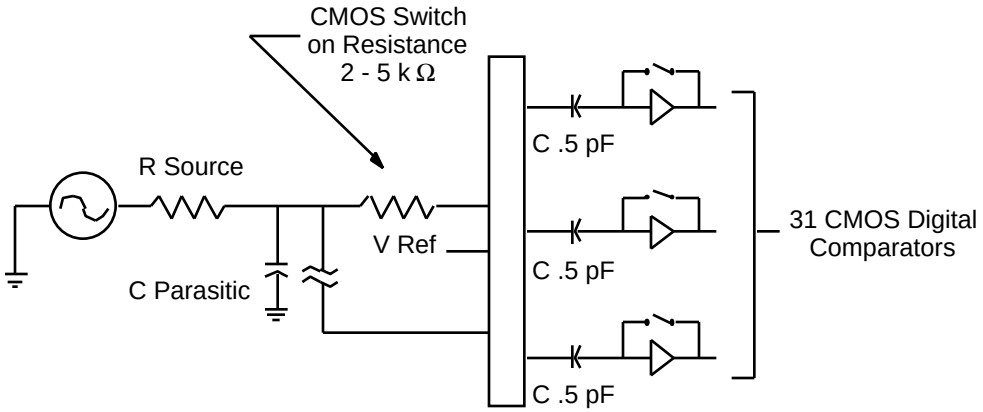


Figure 27. Input Impedance of ADC

Typical Z8 A/D Conversion Sequence

3. Set the register pointer to Extended Bank (C), that is, SRP #%0C instruction.

4. Next, set ADE flag by loading ADC1 Control Register Bank (C) Register 9, bit 7. Also, load bits 0-4 of this same register to select a AV_{CC} or A_{GND} offset value. A precision voltage divider connected to the A/D resistive ladder can offset conversion dynamic range to specified limits within the AV_{CC} and A_{GND} limits. By loading Bank (C) Register 9, bits 0-4, with the appropriate value it is possible to select from these groups:

   a. No Offset. The Converter Dynamic range is from 0V to 5.0V for AV_{CC} = 5.0V.

   b. 35 Percent A_{GND} Offset. The Converter Dynamic range is 1.75V - 5.0V for AV_{CC} = 5.0V.

   c. 50 Percent A_{GND} Offset. The Converter Dynamic range is 2.5V - 5.0V for AV_{CC} = 5.0V.

5. Select one of the eight A/D inputs for conversion by loading Bank (C) Register 8 with the desired attributes: Bits 0 - 2 select an A/D input, bits 3 and 4 select A/D conversion (or digital port I/O).

6. Set Bank (C) Register 8, bit 3 to enable A/D conversion. (This flag can be set concurrently with step 3.) This flag is automatically reset when the A/D conversion is completed, so a bit test can be performed to determine A/D readiness if necessary.

7. Read the A/D result in Bank (C) Register A. Please note that the A/D result is not valid (indeterminate) unless ADE flag (Register 9, bit 7) was previously set, otherwise A/D converter output is tri-stated.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

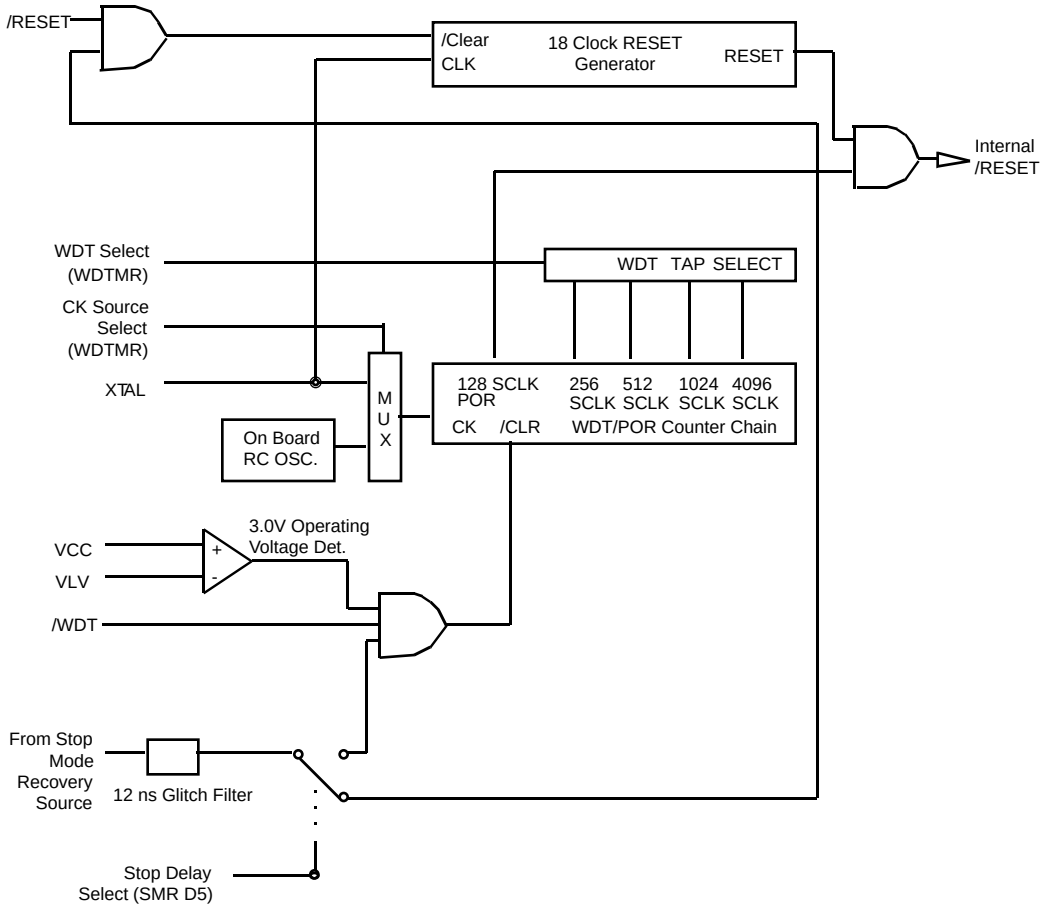


Figure 38. Resets and WDT

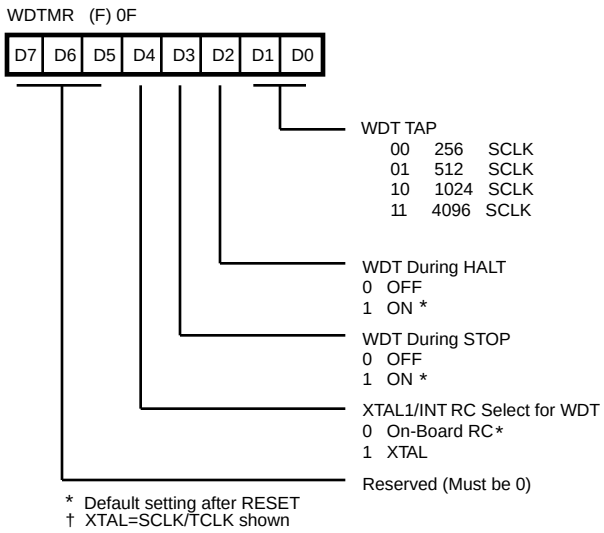


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 15.

Table 15. WDT Time Select (Min. @ 5.0V)

D1	D0	Time-Out of Internal RC OSC	Time-Out of SCLK Clock
0	0	6.25 ms min	256 SCLK
0	1	12.5 ms min	512 SCLK
1	0	25 ms min	1024 SCLK
1	1	100 ms min	4096 SCLK

Note: The minimum time shown is for V_{CC} @ 5.0V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. The default is "1".

Note: If WDT is permanently selected (always ON mode), the WDT will continue to run even if set not to run in STOP or HALT Mode.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A "1" indicates active during STOP. The default is "1". If bits D3 and D4 are both set to "1", the WDT only, is driven by the external clock during STOP Mode.

Notes:

1. If WDT is permanently selected (always ON mode) using internal on-board RC oscillator, the WDT will continue to run even if set not to run in STOP or HALT Mode.

2. WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a "1", the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. If the XTAL1 pin is selected as the oscillator source for the WDT, during STOP Mode, the oscillator will be stopped and the WDT will not run. This is true even if the WDT is selected to run during STOP Mode.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

ROM Protect. ROM Protect is mask or OTP bit-programmable. It is selected by the customer at the time the ROM code is submitted.

ROM Mask Selectable Options

There are two ROM mask options that must be selected at the time the ROM mask is ordered (ROM code submitted) for the Z86C83/C84 and three Z86E83 OTP bit options.

Table 16. Selectable Options

Option	Selection
Permanent WDT	Yes/No
ROM Protect	Yes/No
EPROM/TEST Mode Disable*	Yes/No

Note:
*For Z86E83 only
EPROM/TEST Mode Disable - On the Z86E83, the user can permanently disable entry into EPROM Mode and TEST Mode by programming this bit.

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