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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316ssc

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

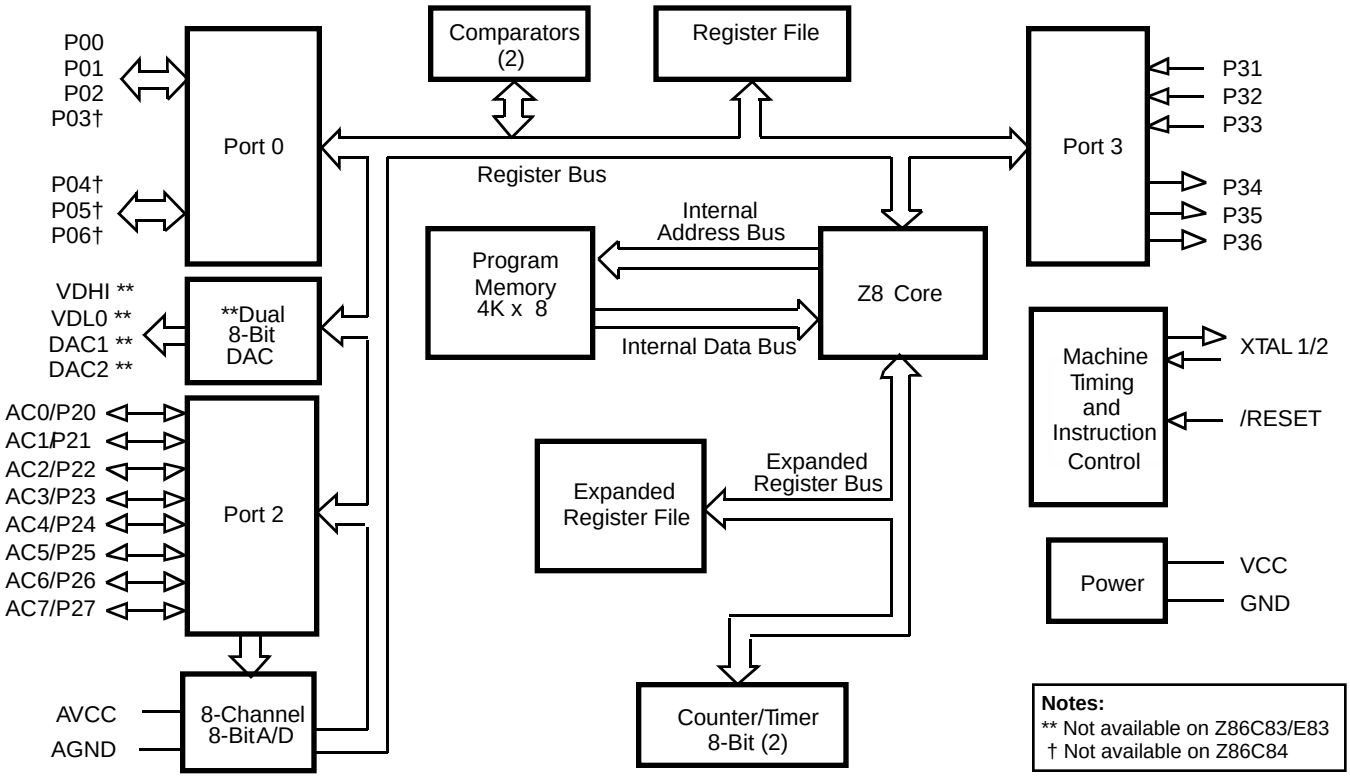


Figure 1. Z86C83/C84/E83 Functional Block Diagram

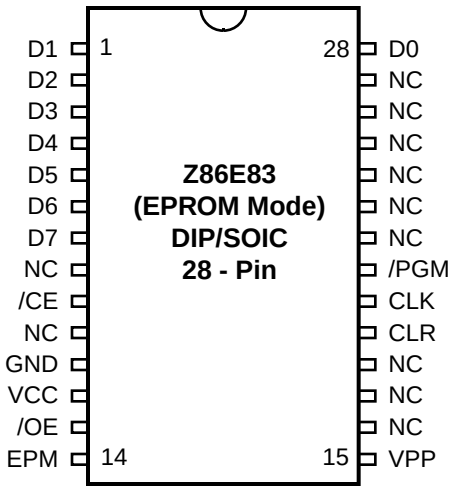


Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

For Z86E83 Only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	Max	T_A = -40° C to +105° C Min	Max	Typical [13] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Ouput High Voltage	3.5V	V_{CC}-0.4				3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.5V		0.6			0.2	V	I_{OH} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OH} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2			0.3	V	I_{OH} = +6.0 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OH} = +10.0 mA	8
V_{RH}	Reset Input High Voltage	3.5V	0.8V_{CC}	V_{CC}			1.5	V		
		5.5V	0.8V_{CC}	V_{CC}	0.8V_{CC}	V_{CC}	2.1	V		
		3.5V	GND-0.3	0.2V_{CC}			1.1	V		
		5.5V	GND-0.3	0.2V_{CC}	GND-0.3	0.2V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25			10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V		-130			-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.5V		20			7	mA	@16 MHz	1,4
		5.5V		25		25	20	mA	@16 MHz	1,4
I_{CC1}	Standby Current (HALT Mode)	3.5V		4.5			2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		3.5V		3.4			1.5	mA	Clock divide by 16 @ 16 MHz	1,4
		5.5V		7.0		7.0	2.9	mA	Clock divide by 16 @ 16 MHz	1,4

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

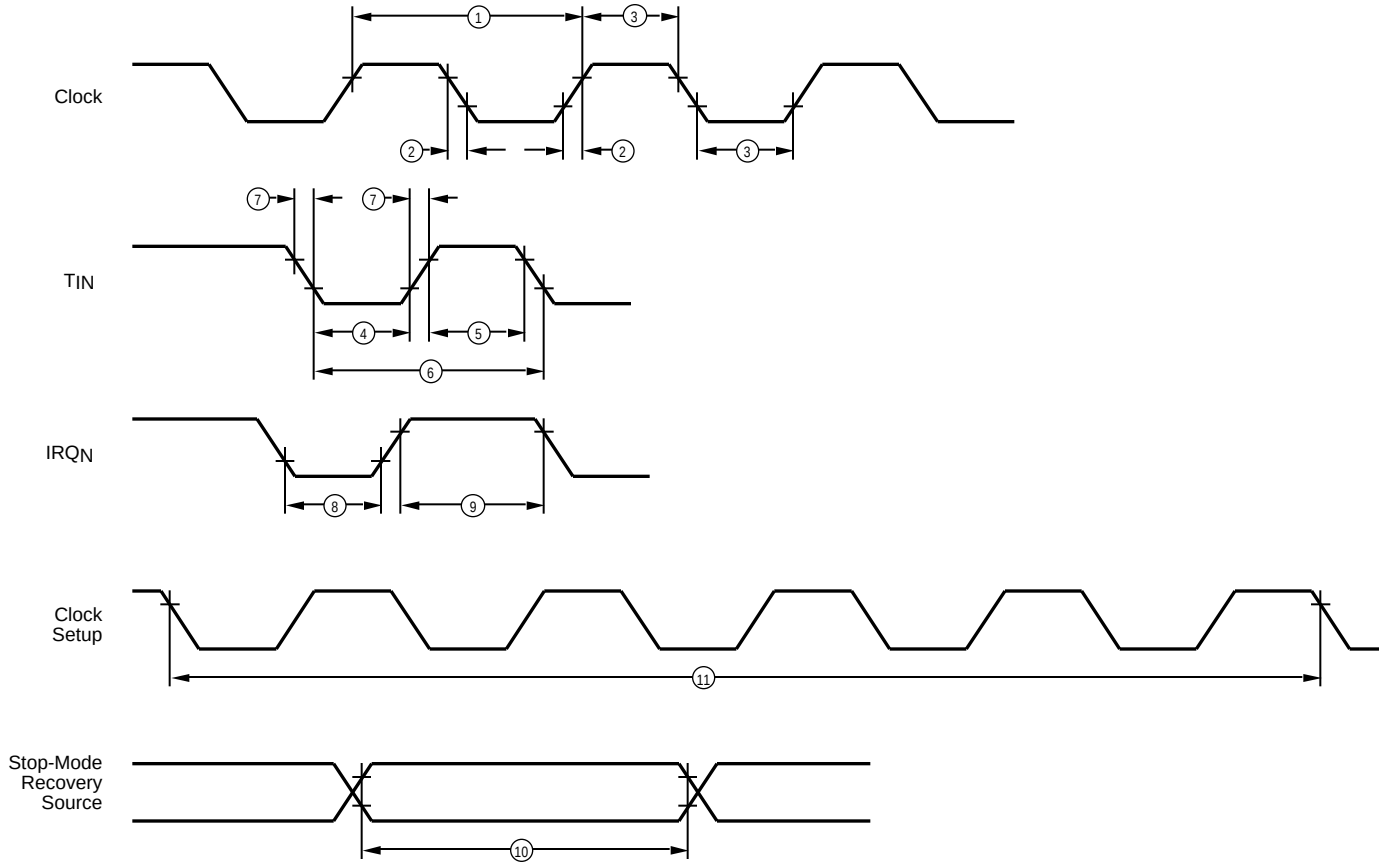


Figure 9. Additional Timing

PIN FUNCTIONS (Continued)

Port 2 (P27-P20) Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port and an 8-channel muxed input to the 8-bit ADC. When configured as a digital input, by programming the Port2 Mode register, the Port 2 register can be evaluated to read digital data applied to Port 2, or the ADC result register can be read to evaluate the analog signals applied to Port 2 after configuring the ADC Control Registers. The direction of each of the eight Port 2 I/O lines can be configured individually (Figure 11).

In addition, all four versions of the device provide the capability of connecting 10K (±20%) pull-up resistors to each of the Port 2 I/O lines individually. The pull-ups are connected when activated through software control of P2RES register (Figure 67) when the corresponding Port 2 pin is configured to be an input. The pull-up resistor of a Port 2 I/O line is automatically disabled when the corresponding I/O is an output, regardless of the state of the corresponding P2RES bit value.

Note: The Z86C83/C84 Emulator does not emulate the P2RES Register. Selection of the pull-ups are done via jumper settings on the emulator.

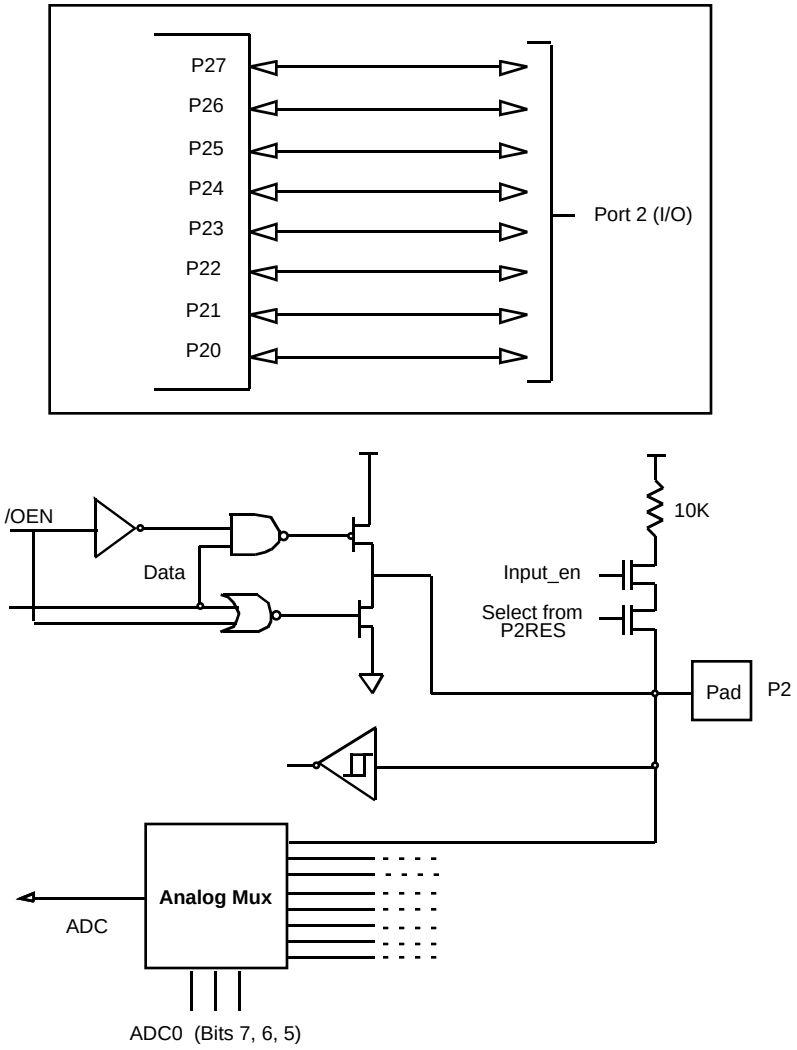


Figure 11. Port 2 Configuration

Port 3 (P36-P31) Port 3 is a 6-bit, CMOS-compatible port, with three fixed inputs (P33-P31) and three fixed outputs (P34-P36), configured under software control for Input/Output, Counter/Timers, interrupt, and port handshake. P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, and P36 are push-pull output lines (Figure 11). Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 3 is falling-edge interrupt input. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P31/P36 and P32/P35 (Table 10).

Port 3 also provides the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); timer input and output signals (T_{IN} and T_{OUT}).

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on CMOS inputs that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Pins 03, 04, 05, 06 have permanently enabled Auto Latches.

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. In Analog Mode, the internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR register. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In Digital Mode, P33 can be used as a Port 3 register input or IRQ1 source. P34 outputs the comparator outputs by software programming the PCON Register bit D0 to 1.

Note: When enabling/or disabling the analog mode, the following is recommended:

1. allow two NOP delays before reading the comparator output

2. disable interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

PIN FUNCTIONS (Continued)

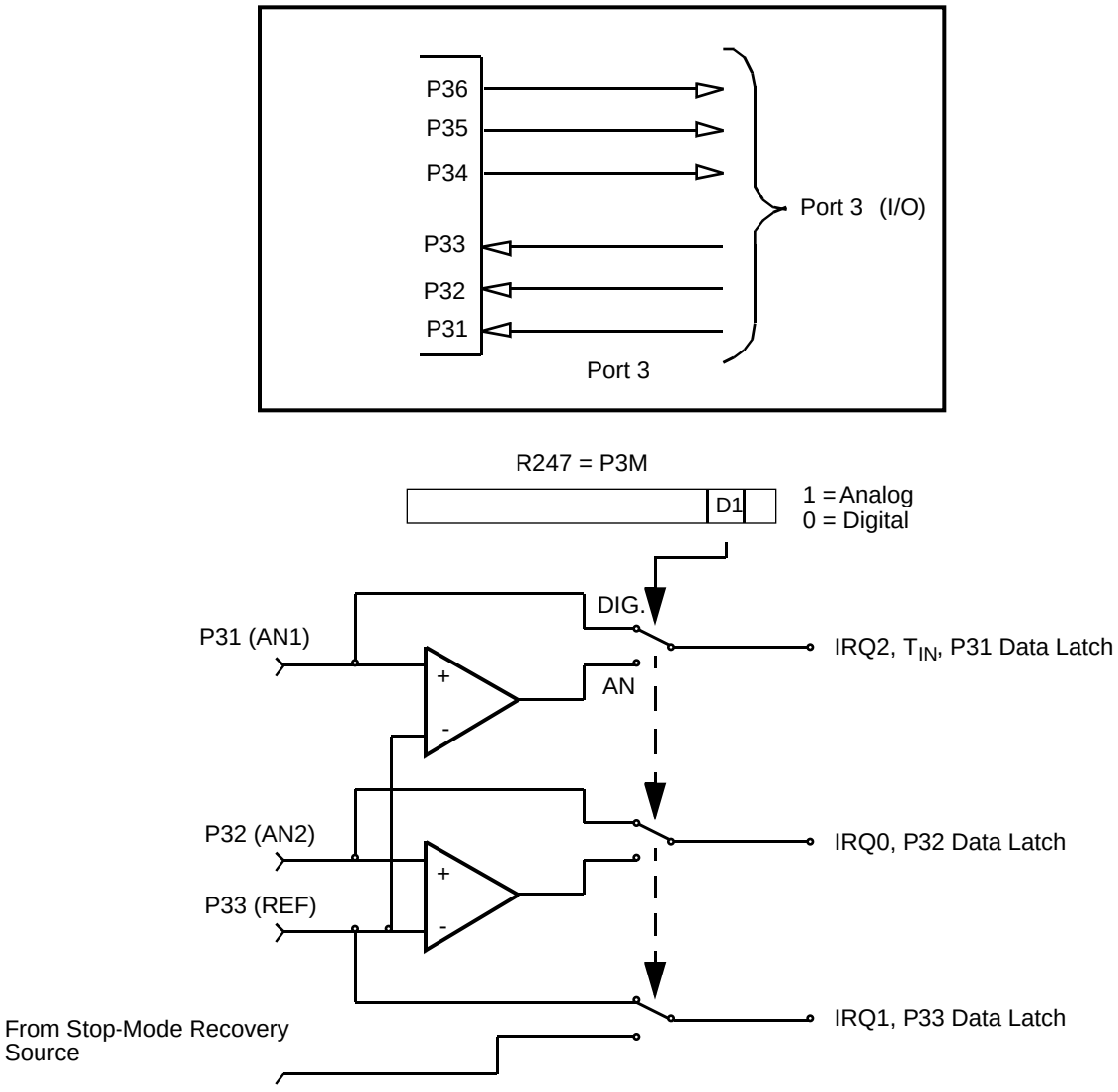


Figure 12. Port 3 Input Configuration

FUNCTIONAL DESCRIPTION

RESET. (Input, Active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) Reset, or external reset. During POR, and WDT Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. After the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000C (hex), 5-10 TpC cycles after the RST is released. For POR, the reset output time is T_{POR}.

Program Memory. C83/C84/E83/E84 can address up to 4 KB of internal Program Memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 4095 consist of on-chip, mask-programmed ROM.

ROM Protect. The 4 KB of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents from an external program outside the ROM.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 16). These register banks are known as the Expanded Register File (ERF). Bits 3-0 of the Register Pointer (RP) select the active ERF bank. Bits 7-4 of register RP select the working register group (Figure 16). Four system configuration registers reside in the ERF address space in Bank F and eight registers reside in Bank C. The rest of the ERF addressing space is not physically implemented, and is open for future expansion.

Note: When using Zilog's Cross Assembler version 2.1 or earlier, use the LD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

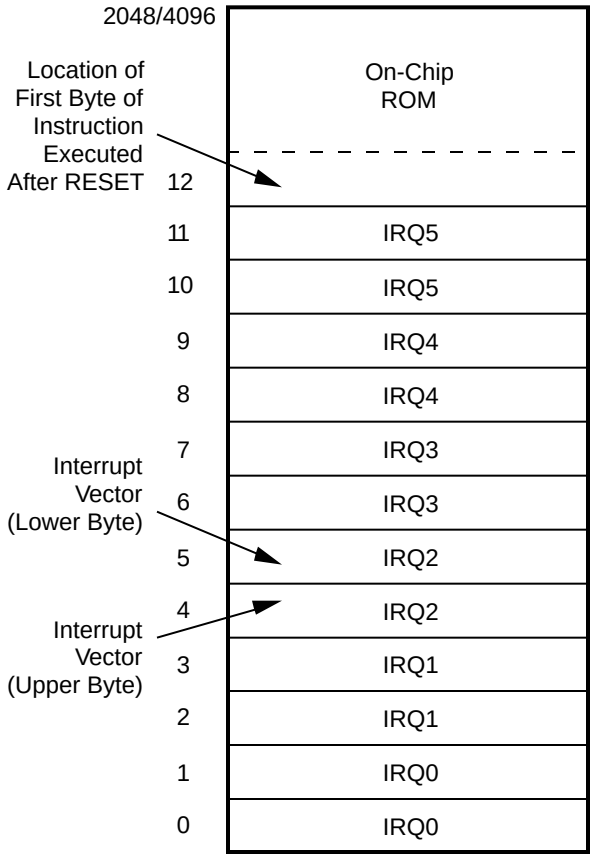


Figure 15. Program Memory Map

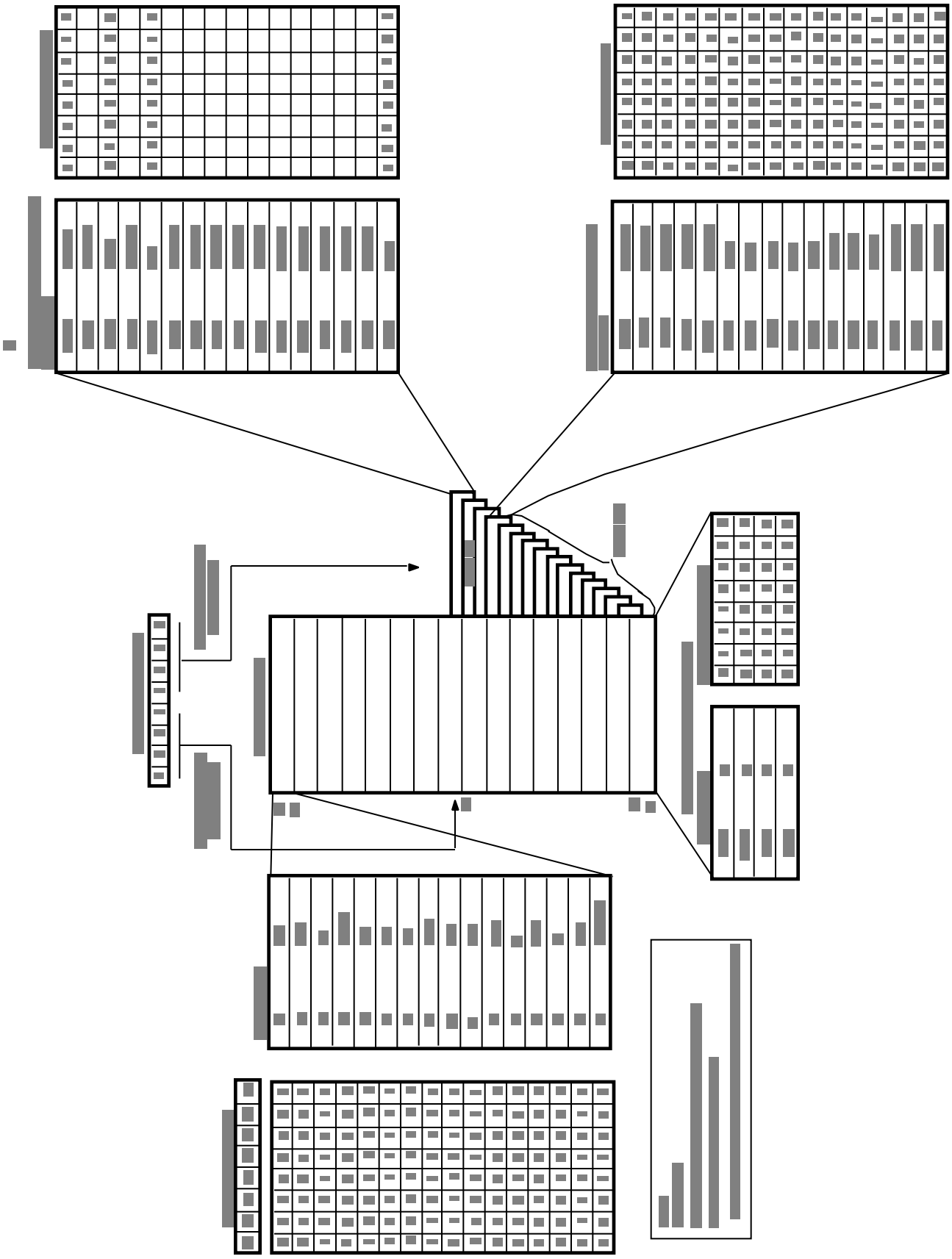


Figure 16. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

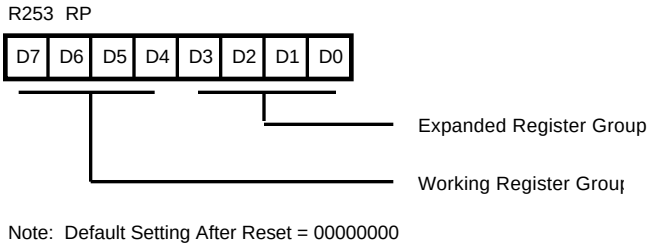


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

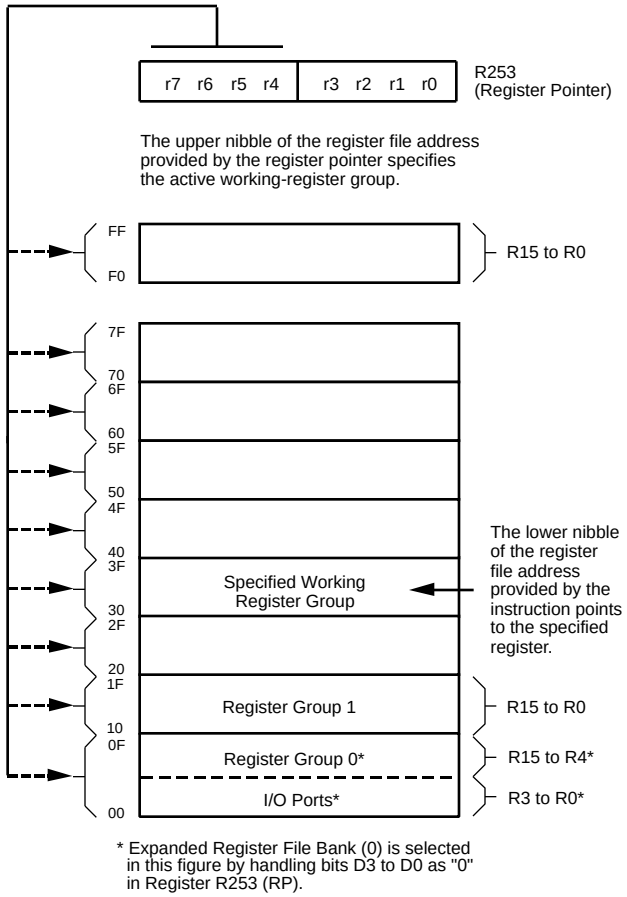


Figure 18. Register Pointer

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 12.

Table 12. IRQ Register

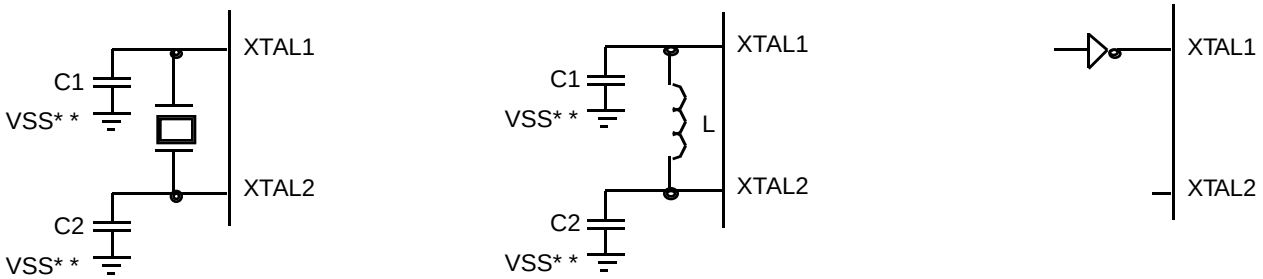
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when clocking from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator (Figure 21).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 21. Oscillator Configuration

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

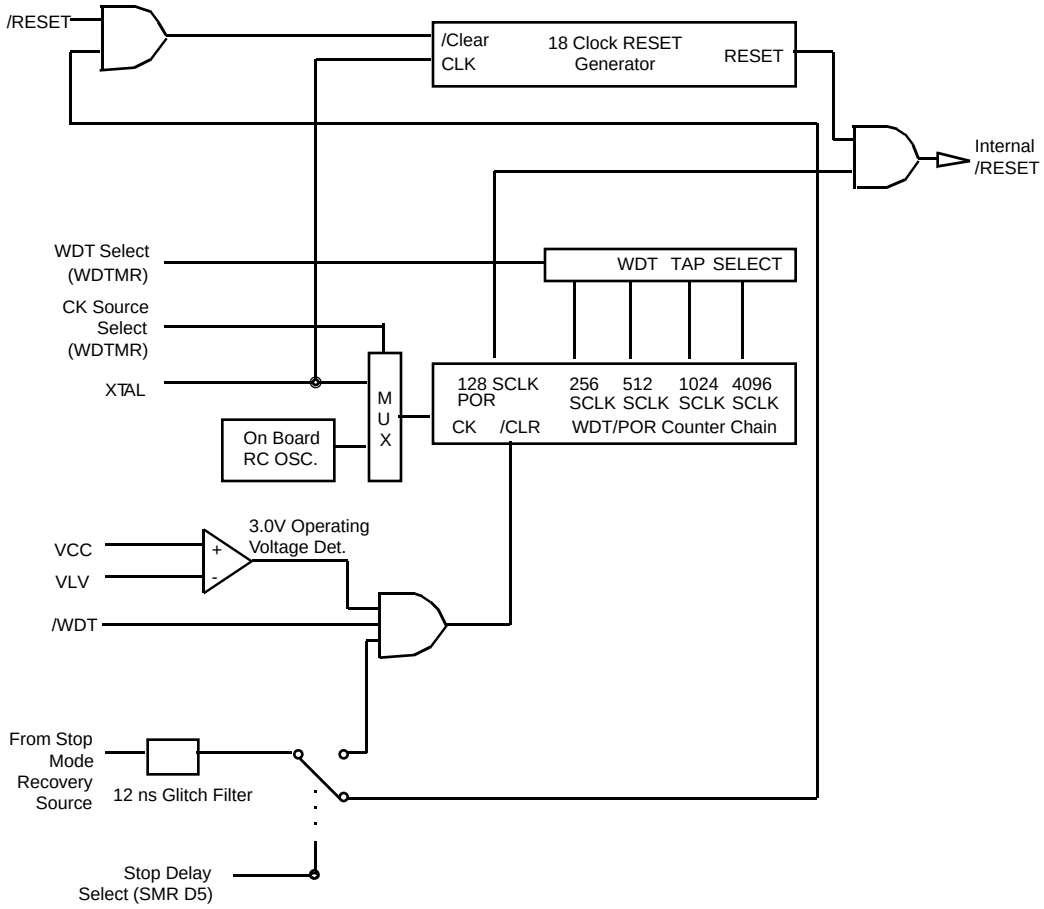


Figure 38. Resets and WDT

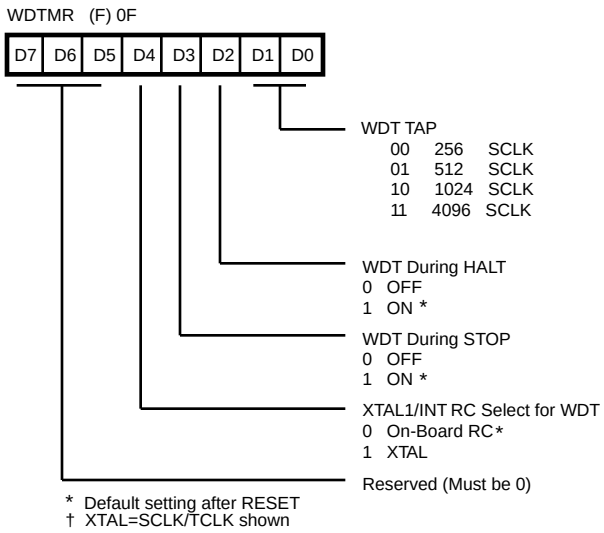


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 15.

Table 15. WDT Time Select (Min. @ 5.0V)

D1	D0	Time-Out of Internal RC OSC	Time-Out of SCLK Clock
0	0	6.25 ms min	256 SCLK
0	1	12.5 ms min	512 SCLK
1	0	25 ms min	1024 SCLK
1	1	100 ms min	4096 SCLK

Note: The minimum time shown is for V_{CC} @ 5.0V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. The default is "1".

Note: If WDT is permanently selected (always ON mode), the WDT will continue to run even if set not to run in STOP or HALT Mode.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A "1" indicates active during STOP. The default is "1". If bits D3 and D4 are both set to "1", the WDT only, is driven by the external clock during STOP Mode.

Notes:

1. If WDT is permanently selected (always ON mode) using internal on-board RC oscillator, the WDT will continue to run even if set not to run in STOP or HALT Mode.

2. WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a "1", the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. If the XTAL1 pin is selected as the oscillator source for the WDT, during STOP Mode, the oscillator will be stopped and the WDT will not run. This is true even if the WDT is selected to run during STOP Mode.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

ROM Protect. ROM Protect is mask or OTP bit-programmable. It is selected by the customer at the time the ROM code is submitted.

ROM Mask Selectable Options

There are two ROM mask options that must be selected at the time the ROM mask is ordered (ROM code submitted) for the Z86C83/C84 and three Z86E83 OTP bit options.

Table 16. Selectable Options

Option	Selection
Permanent WDT	Yes/No
ROM Protect	Yes/No
EPROM/TEST Mode Disable*	Yes/No

Note:
*For Z86E83 only
EPROM/TEST Mode Disable - On the Z86E83, the user can permanently disable entry into EPROM Mode and TEST Mode by programming this bit.

EXPANDED REGISTER FILE CONTROL REGISTERS (0C)

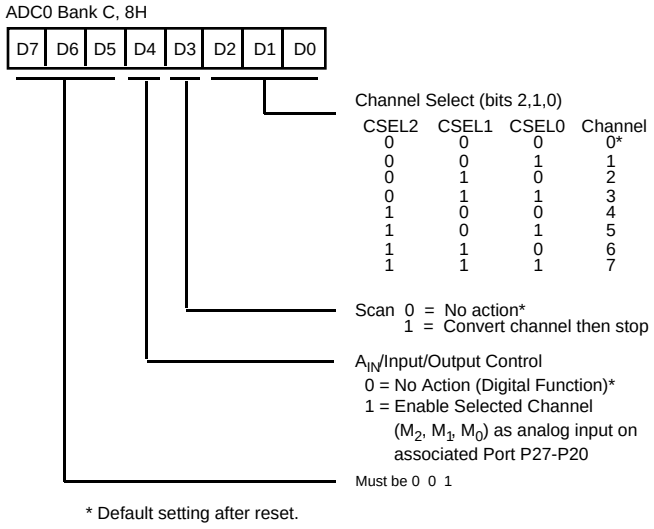


Figure 40. ADC Control Register 0 (Read/Write)

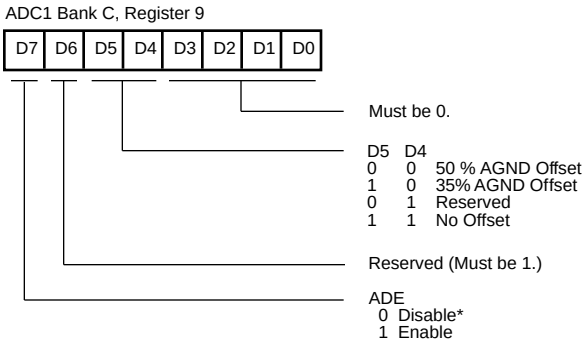


Figure 41. ADC Control Register 1 (Read/Write)

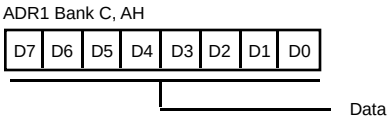


Figure 42. AD Result Register (Read Only)

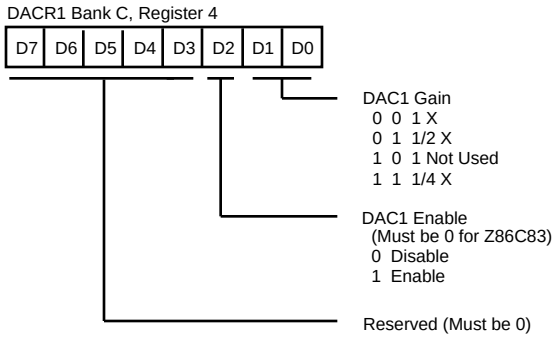


Figure 43. D/A 1 Control Register

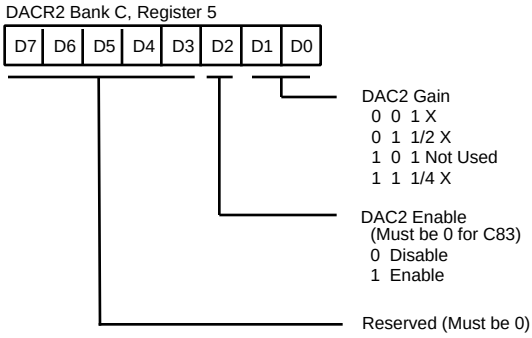


Figure 44. D/A 2 Control Register

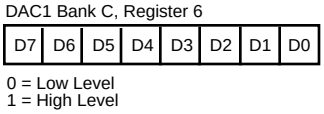


Figure 45. D/A 1 Data Register

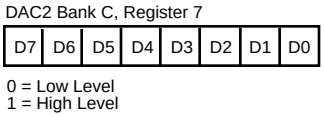


Figure 46. D/A 2 Data Register

Z8 CONTROL REGISTERS

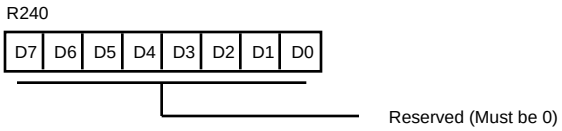


Figure 51. Reserved

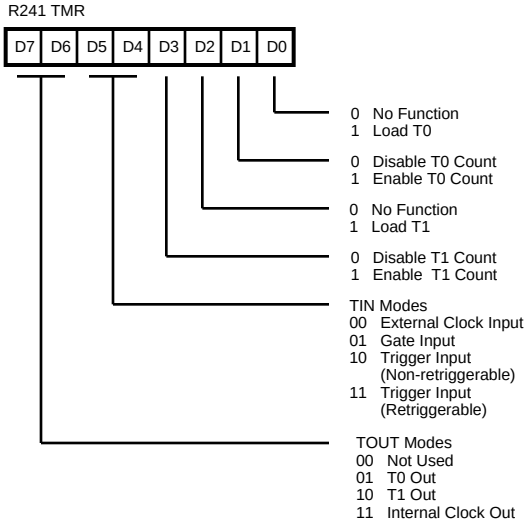


Figure 52. Timer Mode Register ($F1_H$: Read/Write)

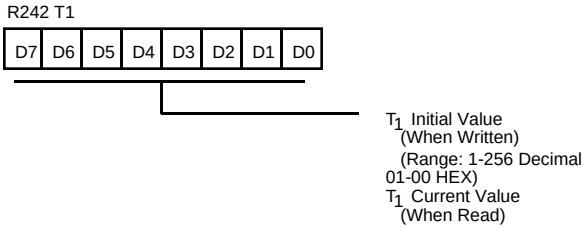


Figure 53. Counter/Timer 1 Register ($F2_H$: Read/Write)

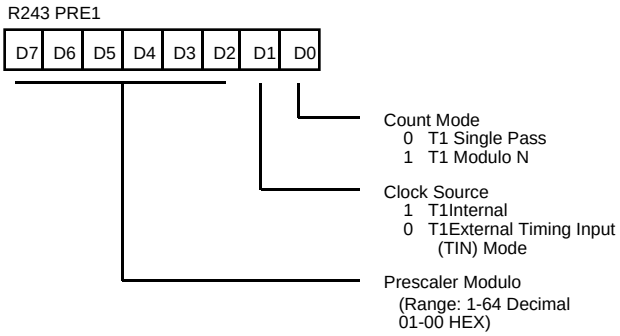


Figure 54. Prescaler 1 Register ($F3_H$: Write-Only)

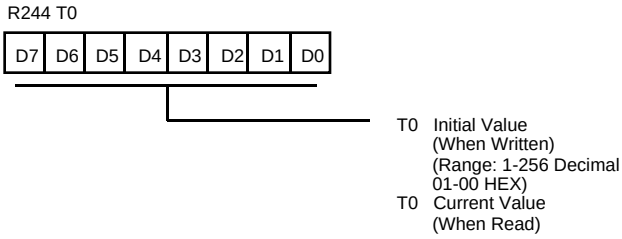


Figure 55. Counter/Timer 0 Register ($F4_H$: Read/Write)

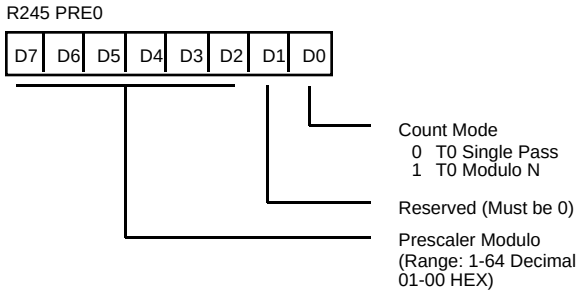


Figure 56. Prescaler 0 Register ($F5_H$: Write-Only)

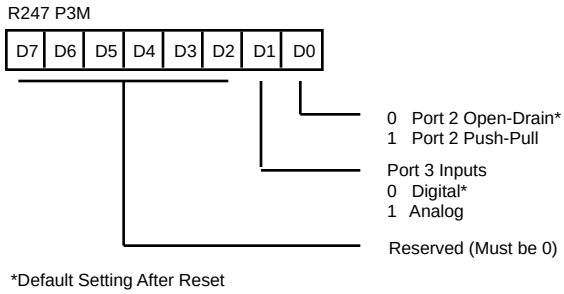


Figure 57. Port 3 Mode Register ($F7_H$: Write-Only)

Z8 CONTROL REGISTERS (Continued)

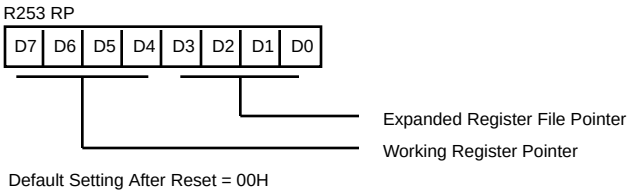


Figure 64. Register Pointer (F_{DH}: Read/Write)

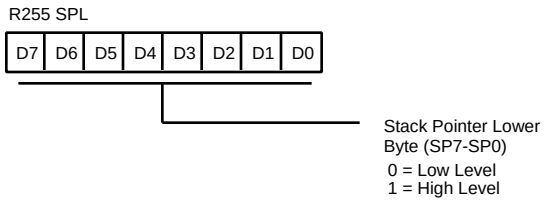


Figure 66. Stack Pointer (F_{FH}: Read/Write)

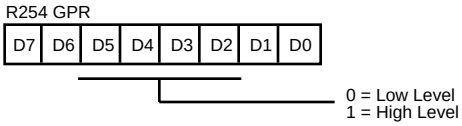


Figure 65. General-Purpose Register (F_{EH}: Read/Write)

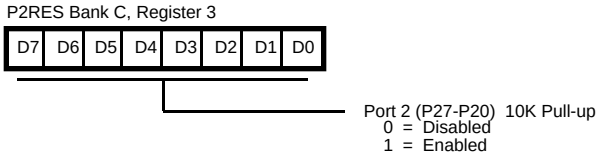
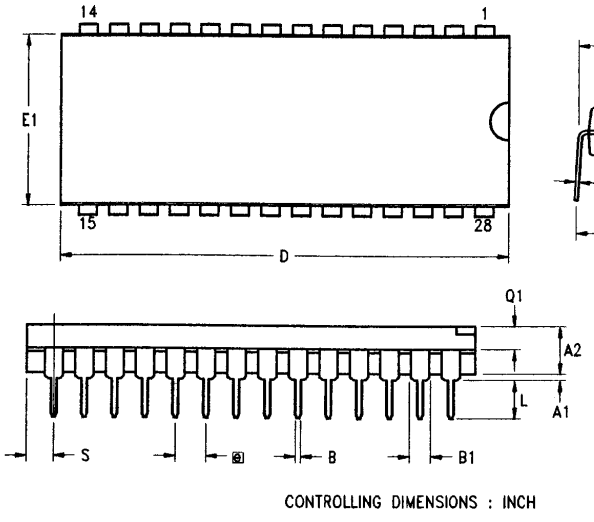


Figure 67. Port 2 Pull-up Register

PACKAGE INFORMATION



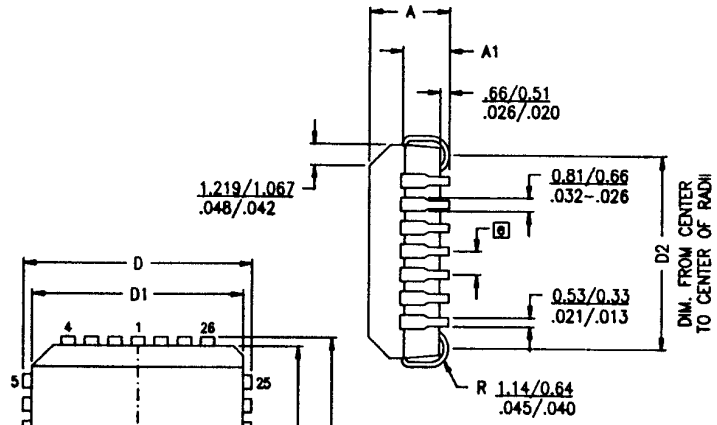
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
G	1.27 TYP		.050 TYP	

NOTES.
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 INCH.
3. DIMENSION : MM / INCH

Figure 70. 28-Pin PLCC Package Diagram