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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316ssc00tr

PIN DESCRIPTION

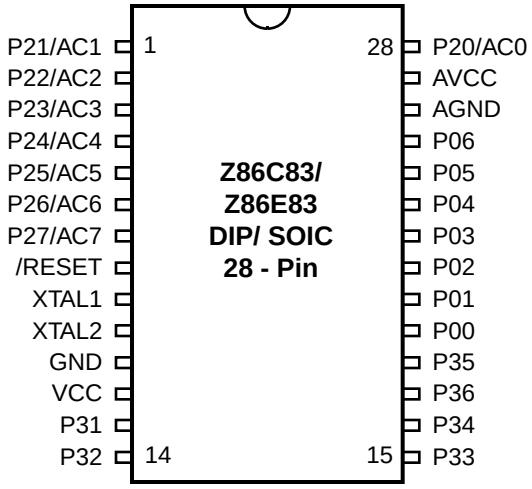


Figure 2. Z86C83 and Standard Mode Z86E83 28-Pin DIP and SOIC Pin Configuration*

Table 1. Z86C83 and Standard Mode Z86E83 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-25	P00-P06	Port 0, Bits 0-6	Input/Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP and SOIC Pin Description and Configuration are identical.

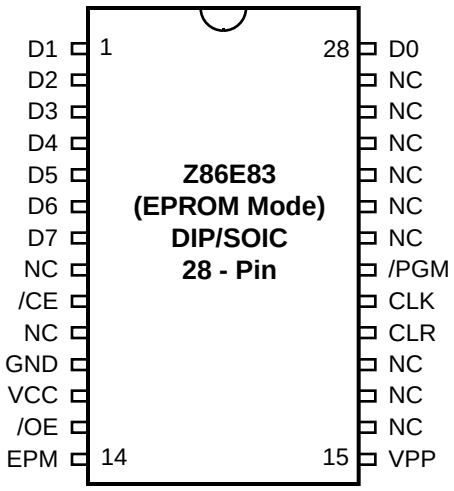


Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

AC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only. Low EMI Mode Only.

				T_A = 0°C to +70°C		T_A = -40° to +105°C			
				4 MHz		4 MHz			
No	**Symbol**	**Parameter**	**V_{CC} [6]**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		ns	1,7,8
			5.5V	3TpC		3TpC		ns	1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC		ns	1,3,7,8
			5.5V	3TpC		3TpC		ns	1,3,7,8
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		ns	1,2,7,8
			5.5V	3TpC		3TpC		ns	1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode
9. For LC oscillator and for oscillator driven by clock driver

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	T_A = 0° C to +70° C Max	T_A = -40° C to +105° C Min	T_A = -40° C to +105° C Max	Typical [13] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.5V		8			1	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.5V		500			310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
V_{ICR}	Input Common Mode	3.5V	0	V_{CC}-1.0V	0			V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.5V		8			5	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		15		20	11	µA	$0V<V_{IN}<V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V		-5			-3	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		-8		-10	-6	µA	$0V<V_{IN}<V_{CC}$	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max. Int. CLK Frequency	7

Notes:

1. Combined digital V_{CC} and analog AV_{CC} supply currents
2. GND = 0V
3. V_{CC} voltage specification of 3.5V guarantees 3.5V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V
4. All outputs unloaded, I/O pins floating, inputs at rail
5. CL1 = CL2 = 100 pF
6. Same as note [4] except inputs at V_{CC}
7. The V_{LV} increases as the temperature decreases
8. Standard Mode (not Low EMI)
9. Auto Latch (mask option) selected
10. For analog comparator, inputs when analog comparators are enabled
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating
12. Excludes clock pins
13. Typicals are at V_{CC} = 3.5V and 5.0V
14. Internal RC selected

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

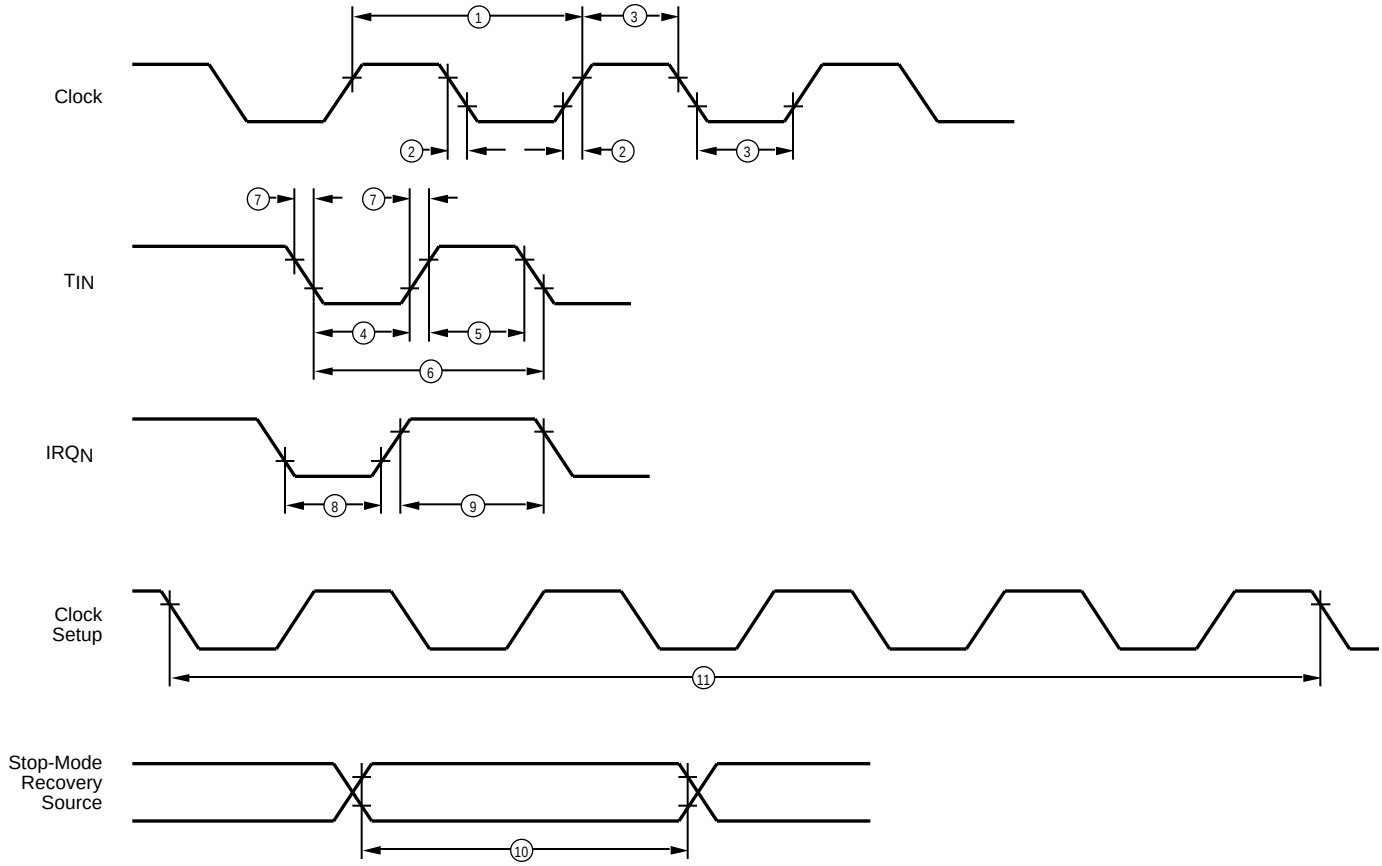


Figure 9. Additional Timing

For Z86C84 Only

Table 4. D/A Converter Electrical Characteristics
V_{CC} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	3.0	3.3	3.6	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 3 volts	1.5	1.8	2.1	Volts
VDLO range at 3 volts	0.2	0.5	0.8	Volts
VDHI–VDLO, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 3.0V – 3.6V
Temp: 0–70°C

For Z86C84 Only

Table 5. D/A Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0†	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 5 volts	2.6		3.5	Volts
VDLO range at 5V volts	0.8		1.7	Volts
VDHI–VDLO, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 4.5V - 5.5V
Temp: 0-70°C
† The C86C84 Emulator has maximum setting time of 20 µsec. (10 µsec. typical).

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

PIN FUNCTIONS

EPROM Programming Mode (E83 Only)

D7-D0. *Data Bus.* The data can be read from or written to the EPROM through the data bus.

Clock. *Address Clock.* This pin is a clock input. The internal address counter increases by one with one clock signal.

Clear. *Clear.* (active High). This pin resets the internal address counter at the High Level.

$V_{CC.}$ *Power Supply.* This pin must supply 5V during the EPROM Read Mode and 6V during other modes.

/CE. *Chip Enable* (active Low). This pin is active during EPROM Read, Program, and Program Verify Modes.

/OE. *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM. *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

$V_{PP.}$ *Program Voltage.* This pin supplies the program voltage.

/PGM. *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges above V_{cc}*** occur on the /RESET pin.

Processor operation of Z8 OTP devices may be affected by excessive noise surges on the VPP, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to /RESET, VPP, /EPM, /OE
- Adding a capacitor to the affected pin

Z86C83, Z86C84, and Standard Mode Z86E83

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC network or an external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC network to the on-chip oscillator output.

Port 0 P00-P06 (P03-P06 is not available on the Z86C84). Port 0 is a 7-bit, bidirectional, CMOS-compatible I/O port. These seven I/O lines can be nibble programmable as P00-P03 input/output and P04-P06 input/output, separately (Figure 10). All input buffers are Schmitt-triggered and output drivers are push-pull.

Port 0 Auto Latch. (P03-P06 has the Auto Latches permanently enabled). The Auto Latch provides valid CMOS Levels when P03-P06 are selected as inputs and not externally driven. It is impossible to determine if a non-driven input is 1 or 0, however; the Auto Latch will sense the input condition and drive a valid CMOS level, thereby eliminating a floating mode that could cause excessive current.

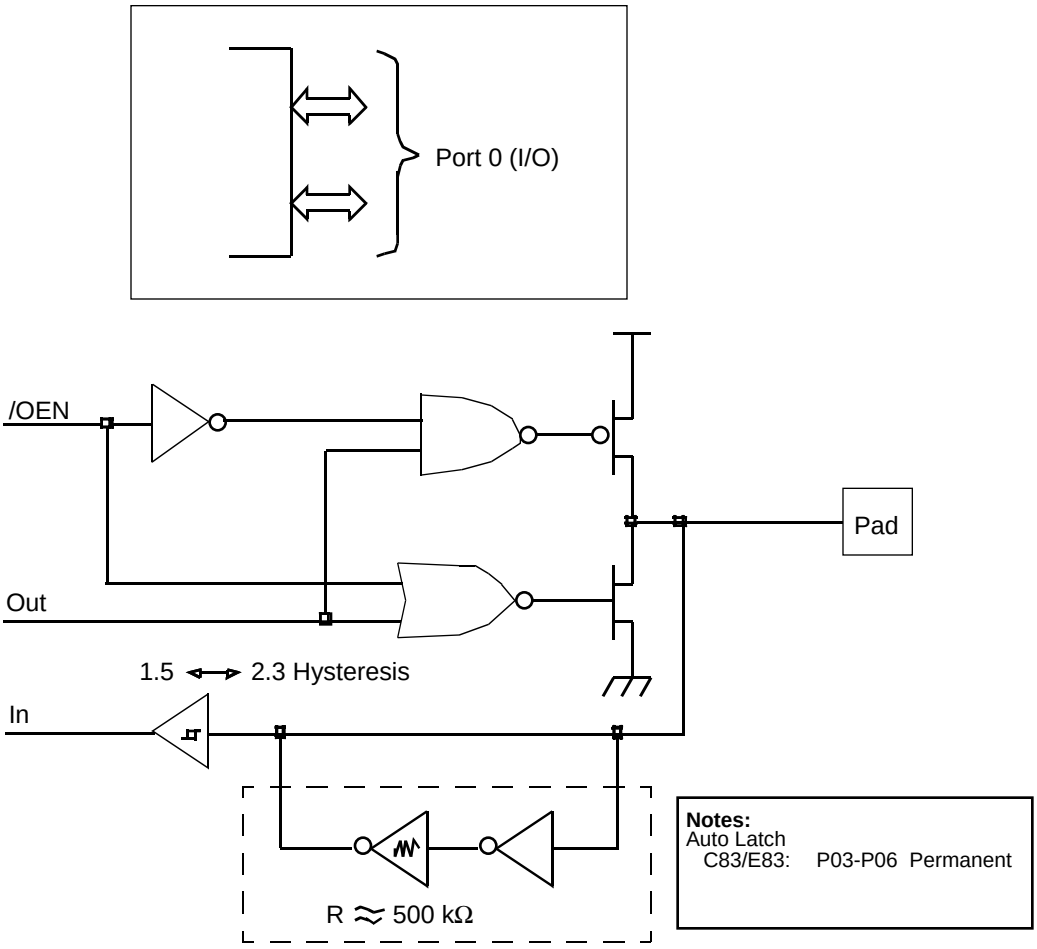


Figure 10. Port 0 Configuration

Port Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 13).

Bit 0 multiplexes comparator AN1 Output at P34. A "1" in this location brings the comparator output to P34 (Figure 14), and a "0" puts P34 into its standard I/O configuration.

Note: Only comparator output AN1 is multiplexed to a Port 3 output. Comparator AN2 output is not connected to any pins. Note that the PCON Register is reset upon the occurrence of a WDT RESET (not in STOP Mode), and Power-On Reset (POR).

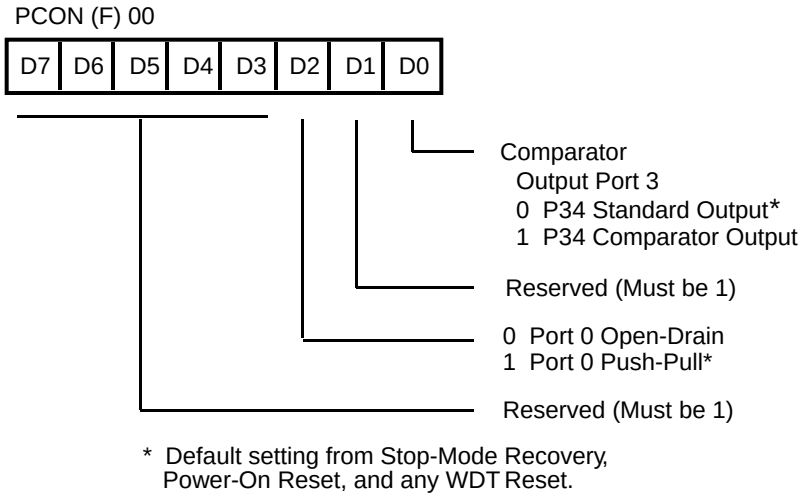


Figure 13. Port Configuration Register (PCON) (Write-Only)

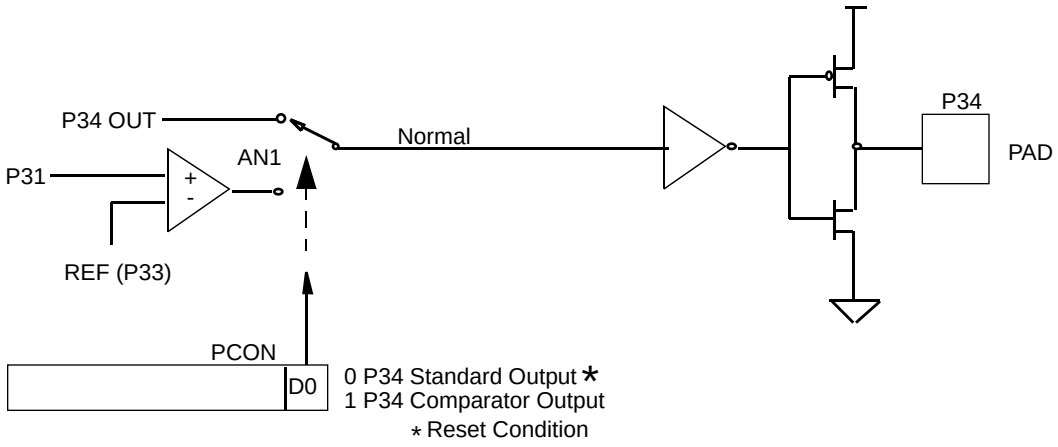


Figure 14. Port 3 P34 Output Configuration

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

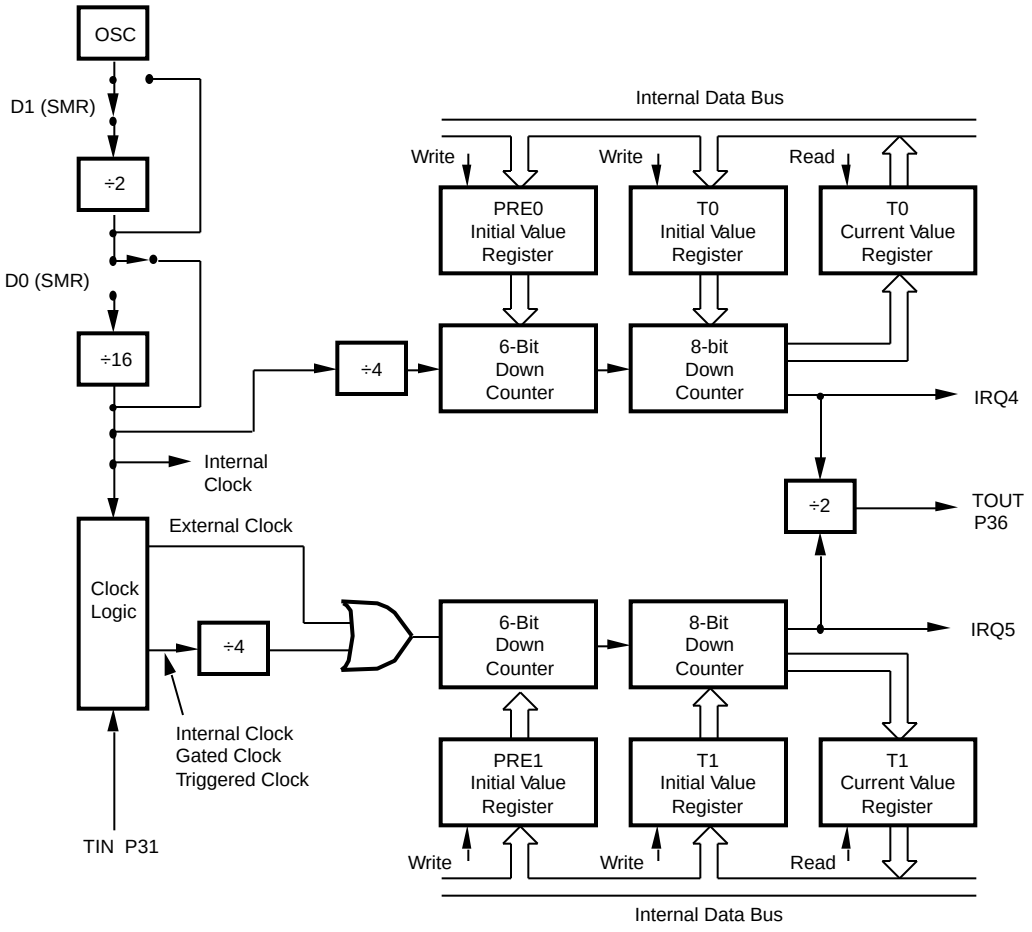


Figure 19. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

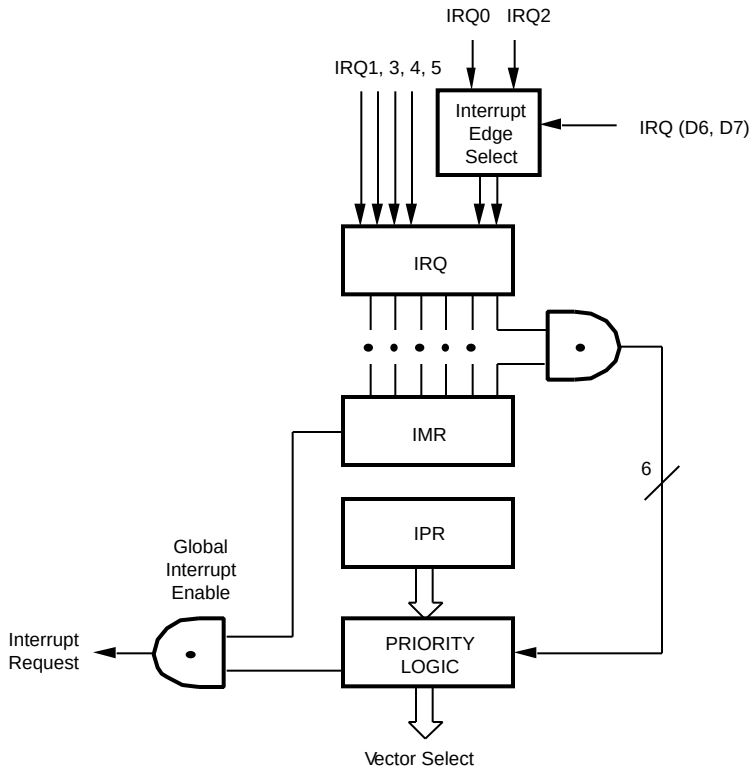


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

FUNCTIONAL DESCRIPTION (Continued)

Figure 27 shows the input circuit of the ADC. When conversion starts the analog input voltage is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Effectively, shunting 31 parallel internal resistance of the analog switches and simultaneously charging 31 parallel 0.5 pF capacitors, which is equivalent to seeing a 400 Ohms input impedance in parallel with a 16 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. For input source resistances up to 2 Kohms can be used under normal operating condition without any degradation of the input settling time. For larger input source resistance, increasing conversion cycle time or adding a capacitor to the input may be required to compensate the input settling time problem.

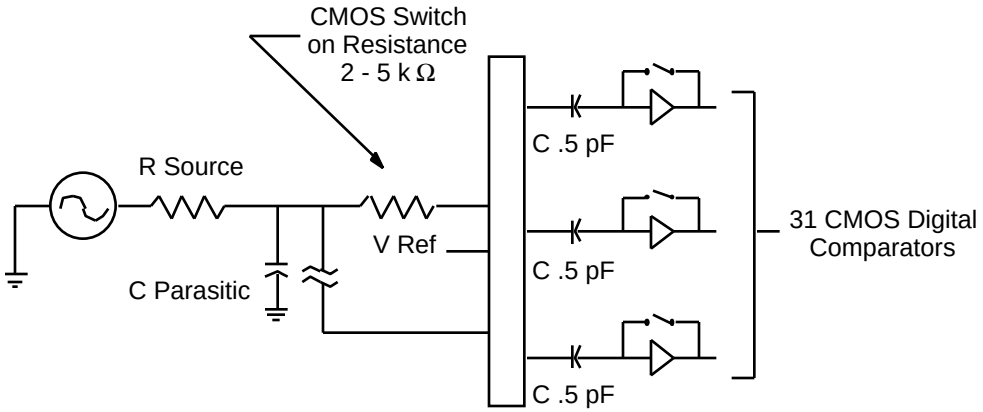


Figure 27. Input Impedance of ADC

Typical Z8 A/D Conversion Sequence

3. Set the register pointer to Extended Bank (C), that is, SRP #%0C instruction.

4. Next, set ADE flag by loading ADC1 Control Register Bank (C) Register 9, bit 7. Also, load bits 0-4 of this same register to select a AV_{CC} or A_{GND} offset value. A precision voltage divider connected to the A/D resistive ladder can offset conversion dynamic range to specified limits within the AV_{CC} and A_{GND} limits. By loading Bank (C) Register 9, bits 0-4, with the appropriate value it is possible to select from these groups:

   a. No Offset. The Converter Dynamic range is from 0V to 5.0V for AV_{CC} = 5.0V.

   b. 35 Percent A_{GND} Offset. The Converter Dynamic range is 1.75V - 5.0V for AV_{CC} = 5.0V.

   c. 50 Percent A_{GND} Offset. The Converter Dynamic range is 2.5V - 5.0V for AV_{CC} = 5.0V.

5. Select one of the eight A/D inputs for conversion by loading Bank (C) Register 8 with the desired attributes: Bits 0 - 2 select an A/D input, bits 3 and 4 select A/D conversion (or digital port I/O).

6. Set Bank (C) Register 8, bit 3 to enable A/D conversion. (This flag can be set concurrently with step 3.) This flag is automatically reset when the A/D conversion is completed, so a bit test can be performed to determine A/D readiness if necessary.

7. Read the A/D result in Bank (C) Register A. Please note that the A/D result is not valid (indeterminate) unless ADE flag (Register 9, bit 7) was previously set, otherwise A/D converter output is tri-stated.

Digital-to-Analog Converters

The Z86C84 has two Digital-to-Analog Converters (DACs). Each DAC is an 8-bit resistor string, with a programmable 0.25X, 0.5X, or 1X gain output buffer. The DAC output voltage settles after the internal data is latched into the DAC Data register. The top and bottom ends of the resistor ladder are register-selected to be connected to either the analog supply rails, AV_{CC} and A_{GND}, or two externally-provided reference voltages, VDHI and VDLO. External references are recommended to explicitly set the DAC output limits. Since the gain stage cannot drive to the supply rails, VDHI and VDLO must be within ranges shown in the specifications. If either reference approaches the analog supply rails, the output will be unable to span the reference voltage range. The externally provided reference voltages should not exceed the supply voltages. The DAC outputs are latch-up protected and can drive output loads (Figure 28).

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND

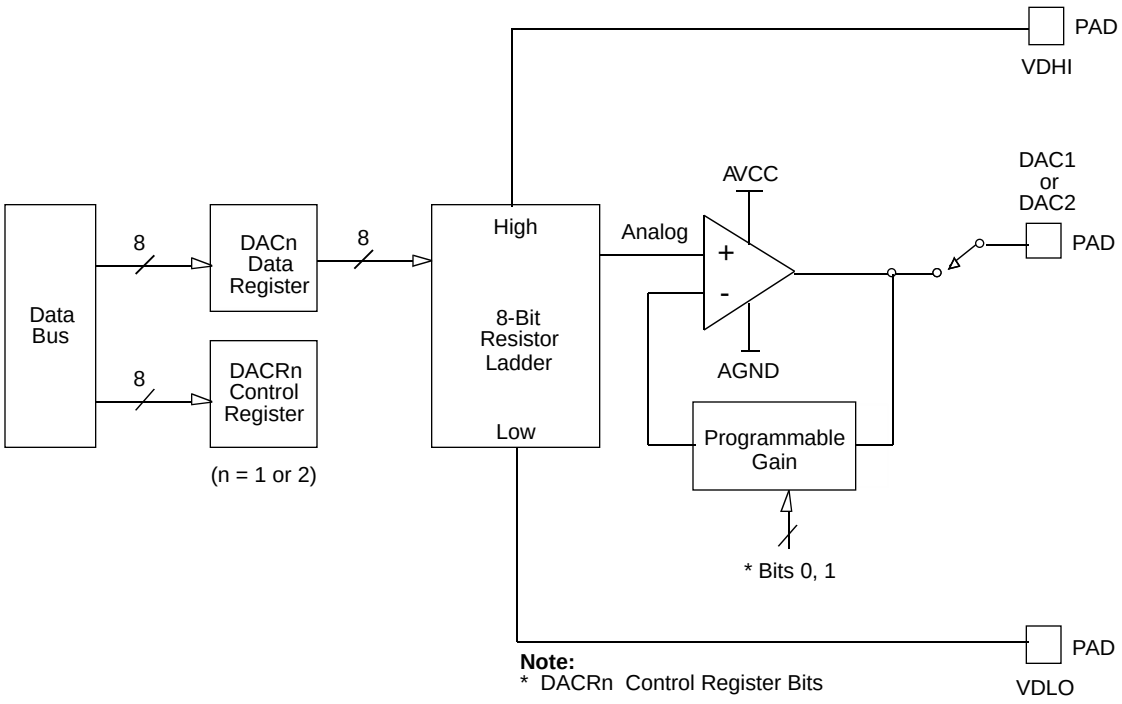


Figure 28. DAC Block Diagram

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

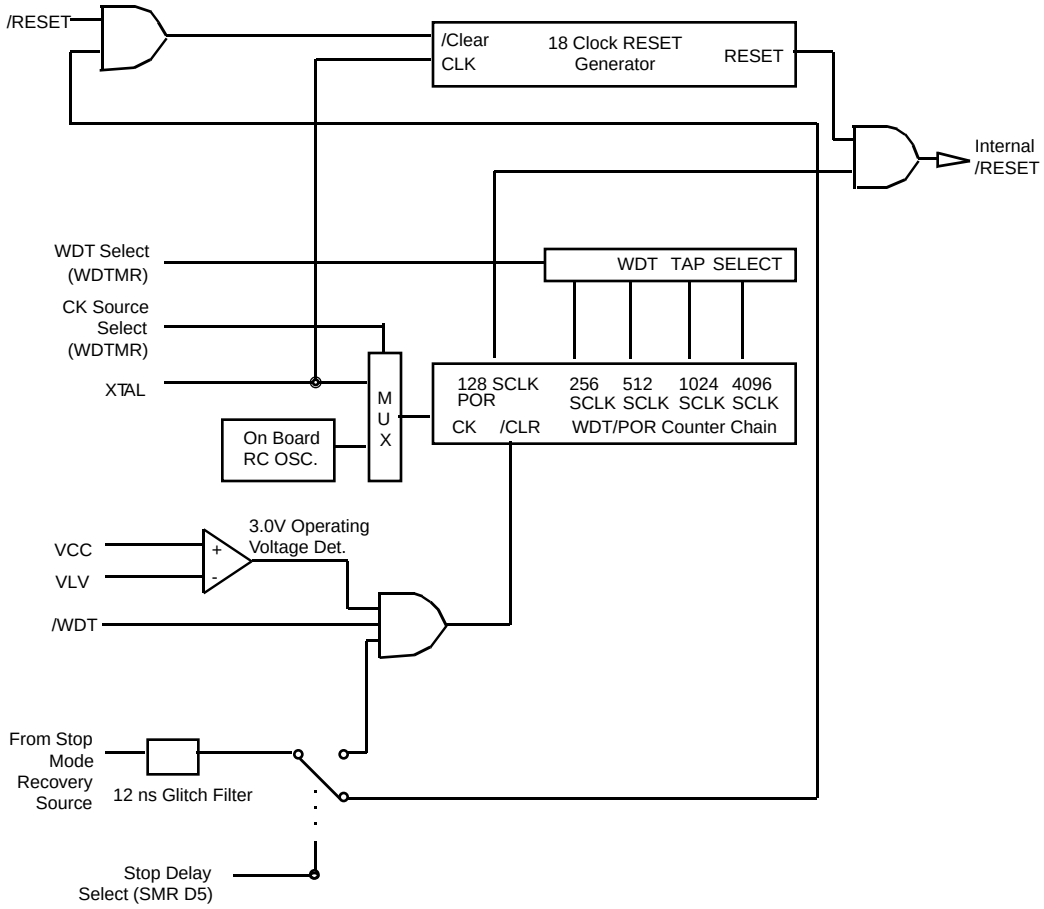


Figure 38. Resets and WDT

EXPANDED REGISTER FILE CONTROL REGISTERS (0C)

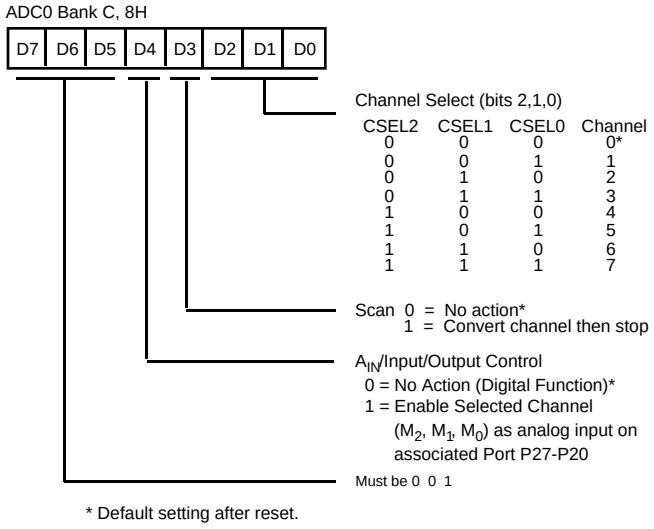


Figure 40. ADC Control Register 0 (Read/Write)

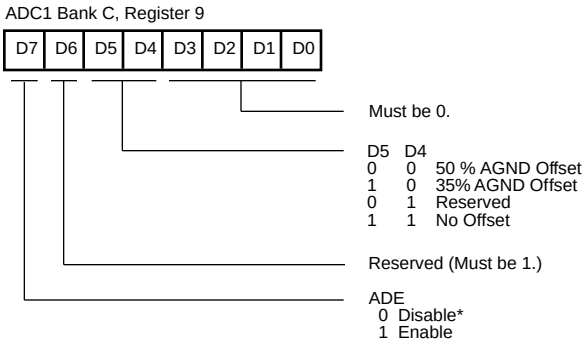


Figure 41. ADC Control Register 1 (Read/Write)

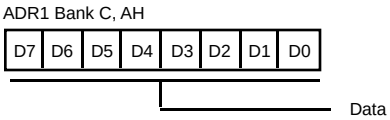


Figure 42. AD Result Register (Read Only)

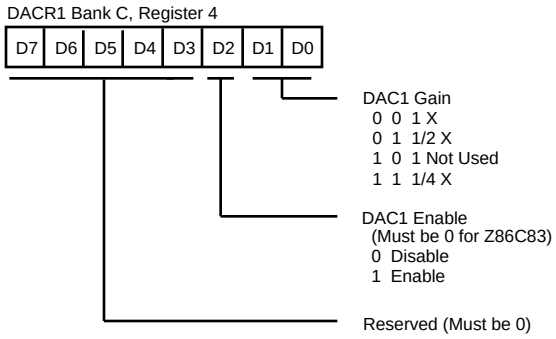


Figure 43. D/A 1 Control Register

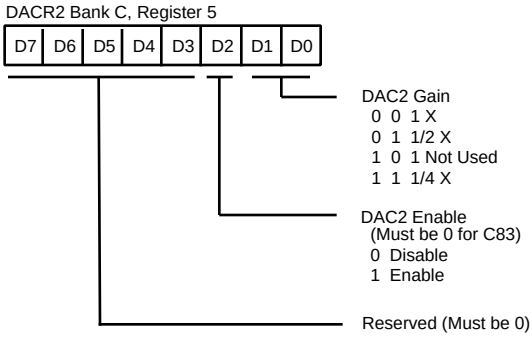


Figure 44. D/A 2 Control Register

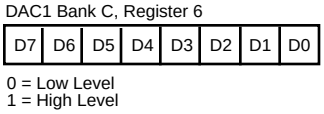


Figure 45. D/A 1 Data Register

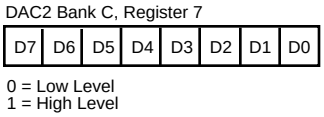
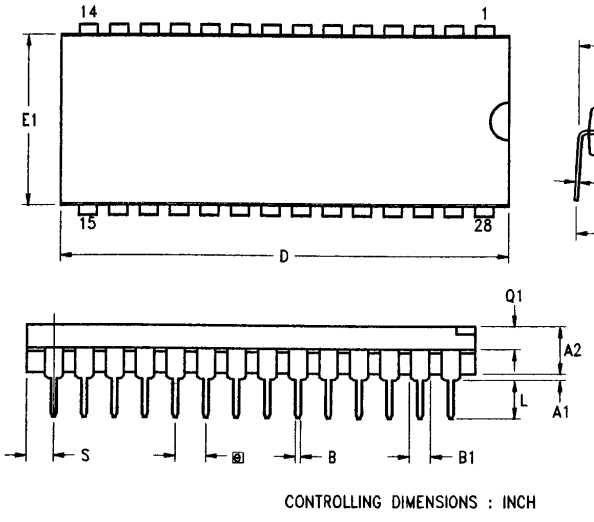


Figure 46. D/A 2 Data Register

PACKAGE INFORMATION



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C83 16 MHz			Z86E83 16 MHz		
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**	**28-Pin DIP**	**28-Pin SOIC**	**28-Pin PLCC**
Z86C8316PSC	Z86C8316SSC	Z86C8316VSC	Z86E8316PSC	Z86E8316SSC	Z86E8316VSC
Z86C8316PEC	Z86C8316SEC	Z86C8316VEC	Z86E8316PEC	Z86E8316SEC	Z86E8316VEC
Z86C84 16 MHz					
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**			
Z86C8416PSC	Z86C8416SSC	Z86C8416VSC			
Z86C8416PEC	Z86C8416SEC	Z86C8416VEC			

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to + 70°C
E = -40°C to +105°C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard

Example:

Z 86C83 16 P S C is a Z86C83, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow