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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316ssg

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

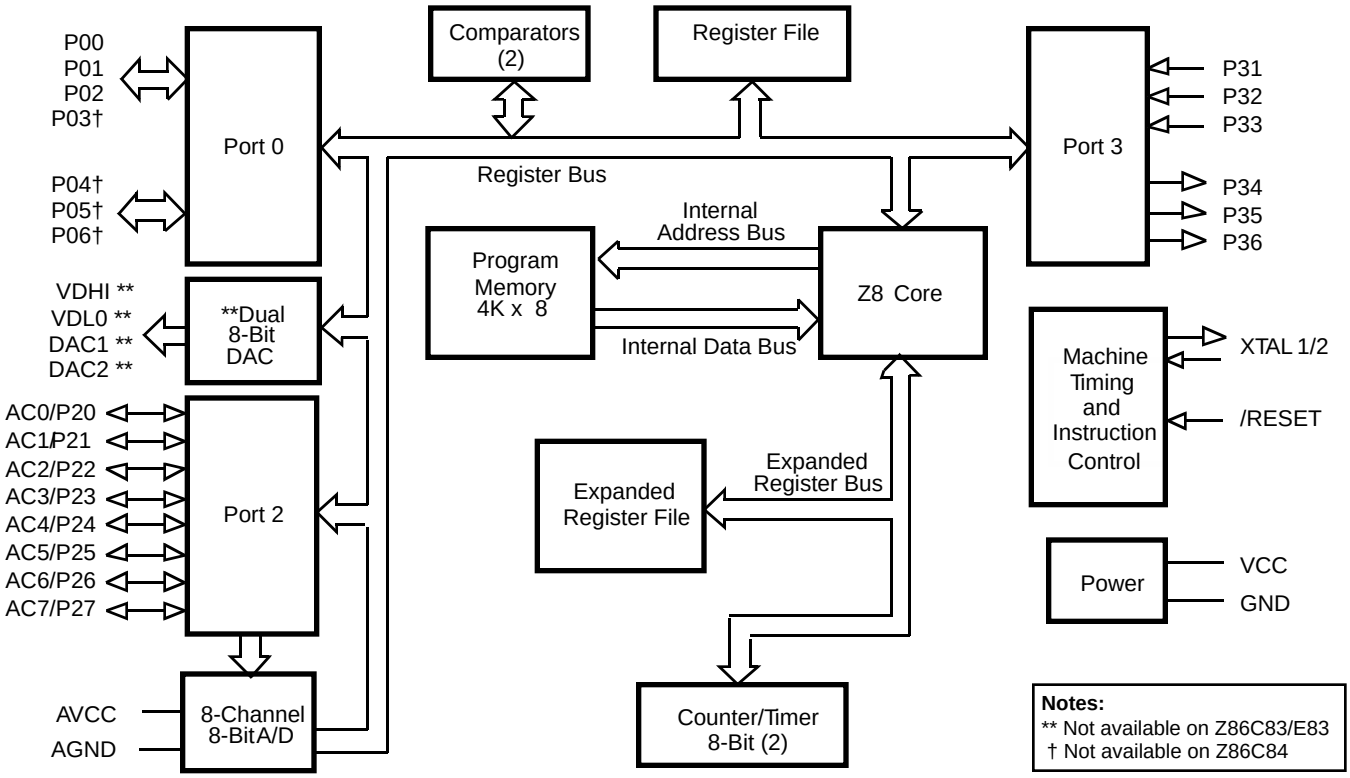


Figure 1. Z86C83/C84/E83 Functional Block Diagram

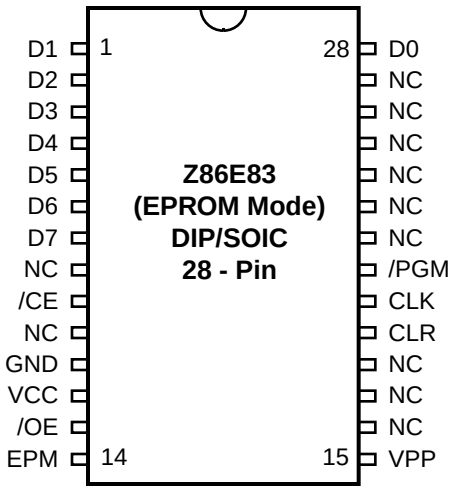


Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

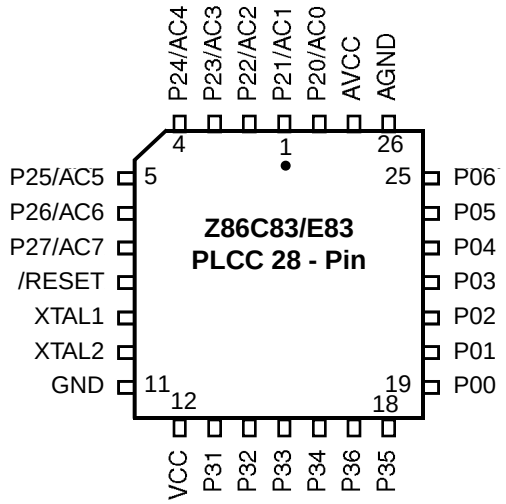


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

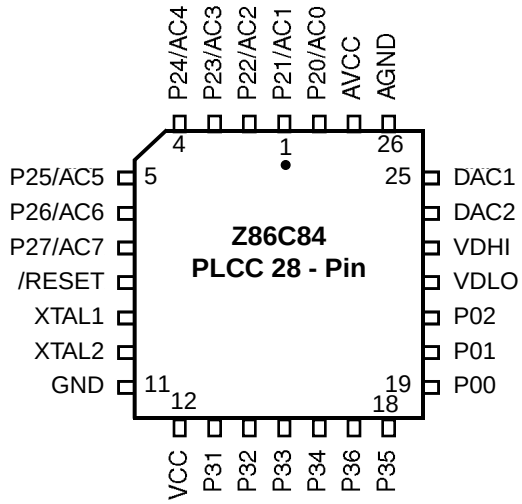


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

For Z86E83 Only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	Max	T_A = -40° C to +105° C Min	Max	Typical [13] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Ouput High Voltage	3.5V	V_{CC}-0.4				3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.5V		0.6			0.2	V	I_{OH} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OH} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2			0.3	V	I_{OH} = +6.0 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OH} = +10.0 mA	8
V_{RH}	Reset Input High Voltage	3.5V	0.8V_{CC}	V_{CC}			1.5	V		
		5.5V	0.8V_{CC}	V_{CC}	0.8V_{CC}	V_{CC}	2.1	V		
		3.5V	GND-0.3	0.2V_{CC}			1.1	V		
		5.5V	GND-0.3	0.2V_{CC}	GND-0.3	0.2V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25			10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V		-130			-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.5V		20			7	mA	@16 MHz	1,4
		5.5V		25		25	20	mA	@16 MHz	1,4
I_{CC1}	Standby Current (HALT Mode)	3.5V		4.5			2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		3.5V		3.4			1.5	mA	Clock divide by 16 @ 16 MHz	1,4
		5.5V		7.0		7.0	2.9	mA	Clock divide by 16 @ 16 MHz	1,4

For Z86C84 Only

Table 4. D/A Converter Electrical Characteristics
V_{CC} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		0.25	0.5	LSB
Supply Range	3.0	3.3	3.6	Volts
Power dissipation, no load		10		mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 3 volts	1.5	1.8	2.1	Volts
VDLO range at 3 volts	0.2	0.5	0.8	Volts
VDHI–VDLO, at 3 volts	1.3	1.6	1.9	Volts
Capacitive output load, CL			20	pF
Resistive output load, RL	50K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 3.0V – 3.6V
Temp: 0–70°C

For Z86C84 Only

Table 5. D/A Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.25	1	LSB
Differential non-linearity		0.25	0.5	LSB
Setting time, 1/2 LSB		1.5	3.0†	µsec
Zero Error at 25°C		10	20	mV
Full Scale error at 25°C		1	2	% FSR
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Ref Input resistance	2K	4K	10K	Ohms
Output noise voltage		50		µVp-p
VDHI range at 5 volts	2.6		3.5	Volts
VDLO range at 5V volts	0.8		1.7	Volts
VDHI–VDLO, at 5V volts	0.9		2.7	Volts
Capacitive output load, CL			30	pF
Resistive output load, RL	20K			Ohms
Output slew rate	1.0	3.0		V/µsec

Notes:
Voltage: 4.5V - 5.5V
Temp: 0-70°C
† The C86C84 Emulator has maximum setting time of 20 µsec. (10 µsec. typical).

Port 3 (P36-P31) Port 3 is a 6-bit, CMOS-compatible port, with three fixed inputs (P33-P31) and three fixed outputs (P34-P36), configured under software control for Input/Output, Counter/Timers, interrupt, and port handshake. P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, and P36 are push-pull output lines (Figure 11). Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 3 is falling-edge interrupt input. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P31/P36 and P32/P35 (Table 10).

Port 3 also provides the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); timer input and output signals (T_{IN} and T_{OUT}).

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on CMOS inputs that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Pins 03, 04, 05, 06 have permanently enabled Auto Latches.

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. In Analog Mode, the internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR register. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In Digital Mode, P33 can be used as a Port 3 register input or IRQ1 source. P34 outputs the comparator outputs by software programming the PCON Register bit D0 to 1.

Note: When enabling/or disabling the analog mode, the following is recommended:

1. allow two NOP delays before reading the comparator output

2. disable interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

PIN FUNCTIONS (Continued)

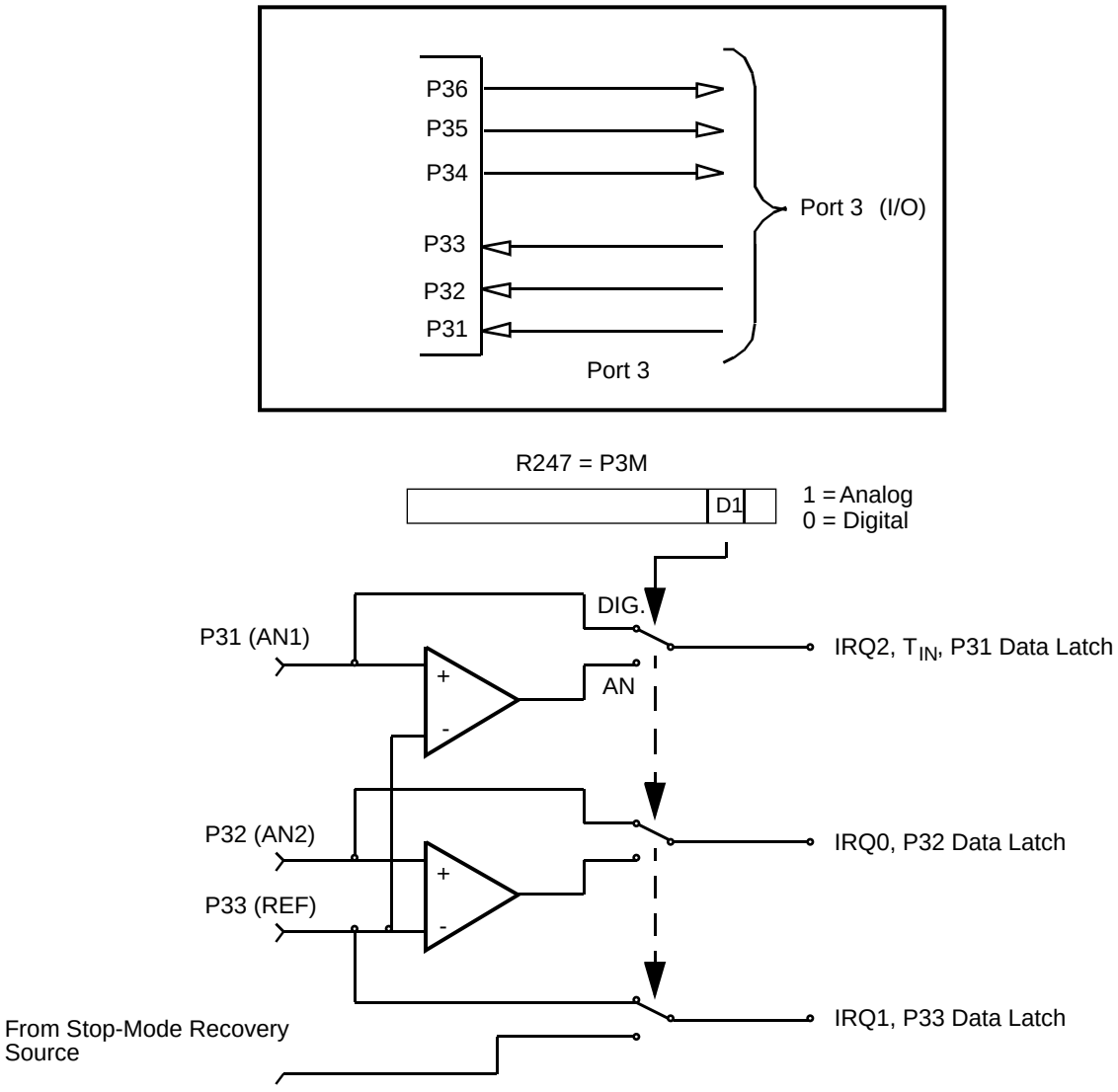


Figure 12. Port 3 Input Configuration

FUNCTIONAL DESCRIPTION

RESET. (Input, Active Low). This pin initializes the MCU. Reset is accomplished either through Power-On Reset (POR), Watch-Dog Timer (WDT) Reset, or external reset. During POR, and WDT Reset, the internally generated reset is driving the reset pin Low for the POR time. **Any devices driving the reset line must be open-drain to avoid damage from a possible conflict during reset conditions.** Pull-up is provided internally.

After the POR time, /RESET is a Schmitt-triggered input. After the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. Program execution begins at location 000C (hex), 5-10 TpC cycles after the RST is released. For POR, the reset output time is T_{POR}.

Program Memory. C83/C84/E83/E84 can address up to 4 KB of internal Program Memory (Figure 15). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 13 to 4095 consist of on-chip, mask-programmed ROM.

ROM Protect. The 4 KB of Program Memory is mask programmable. A ROM protect feature will prevent dumping of the ROM contents from an external program outside the ROM.

Expanded Register File. The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 16). These register banks are known as the Expanded Register File (ERF). Bits 3-0 of the Register Pointer (RP) select the active ERF bank. Bits 7-4 of register RP select the working register group (Figure 16). Four system configuration registers reside in the ERF address space in Bank F and eight registers reside in Bank C. The rest of the ERF addressing space is not physically implemented, and is open for future expansion.

Note: When using Zilog's Cross Assembler version 2.1 or earlier, use the LD RP, #0X instruction rather than the SRP #0X instruction to access the ERF.

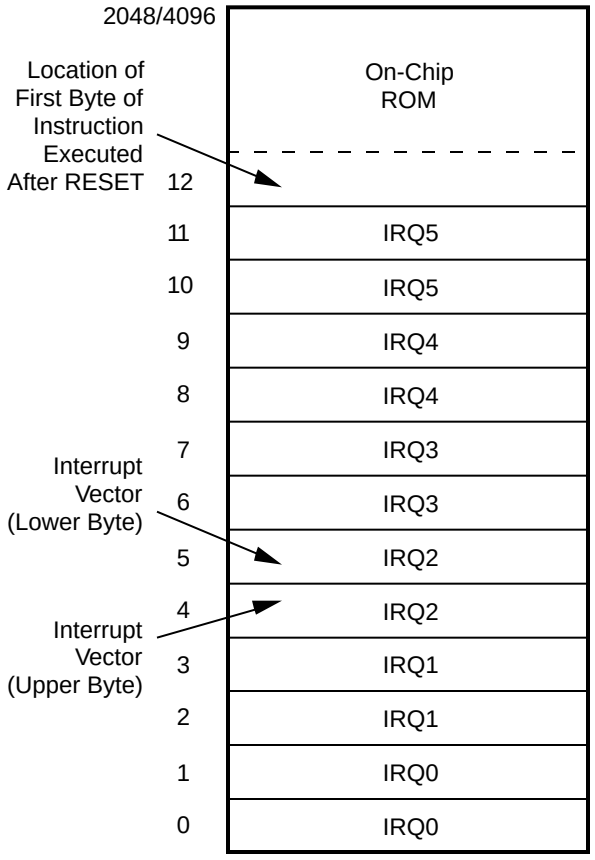


Figure 15. Program Memory Map

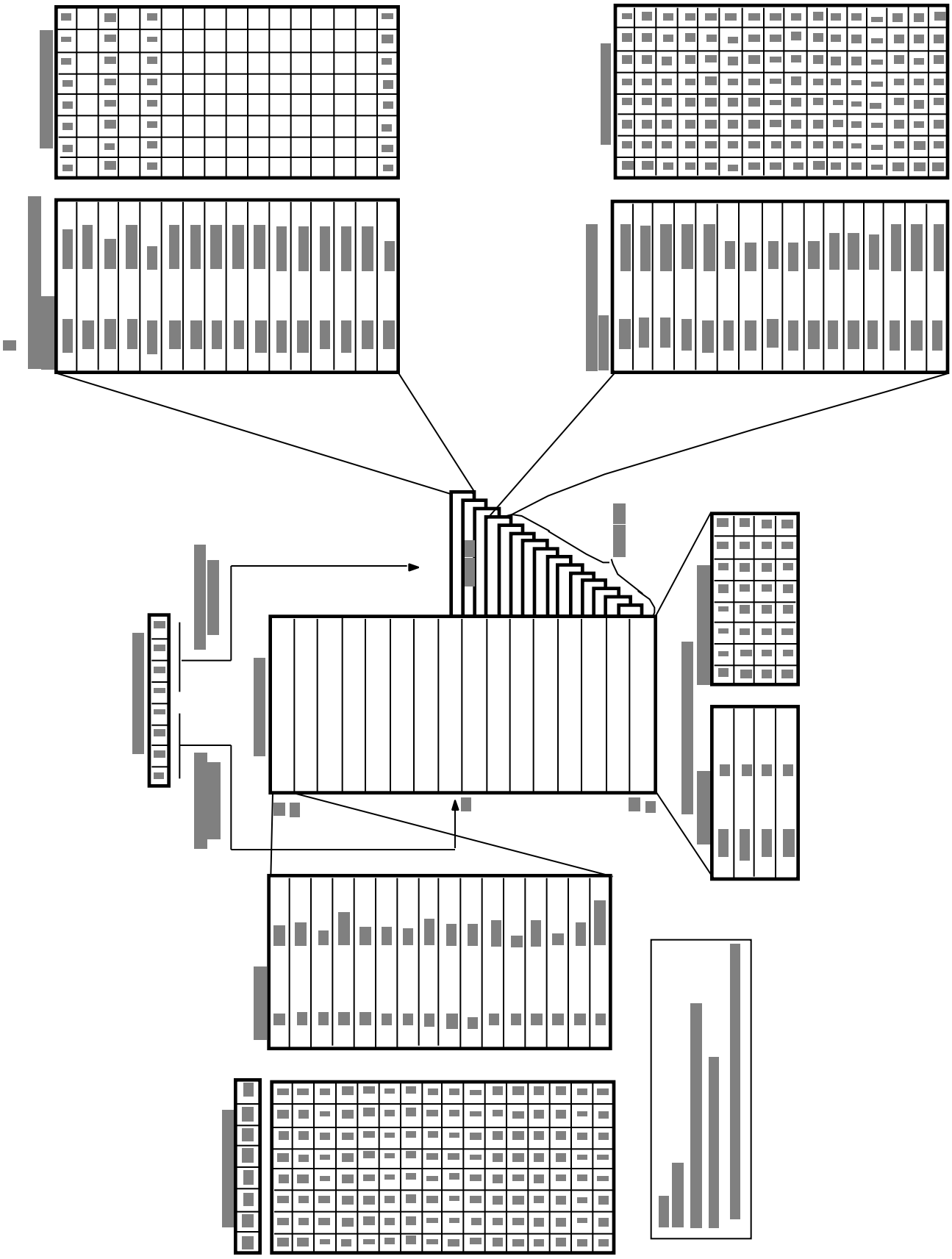


Figure 16. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

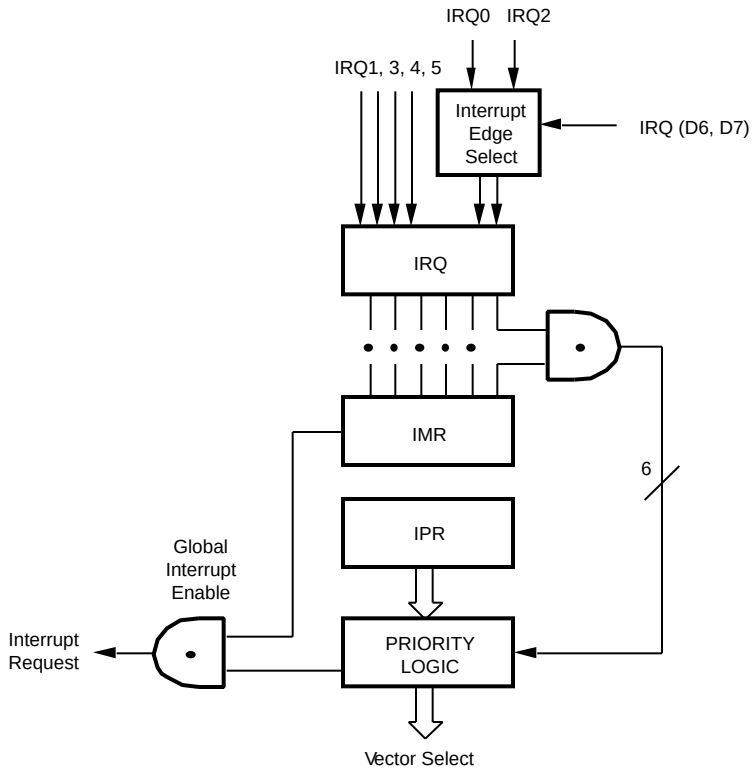


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

Digital-to-Analog Converters

The Z86C84 has two Digital-to-Analog Converters (DACs). Each DAC is an 8-bit resistor string, with a programmable 0.25X, 0.5X, or 1X gain output buffer. The DAC output voltage settles after the internal data is latched into the DAC Data register. The top and bottom ends of the resistor ladder are register-selected to be connected to either the analog supply rails, AV_{CC} and A_{GND}, or two externally-provided reference voltages, VDHI and VDLO. External references are recommended to explicitly set the DAC output limits. Since the gain stage cannot drive to the supply rails, VDHI and VDLO must be within ranges shown in the specifications. If either reference approaches the analog supply rails, the output will be unable to span the reference voltage range. The externally provided reference voltages should not exceed the supply voltages. The DAC outputs are latch-up protected and can drive output loads (Figure 28).

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND

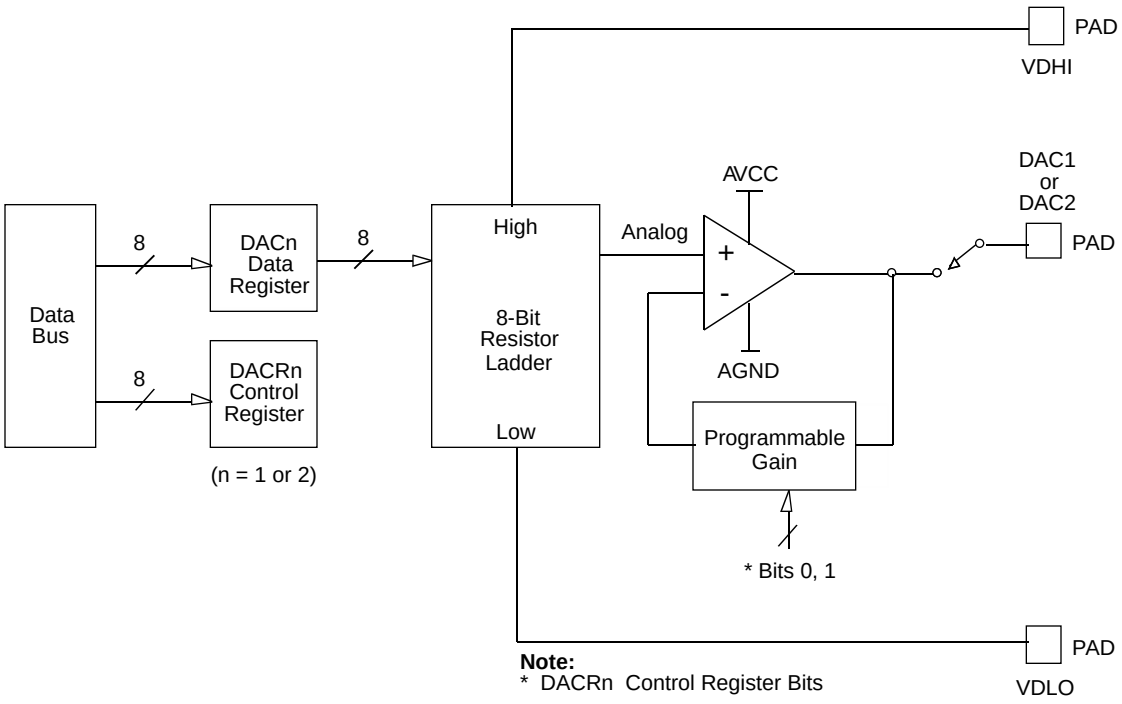


Figure 28. DAC Block Diagram

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

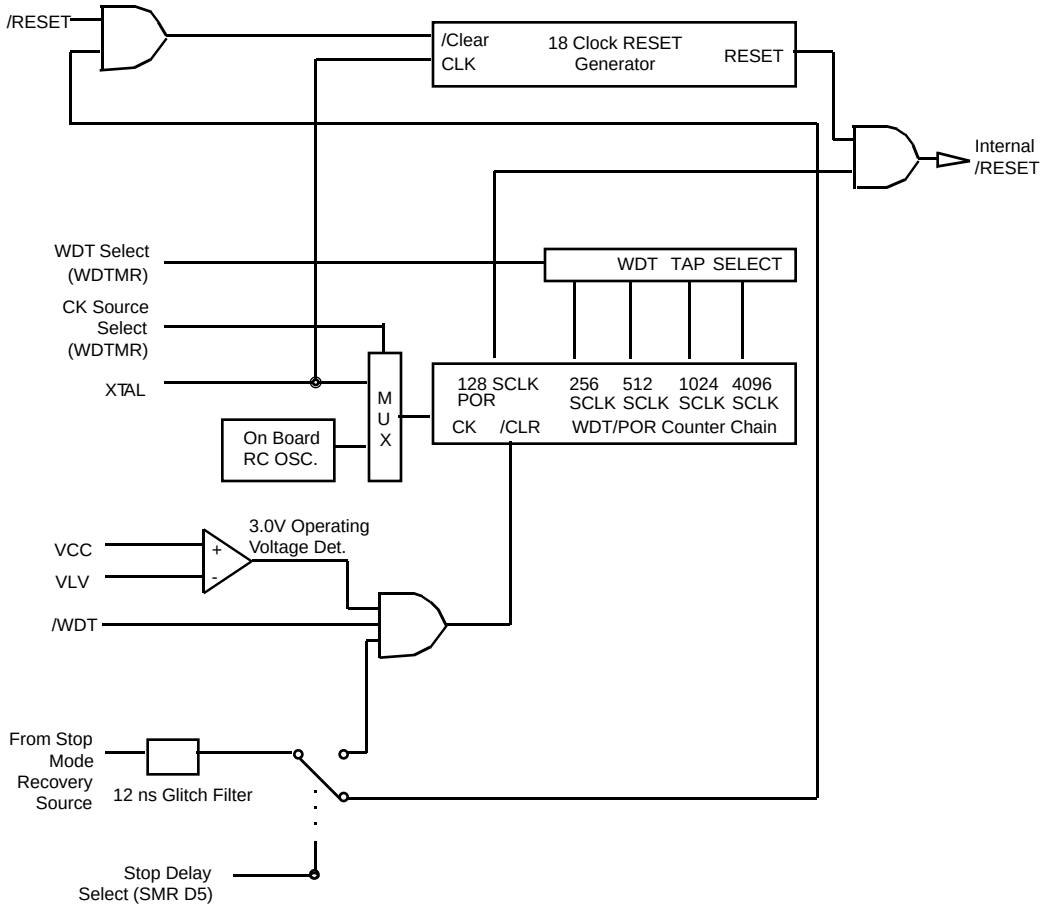


Figure 38. Resets and WDT

EXPANDED REGISTER FILE CONTROL REGISTERS (0C)

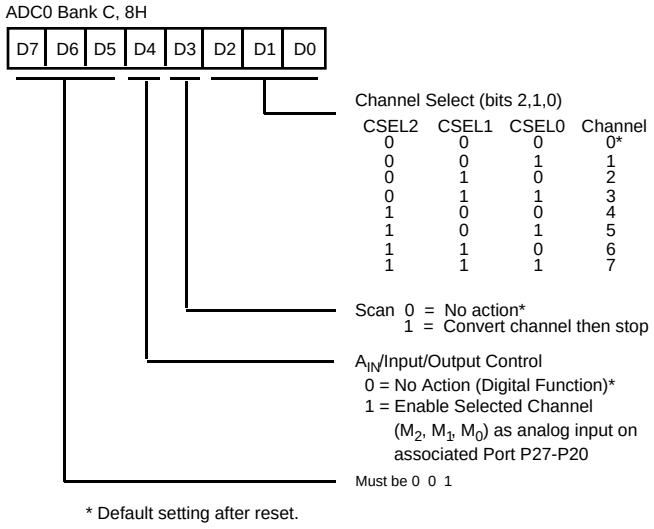


Figure 40. ADC Control Register 0 (Read/Write)

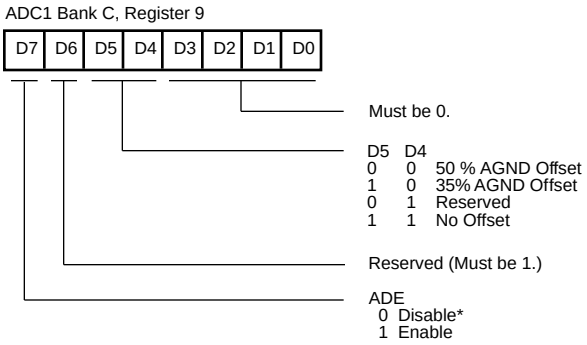


Figure 41. ADC Control Register 1 (Read/Write)

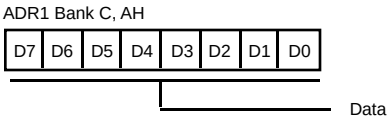


Figure 42. AD Result Register (Read Only)

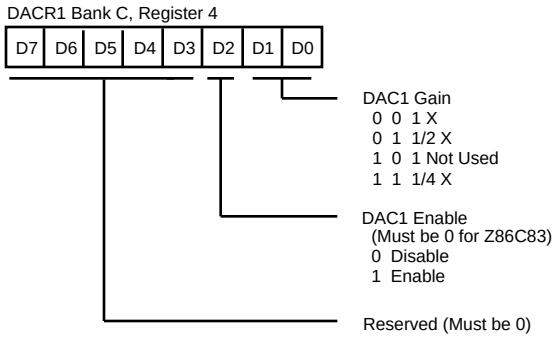


Figure 43. D/A 1 Control Register

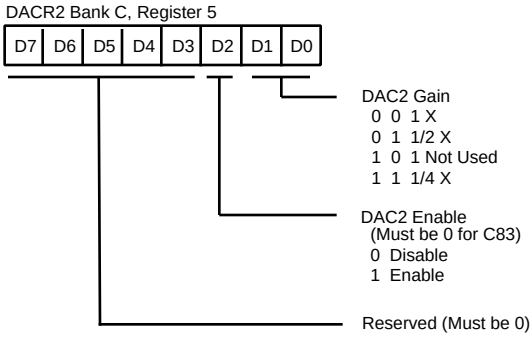


Figure 44. D/A 2 Control Register

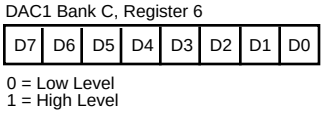


Figure 45. D/A 1 Data Register

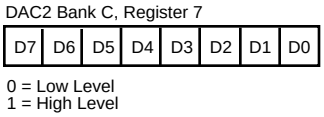
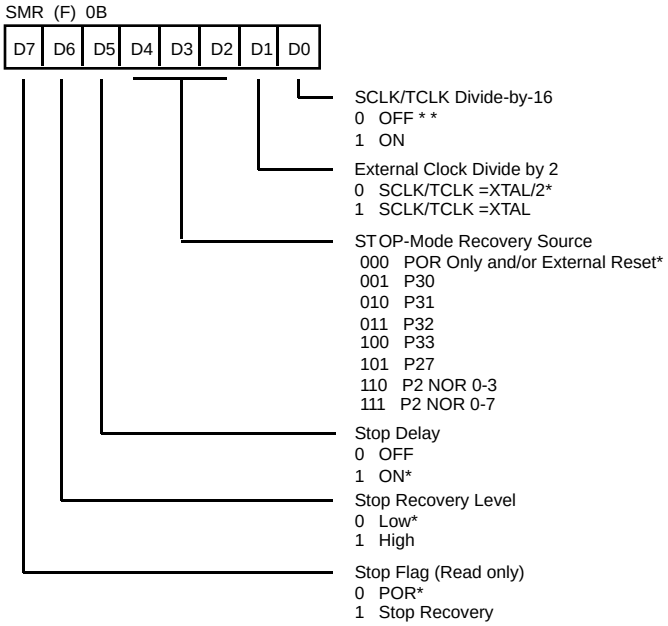


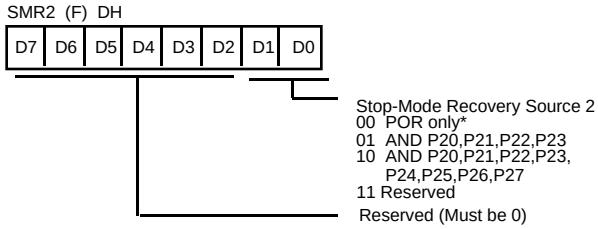
Figure 46. D/A 2 Data Register

EXPANDED REGISTER FILE CONTROL REGISTERS



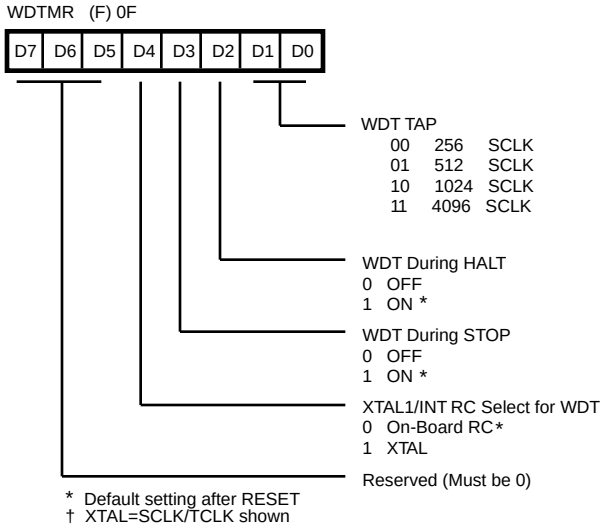
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 47. Stop-Mode Recovery Register (Write-Only, except Bit 7 which is Read-Only)



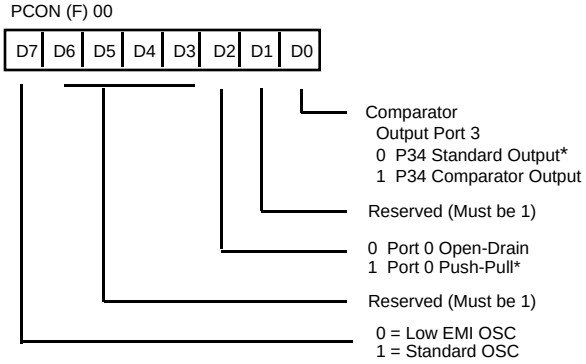
Note: Not used in conjunction with SMR Source

Figure 48. Watch-Dog Timer Mode Register 2



* Default setting after RESET
† XTAL=SCLK/TCLK shown

Figure 49. Watch-Dog Timer Mode Register (Write-Only)



* Default setting from Stop-Mode Recovery
Power-On Reset, and any WDT Reset.

Figure 50. Port Configuration Register (PCON) (Write-Only)

Z8 CONTROL REGISTERS

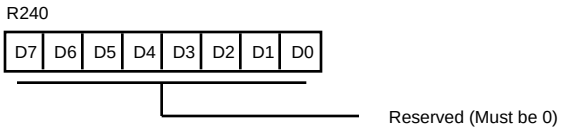


Figure 51. Reserved

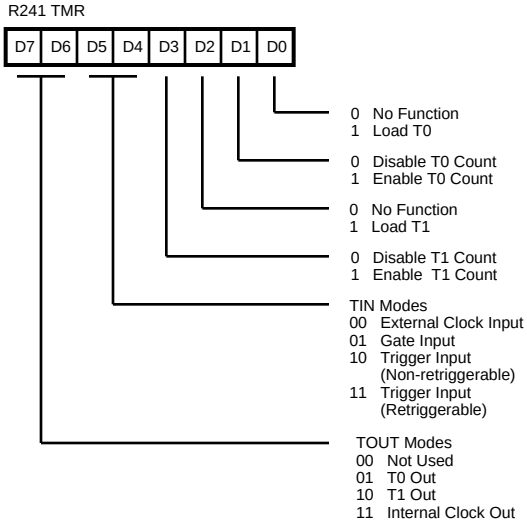


Figure 52. Timer Mode Register ($F1_H$: Read/Write)

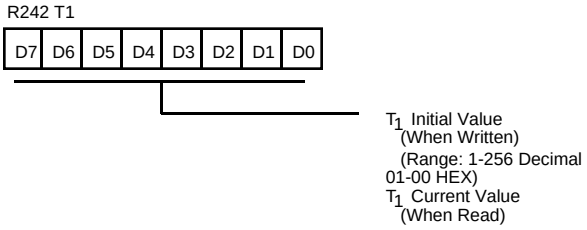


Figure 53. Counter/Timer 1 Register ($F2_H$: Read/Write)

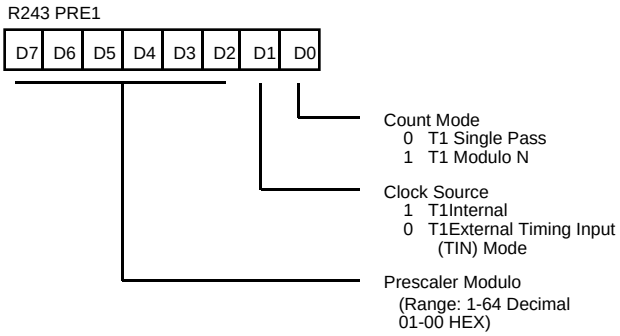


Figure 54. Prescaler 1 Register ($F3_H$: Write-Only)

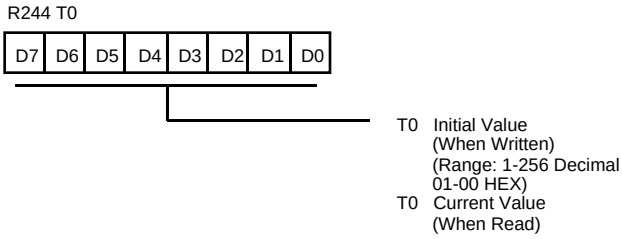


Figure 55. Counter/Timer 0 Register ($F4_H$: Read/Write)

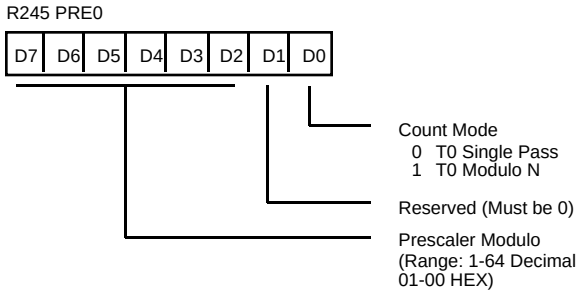


Figure 56. Prescaler 0 Register ($F5_H$: Write-Only)

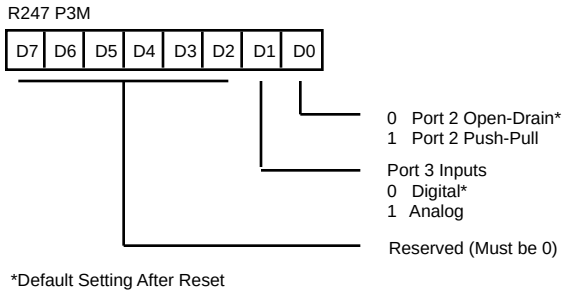


Figure 57. Port 3 Mode Register ($F7_H$: Write-Only)

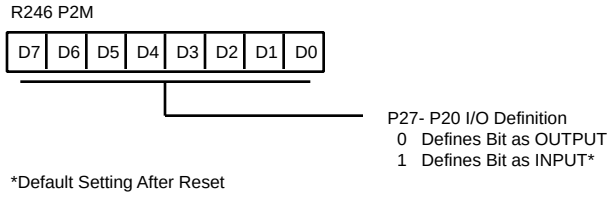


Figure 58. Port 2 Mode Register ($F6_H$: Write-Only)

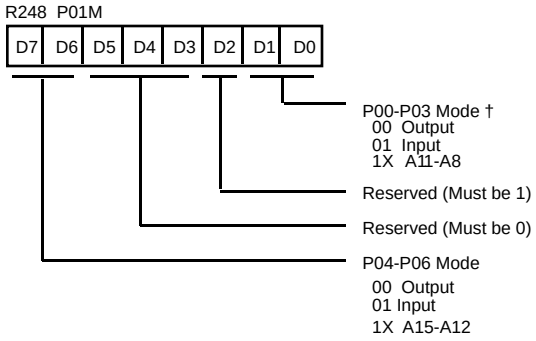


Figure 59. Port 0 and 1 Mode Register ($F8_H$: Write-Only)

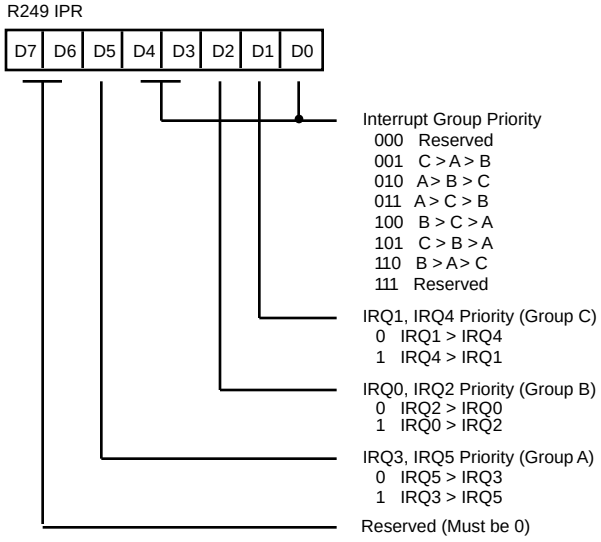


Figure 60. Interrupt Priority Register ($F9_H$: Write-Only)

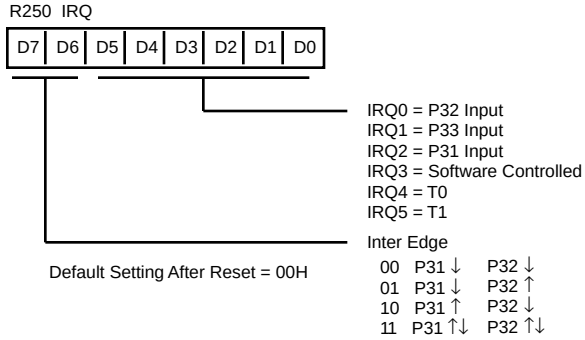


Figure 61. Interrupt Request Register (F_{AH}: Read/Write)

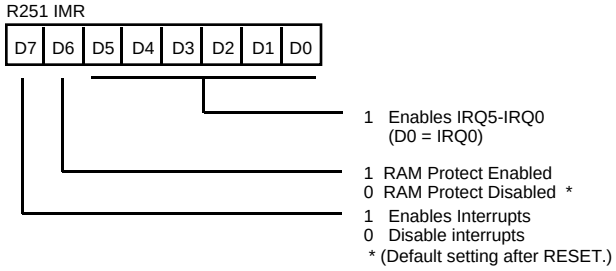


Figure 62. Interrupt Mask Register (F_{BH}: Read/Write)

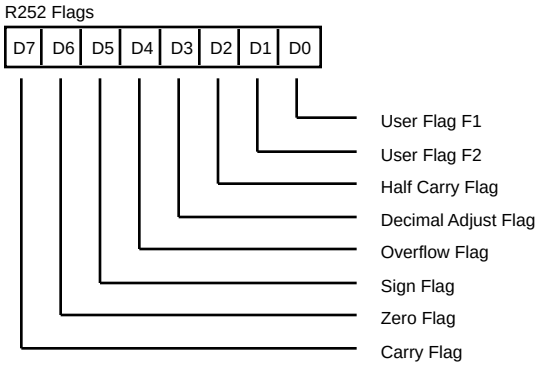


Figure 63. Flag Register (F_{CH}: Read/Write)

Z8 CONTROL REGISTERS (Continued)

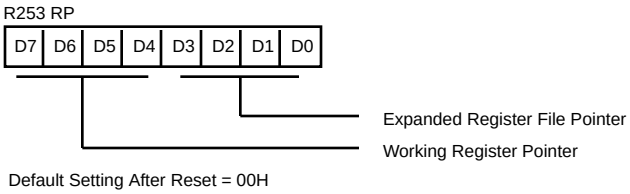


Figure 64. Register Pointer (F_{DH}: Read/Write)

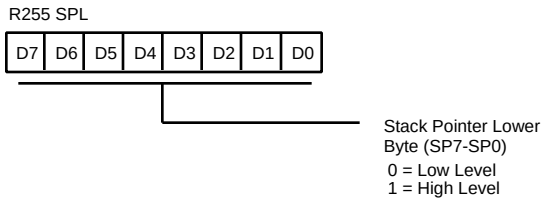


Figure 66. Stack Pointer (F_{FH}: Read/Write)

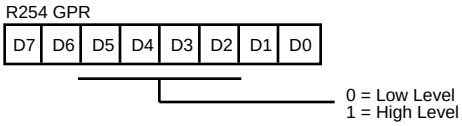


Figure 65. General-Purpose Register (F_{EH}: Read/Write)

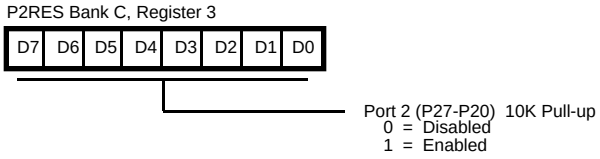
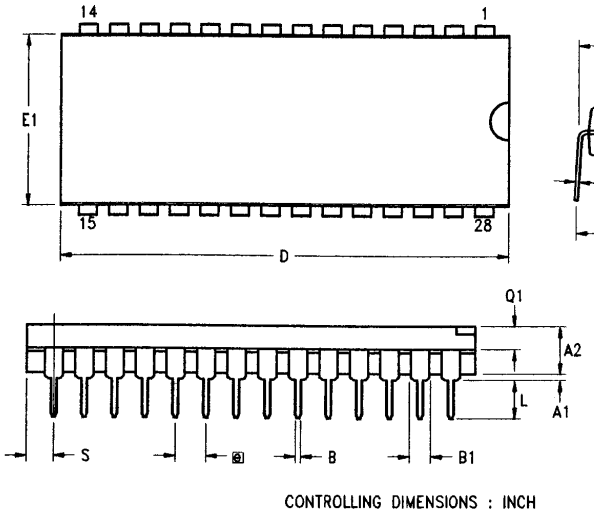


Figure 67. Port 2 Pull-up Register

PACKAGE INFORMATION



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C83 16 MHz			Z86E83 16 MHz		
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**	**28-Pin DIP**	**28-Pin SOIC**	**28-Pin PLCC**
Z86C8316PSC	Z86C8316SSC	Z86C8316VSC	Z86E8316PSC	Z86E8316SSC	Z86E8316VSC
Z86C8316PEC	Z86C8316SEC	Z86C8316VEC	Z86E8316PEC	Z86E8316SEC	Z86E8316VEC
Z86C84 16 MHz					
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**			
Z86C8416PSC	Z86C8416SSC	Z86C8416VSC			
Z86C8416PEC	Z86C8416SEC	Z86C8416VEC			

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to + 70°C
E = -40°C to +105°C

Speed

16 = 16 MHz

Environmental

C = Plastic Standard

Example:

Z 86C83 16 P S C is a Z86C83, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow