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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316vec

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

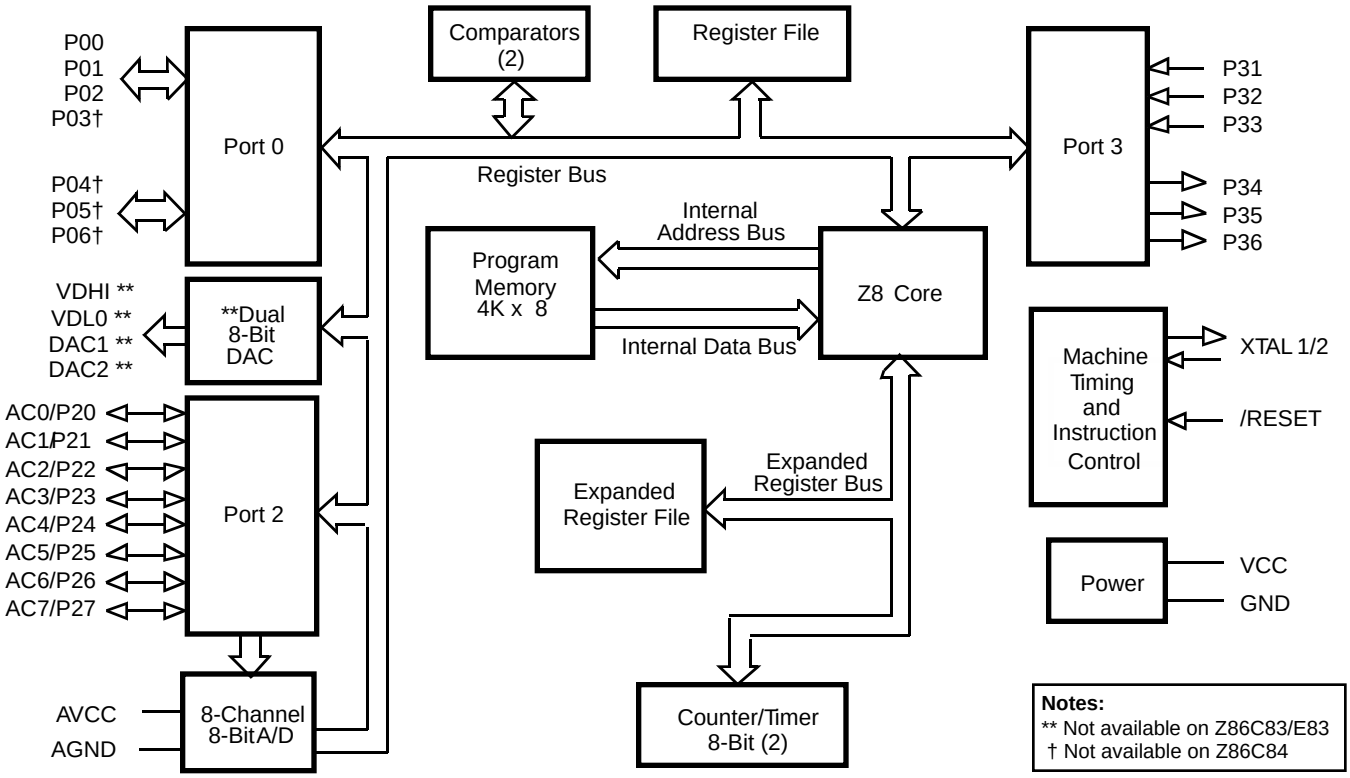


Figure 1. Z86C83/C84/E83 Functional Block Diagram

PIN DESCRIPTION (Continued)

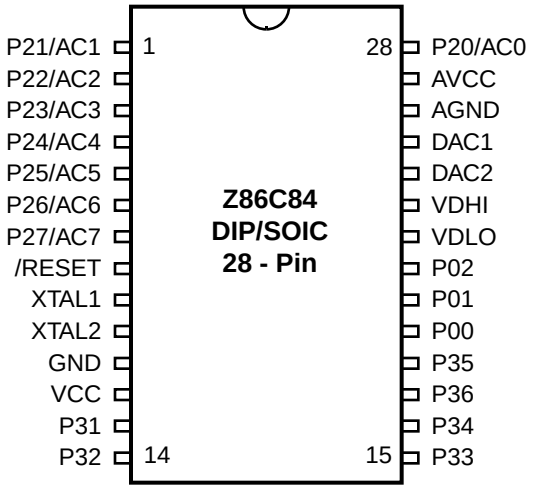


Figure 3. Z86C84 28-Pin DIP and SOIC Pin Configuration

Table 2. Z86C84 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-21	P00-P02	Port 0, Bits 0-3	Input/Output
22	VDLO	D/A Ref. Volt.,Low	Input
23	VDHI	D/A Ref. Volt.,High	Input
24-25	DAC2-1	D/A Converter	Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP, PLCC and SOIC Pin Description and Configuration are identical

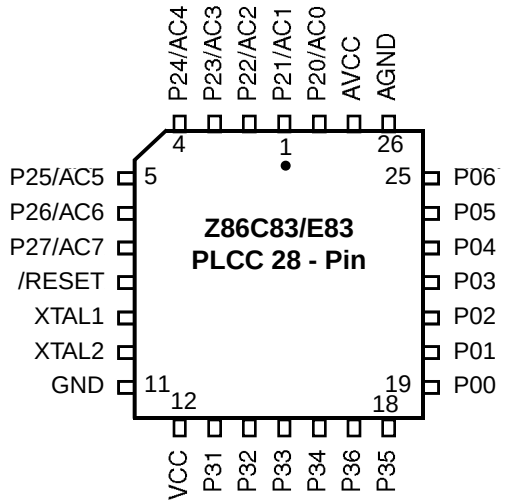


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

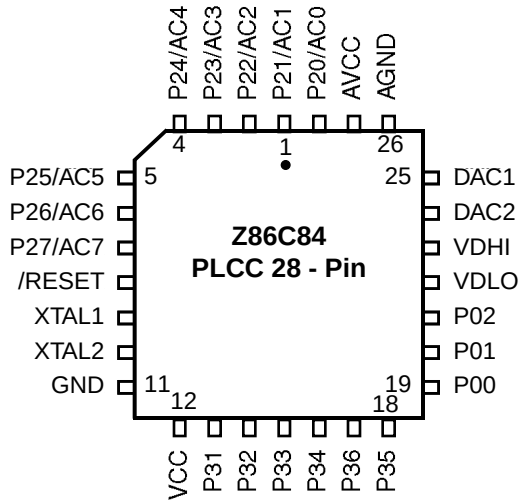


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

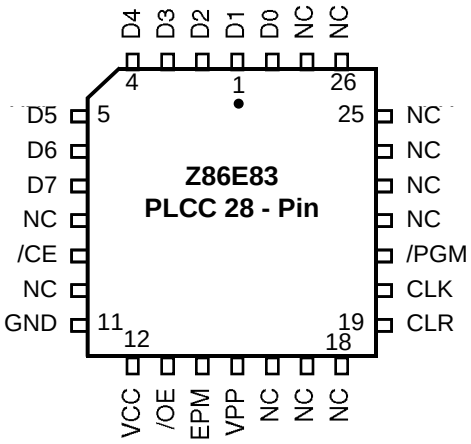


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	T_A = 0° C to +70° C Max	T_A = -40° C to +105° C Min	T_A = -40° C to +105° C Max	Typical [13] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.5V		8			1	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.5V		500			310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
V_{ICR}	Input Common Mode	3.5V	0	V_{CC}-1.0V	0			V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.5V		8			5	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		15		20	11	µA	$0V<V_{IN}<V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V		-5			-3	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		-8		-10	-6	µA	$0V<V_{IN}<V_{CC}$	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max. Int. CLK Frequency	7

Notes:

1. Combined digital V_{CC} and analog AV_{CC} supply currents
2. GND = 0V
3. V_{CC} voltage specification of 3.5V guarantees 3.5V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V
4. All outputs unloaded, I/O pins floating, inputs at rail
5. CL1 = CL2 = 100 pF
6. Same as note [4] except inputs at V_{CC}
7. The V_{LV} increases as the temperature decreases
8. Standard Mode (not Low EMI)
9. Auto Latch (mask option) selected
10. For analog comparator, inputs when analog comparators are enabled
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating
12. Excludes clock pins
13. Typicals are at V_{CC} = 3.5V and 5.0V
14. Internal RC selected

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Low EMI Mode Only) For Z86E83 Only

No	Symbol	Parameter	V_{CC} [Note 6]	T_A = 0°C to +70°C 4 MHz Min	4 MHz Max	T_A = -40°C to +105°C 4 MHz Min	4 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC			ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		25			ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	125				ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100				ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	3TpC					1,7,8
			5.5V	3TpC		3TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	4TpC					1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100			ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100				ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	3TpC					1,3,7,8
			5.5V	3TpC		3TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	3TpC					1,2,7,8
			5.5V	3TpC		2TpC			1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12				ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.5V		5TpC				4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
9. For LC oscillator and for oscillator driven by clock driver

CAPACITANCE (Continued)

Additional Timing Table (SKLK/TCLK = XTAL/2) For Z86C83/C84 Only

				T_A = 0°C to +70°C				T_A = -40°C to +150°C					
			VCC	12 MHz		16MHz		12 MHz		16 MHz			
No	Sym	Parameter	[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		5TpC		5TpC		
			5.5V		5TpC		5TpC		5TpC		5TpC		
12	Twdt	Watch-Dog Timer Delay Time										WDTMR Reg	D1,D0
			5.5V	6.25		6.25		6.25		6.25		ms	0,0 [6]
			5.5V	12.5		12.5		12.5		12.5		ms	0,1 [6]
			5.5V	25		25		25		25		ms	1,0 [6]
			5.5V	100		100		100		100		ms	1,1 [6]
13	T_{POR}	Power On Reset Delay	3.0V	7	24	7	25	7	24	7	25	ms	6
			5.5V	3	13	3	14	3	13	3	14	ms	6

Notes:

1. Timing References used 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 0
5. The V_{CC} voltage specification of 3.0V guarantees 3.3V± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
6. Using internal on-board RC oscillator

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 8. A/D Converter Electrical Characteristics
V_{CC} = 3.5V

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	3.5			Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 9. A/D Converter Electrical Characteristics
V_{CC} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time	4.3		35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

Port 3 (P36-P31) Port 3 is a 6-bit, CMOS-compatible port, with three fixed inputs (P33-P31) and three fixed outputs (P34-P36), configured under software control for Input/Output, Counter/Timers, interrupt, and port handshake. P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, and P36 are push-pull output lines (Figure 11). Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 3 is falling-edge interrupt input. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P31/P36 and P32/P35 (Table 10).

Port 3 also provides the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); timer input and output signals (T_{IN} and T_{OUT}).

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on CMOS inputs that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Pins 03, 04, 05, 06 have permanently enabled Auto Latches.

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. In Analog Mode, the internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR register. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In Digital Mode, P33 can be used as a Port 3 register input or IRQ1 source. P34 outputs the comparator outputs by software programming the PCON Register bit D0 to 1.

Note: When enabling/or disabling the analog mode, the following is recommended:

1. allow two NOP delays before reading the comparator output

2. disable interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

PIN FUNCTIONS (Continued)

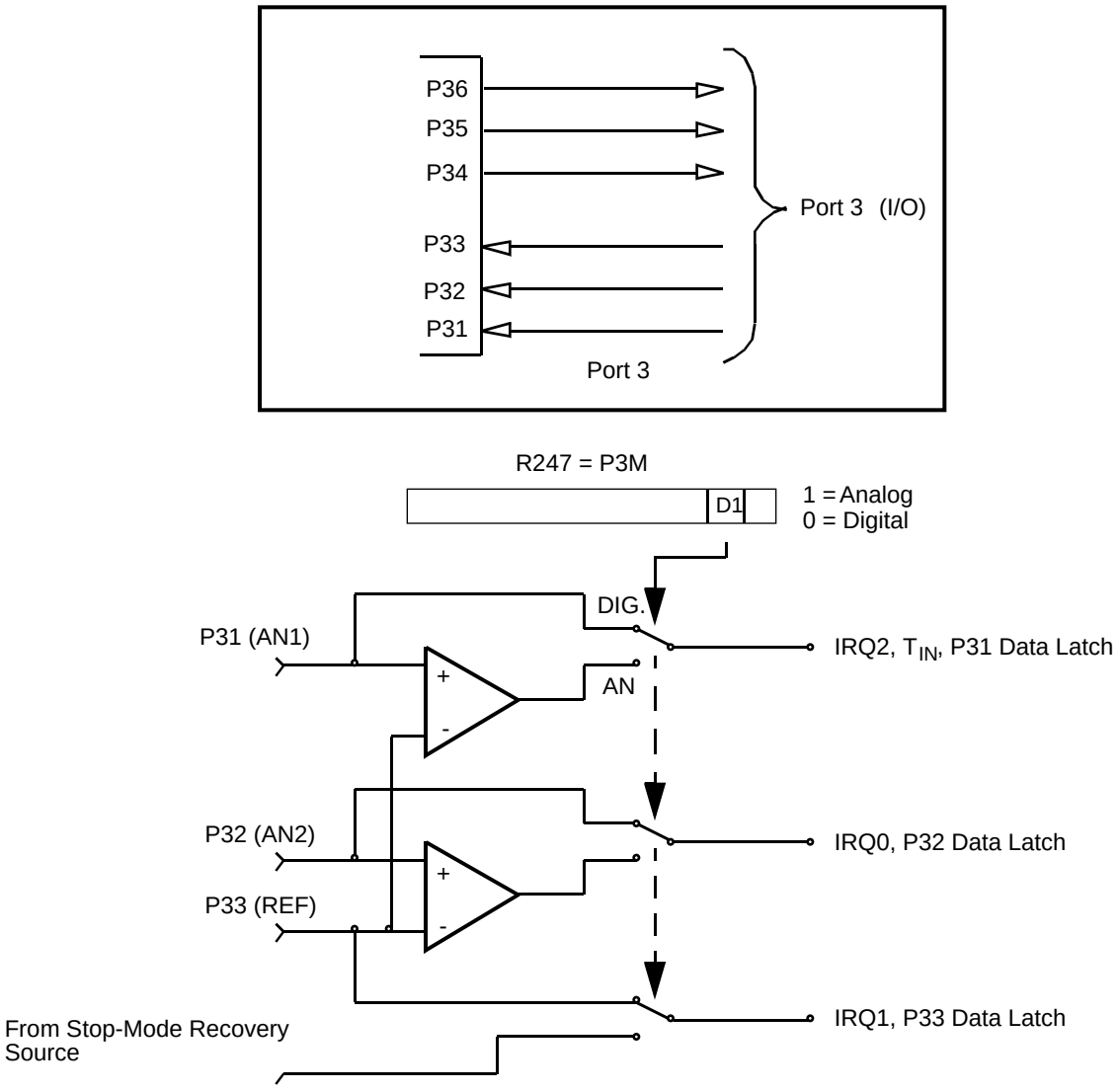


Figure 12. Port 3 Input Configuration

FUNCTIONAL DESCRIPTION (Continued)

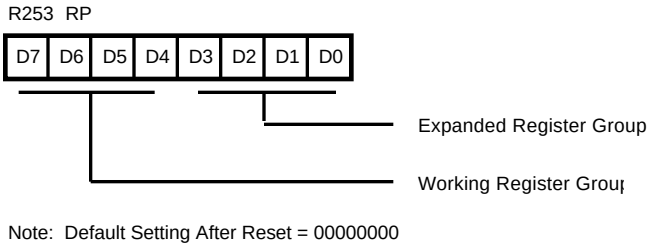


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

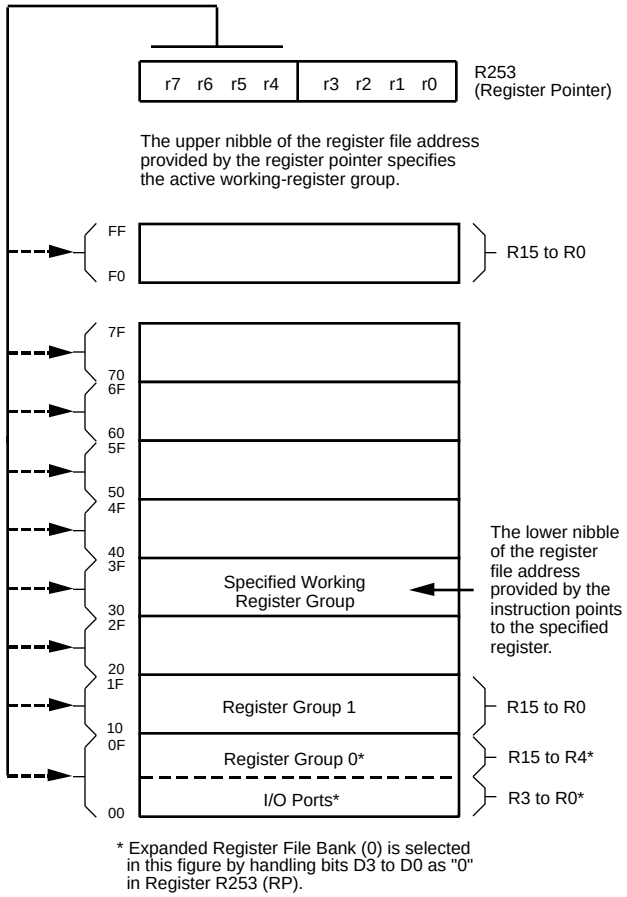


Figure 18. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

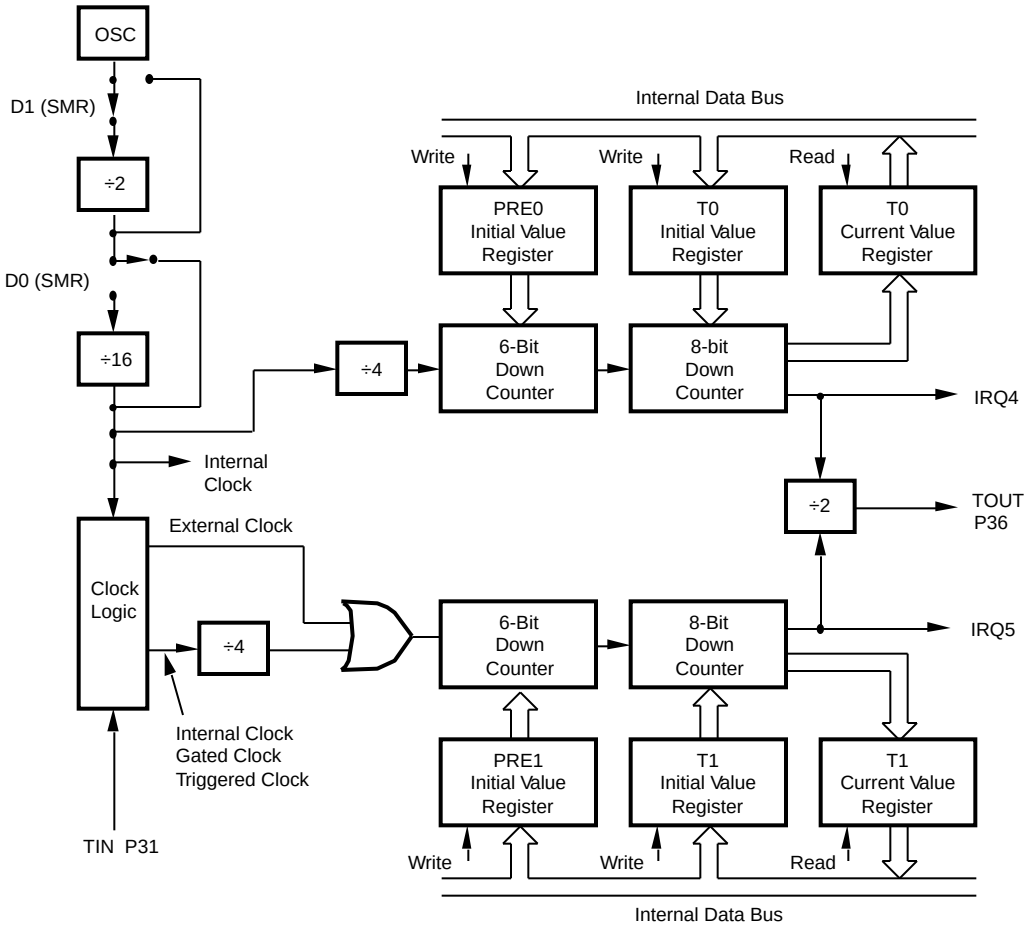


Figure 19. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

The D/A conversion for DAC1 is driven by writing 8-bit data to the DAC1 data register (Bank C, Register 06H). The D/A conversion for DAC2 is controlled by the DAC2 data register (Bank C, Register 07H). Each DAC data register is initialized to midrange 80H on power-up.

There are two DAC control registers: DACR1 (Bank C, Register 04H) for DAC1, and DACR2 (Bank C, Register 05H) for DAC2. Control register bits 0 and 1 set the DAC gain. When DAC data is 80H, the DAC output is constant for any gain setting (Figure 29 and Figure 31).

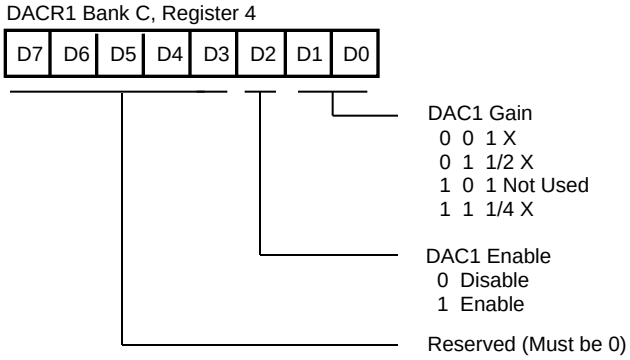


Figure 29. D/A 1 Control Register

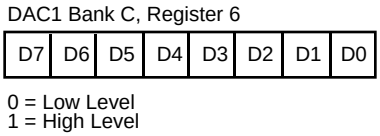


Figure 30. D/A 1 Data Register

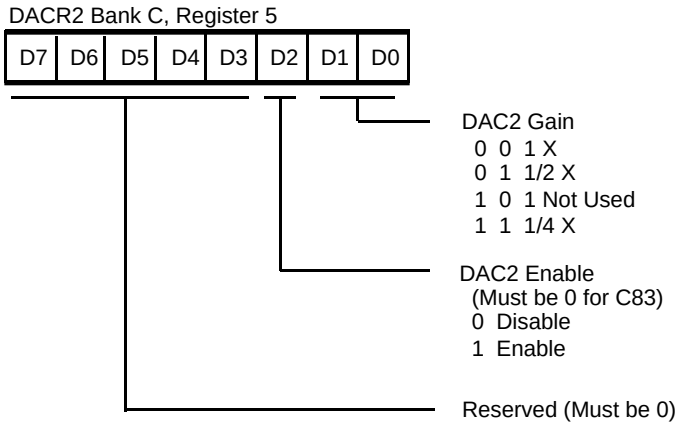


Figure 31. D/A 2 Control Register

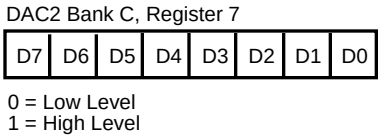


Figure 32. D/A 2 Data Register

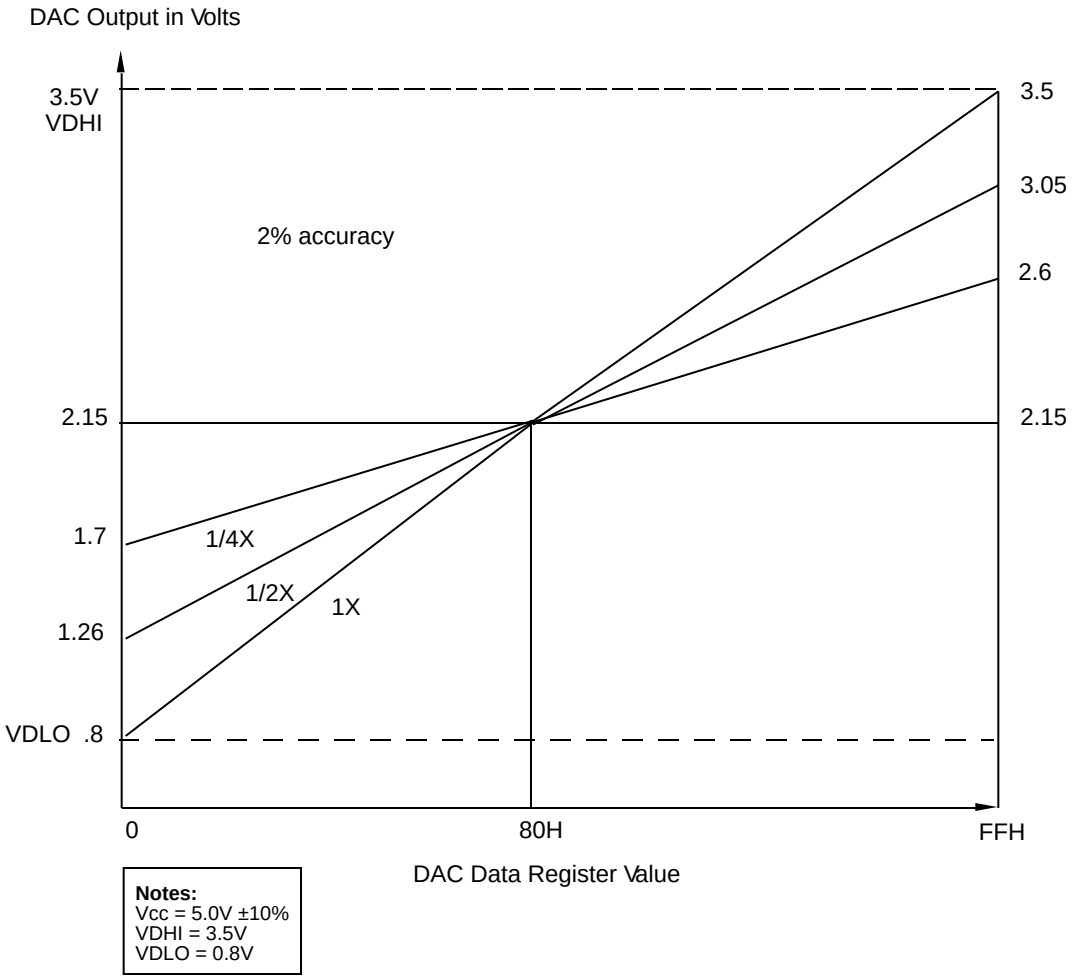


Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

Z8 CONTROL REGISTERS

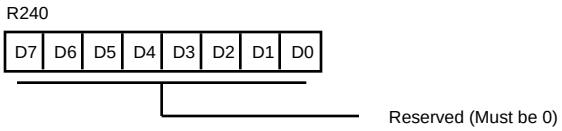


Figure 51. Reserved

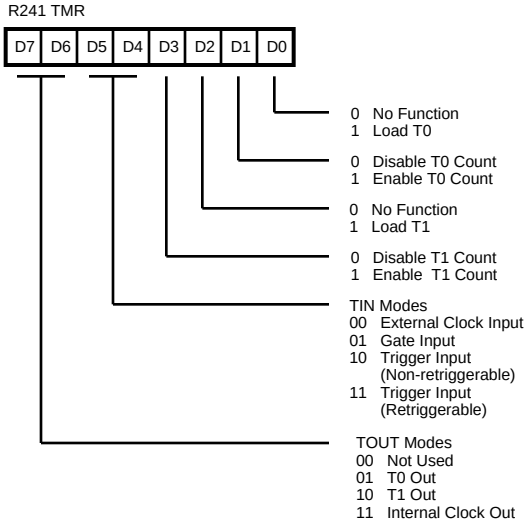


Figure 52. Timer Mode Register ($F1_H$: Read/Write)

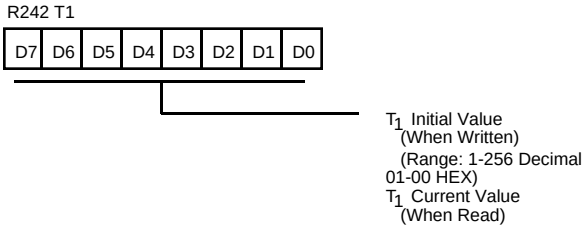


Figure 53. Counter/Timer 1 Register ($F2_H$: Read/Write)

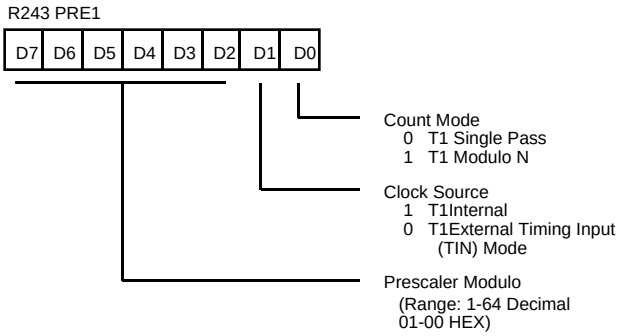


Figure 54. Prescaler 1 Register ($F3_H$: Write-Only)

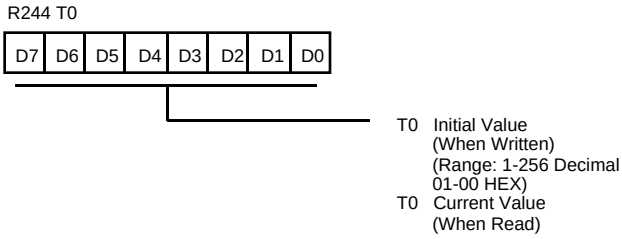


Figure 55. Counter/Timer 0 Register ($F4_H$: Read/Write)

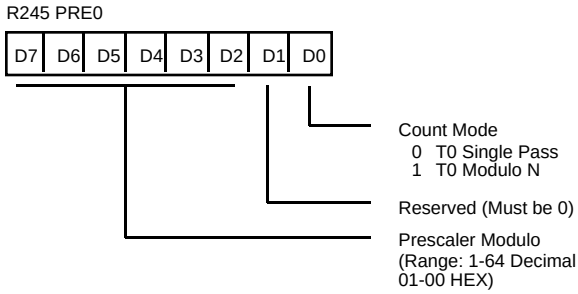


Figure 56. Prescaler 0 Register ($F5_H$: Write-Only)

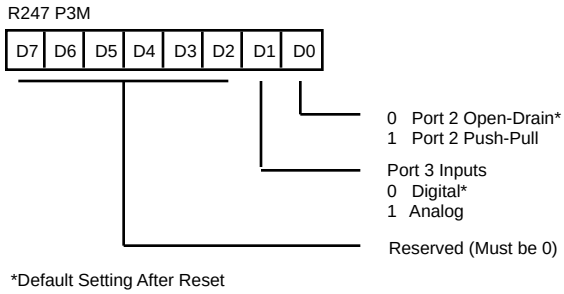
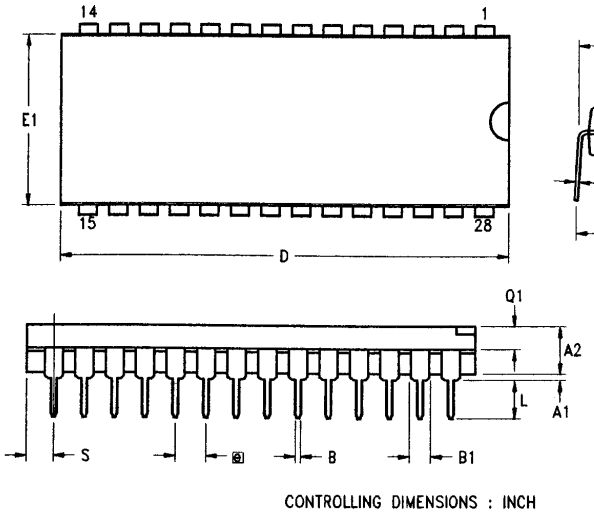


Figure 57. Port 3 Mode Register ($F7_H$: Write-Only)

PACKAGE INFORMATION



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C83 16 MHz			Z86E83 16 MHz		
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**	**28-Pin DIP**	**28-Pin SOIC**	**28-Pin PLCC**
Z86C8316PSC	Z86C8316SSC	Z86C8316VSC	Z86E8316PSC	Z86E8316SSC	Z86E8316VSC
Z86C8316PEC	Z86C8316SEC	Z86C8316VEC	Z86E8316PEC	Z86E8316SEC	Z86E8316VEC
Z86C84 16 MHz					
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**			
Z86C8416PSC	Z86C8416SSC	Z86C8416VSC			
Z86C8416PEC	Z86C8416SEC	Z86C8416VEC			

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to + 70°C
E = -40°C to +105°C

Speed

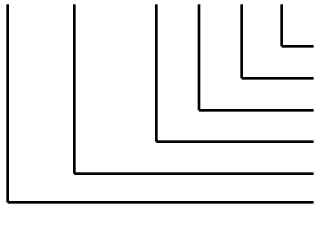
16 = 16 MHz

Environmental

C = Plastic Standard

Example:

Z 86C83 16 P S C is a Z86C83, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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