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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316vec00tr

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

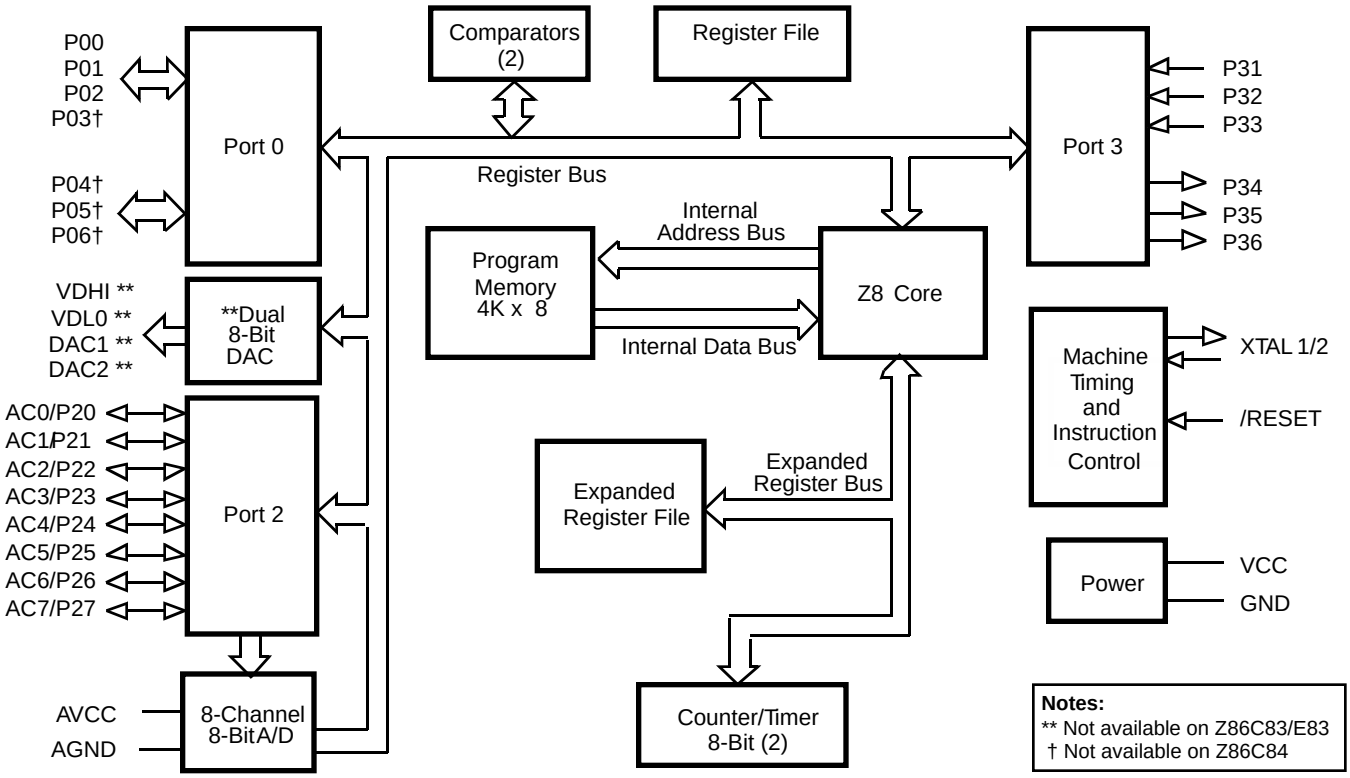


Figure 1. Z86C83/C84/E83 Functional Block Diagram

PIN DESCRIPTION (Continued)

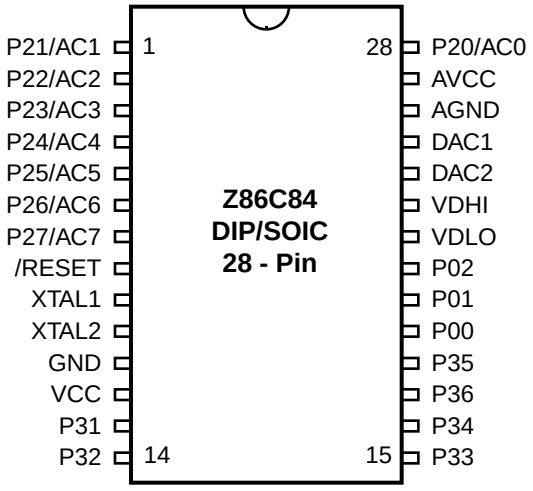


Figure 3. Z86C84 28-Pin DIP and SOIC Pin Configuration

Table 2. Z86C84 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-21	P00-P02	Port 0, Bits 0-3	Input/Output
22	VDLO	D/A Ref. Volt.,Low	Input
23	VDHI	D/A Ref. Volt.,High	Input
24-25	DAC2-1	D/A Converter	Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP, PLCC and SOIC Pin Description and Configuration are identical

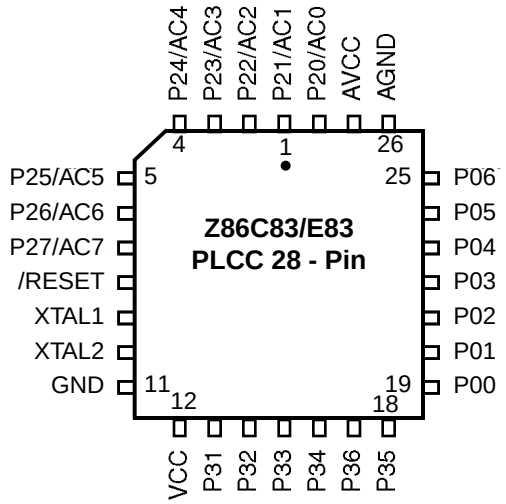


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

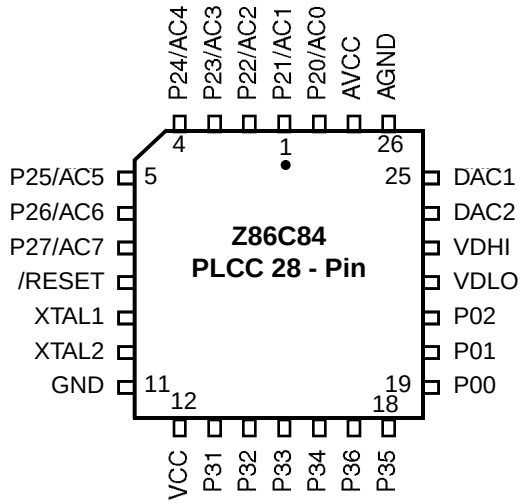


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

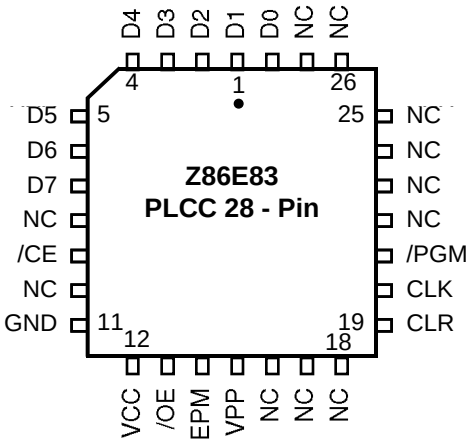


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 8).

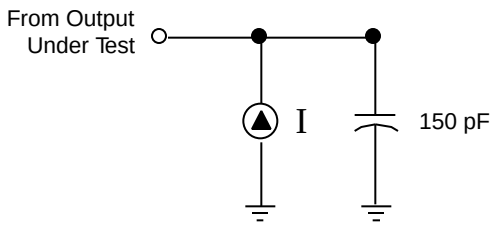


Figure 8. Test Load Diagram

V_{DD} SPECIFICATION

V_{DD} = 3.5V to 5.5V (Z86E83 only at 0° C to 70° C)

V_{DD} = 3.0V to 5.5V (Z86C83/C84)

V_{DD} = 4.5V to 5.5V (Z86E83 only at -40° C to 105° C)

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	15 pF
I/O capacitance	0	15 pF

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (SCLK/TCLK = XTAL/2) For Z86E83 Only

No	Symbol	Parameter	V_{CC} Note 6	T_A = 0°C to +70°C 12 MHz Min	12 MHz Max	16 MHz Min	16 MHz Max	Units	Notes
1	TpC	Input Clock Period	3.5V	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		15	ns	1
			5.5V		15		15	ns	1
3	TwC	Input Clock Width	3.5V	41		31		ms	1
			5.5V	41		31		ns	1
4	TwTinL	Timer Input Low Width	3.5V	100		100		ms	1
			5.5V	70		70		ns	1
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1
			5.5V	5TpC		5TpC			1
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1
			5.5V	8TpC		8TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1
	TfTin		5.5V		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2
			5.5V	70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3
			5.5V	5TpC		5TpC			1,3
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2
			5.5V	5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.5V	12		12		ns	
			5.5V	12		12		ns	
11	Tost	Oscillator Start-up Time	3.5V		5TpC		5TpC		4
			5.5V		5TpC		5TpC		4
12	Twdt	Watch-Dog Timer Delay Time					**WDTMR**	**Reg**	**D1,D0**
			5.5V	6.25		6.25		ms	0,0,[7]
			5.5V	12.5		12.5		ms	0,1,[7]
			5.5V	25		25		ms	1,0,[7]
			5.5V	100		100		ms	1,1,[7]
13	T_{POR}	Power On Reset Delay	3.5V	7	24	7	25	ms	7
			5.5V	3	13	3	14	ms	7

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 0.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 3.5V guarantees 3.5V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
7. Using internal on-board RC oscillator.

CAPACITANCE (Continued)

Additional Timing Table (SKLK/TCLK = XTAL/2) For Z86C83/C84 Only

				T_A = 0°C to +70°C				T_A = -40°C to +150°C					
			VCC	12 MHz		16MHz		12 MHz		16 MHz			
No	Sym	Parameter	[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		5TpC		5TpC		
			5.5V		5TpC		5TpC		5TpC		5TpC		
12	Twdt	Watch-Dog Timer Delay Time										WDTMR Reg	D1,D0
			5.5V	6.25		6.25		6.25		6.25		ms	0,0 [6]
			5.5V	12.5		12.5		12.5		12.5		ms	0,1 [6]
			5.5V	25		25		25		25		ms	1,0 [6]
			5.5V	100		100		100		100		ms	1,1 [6]
13	T_{POR}	Power On Reset Delay	3.0V	7	24	7	25	7	24	7	25	ms	6
			5.5V	3	13	3	14	3	13	3	14	ms	6

Notes:

1. Timing References used 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 0
5. The V_{CC} voltage specification of 3.0V guarantees 3.3V± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
6. Using internal on-board RC oscillator

For Z86E83

Table 8. A/D Converter Electrical Characteristics
V_{CC} = 3.5V

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	3.5			Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 9. A/D Converter Electrical Characteristics
V_{CC} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time	4.3		35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

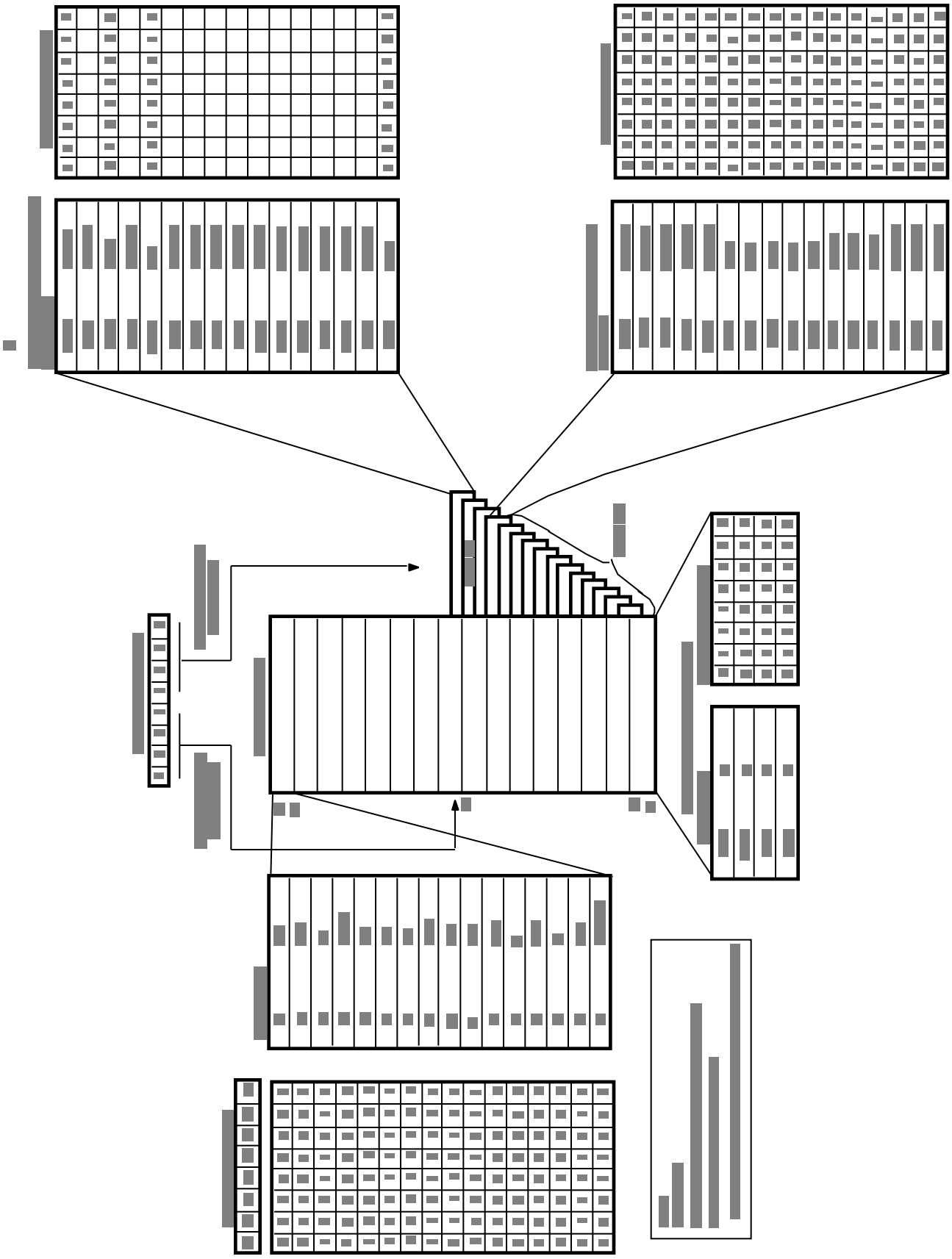


Figure 16. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

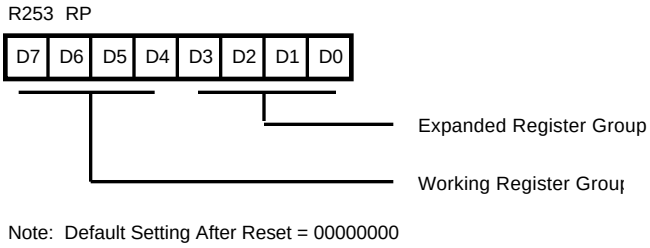


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

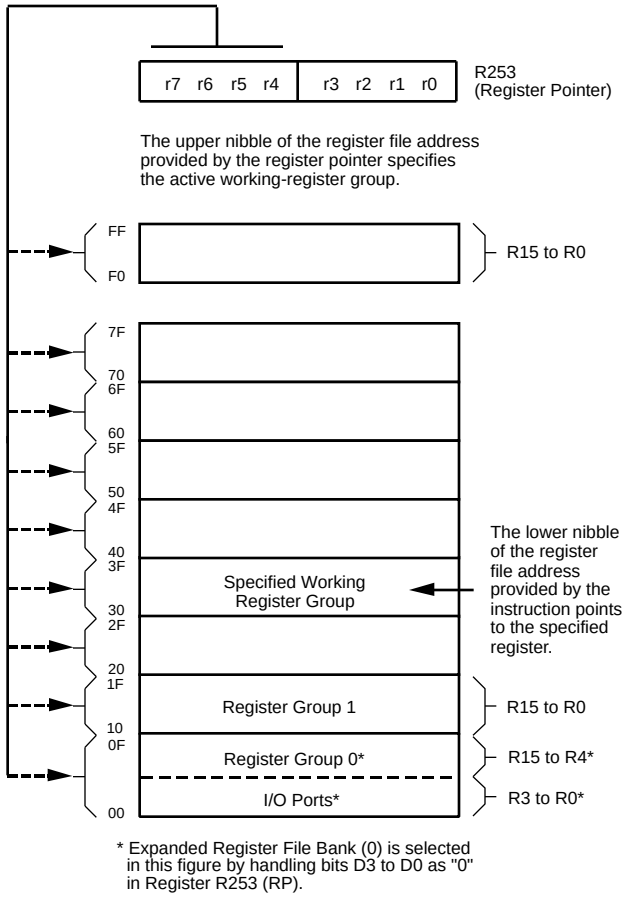


Figure 18. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

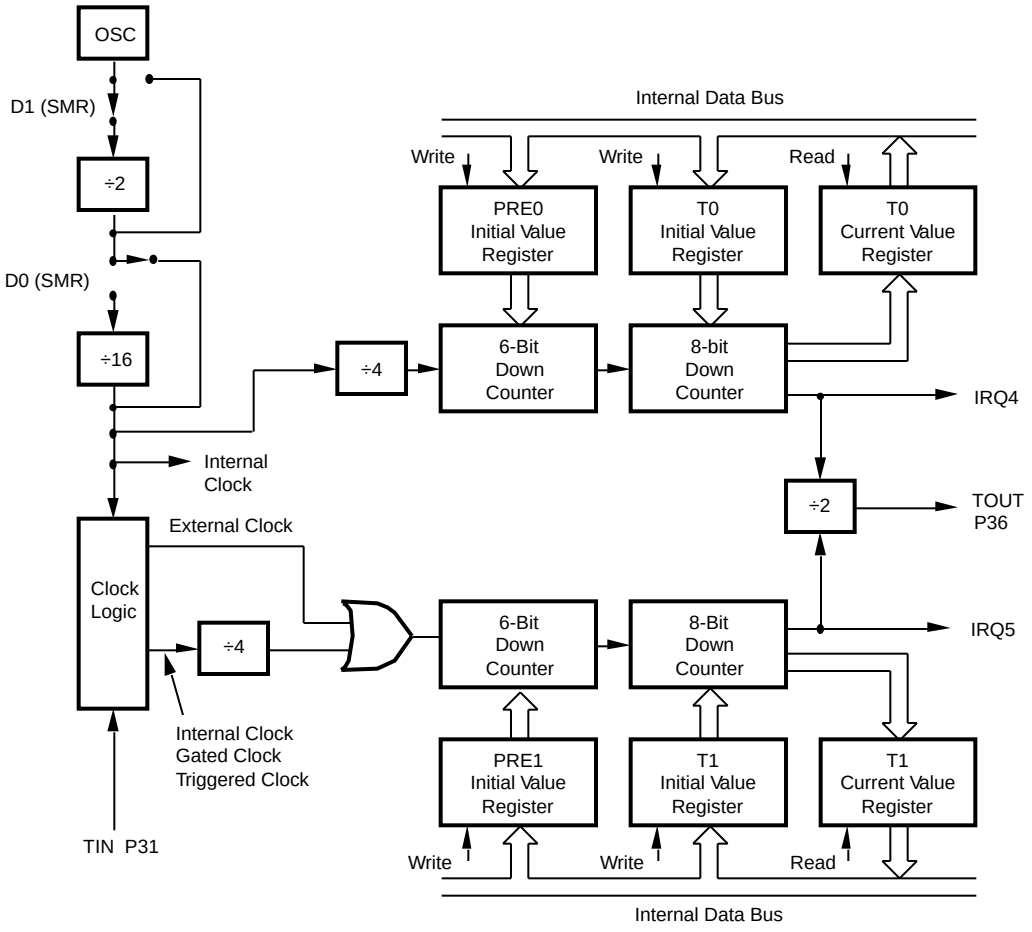


Figure 19. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

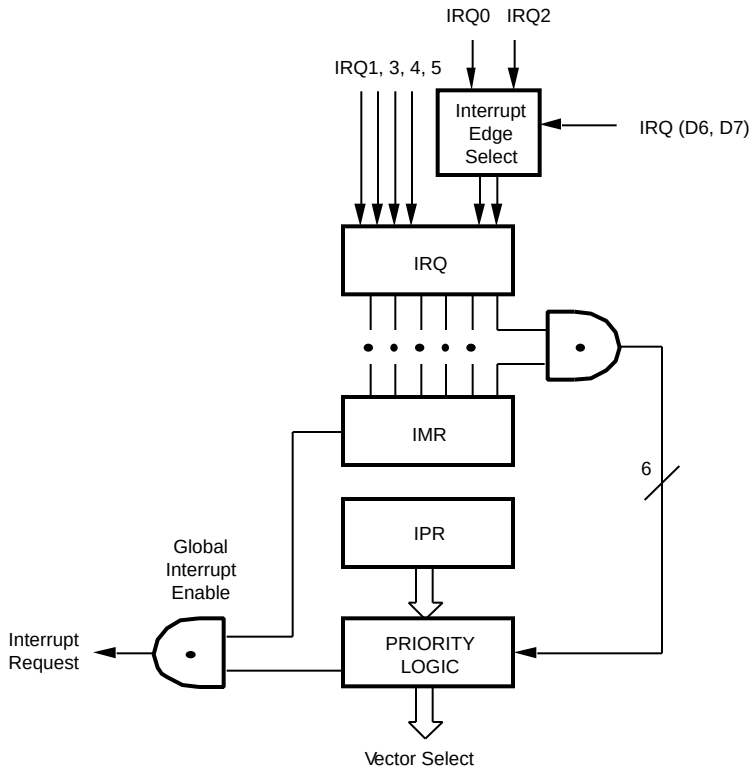


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

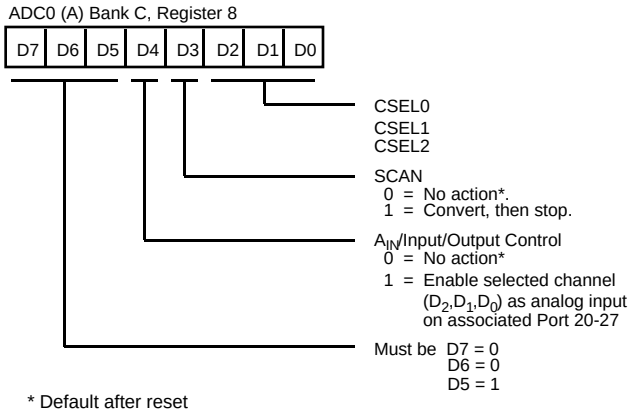


Figure 23. ADC Control Register 0 (Read/Write)

SCAN	
0	No action*
1	Convert channel then stop

Channel Select (bits 2, 1, 0)
* Default after reset

CSEL2	CSEL1	CSEL0	Channel
0	0	0	0 (P20)*
0	0	1	1 (P21)
0	1	0	2 (P22)
0	1	1	3 (P23)
1	0	0	4 (P24)
1	0	1	5 (P25)
1	1	0	6 (P26)
1	1	1	7 (P27)

Note: ADCO D4 must equal 1 to allow Port bit as ADC input.

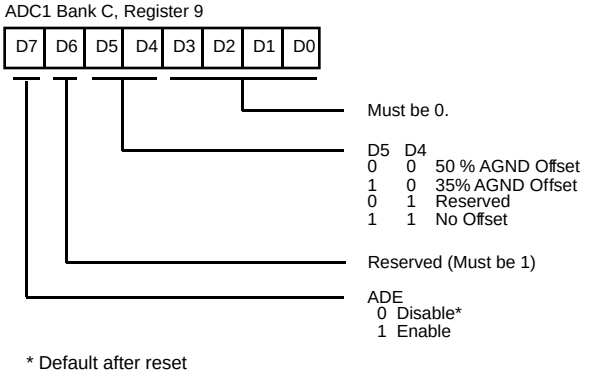


Figure 24. ADC Control Register 1 (Read/Write)

ADE (bit 7). A zero powers down and disables power and any A/D conversions or accessing any ADC registers except writing to ADE bit. A one Enables all ADC accesses. ADC result register is shown in Figure 25.

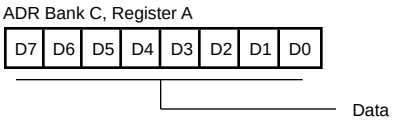


Figure 25. Result Register (Read-Only)

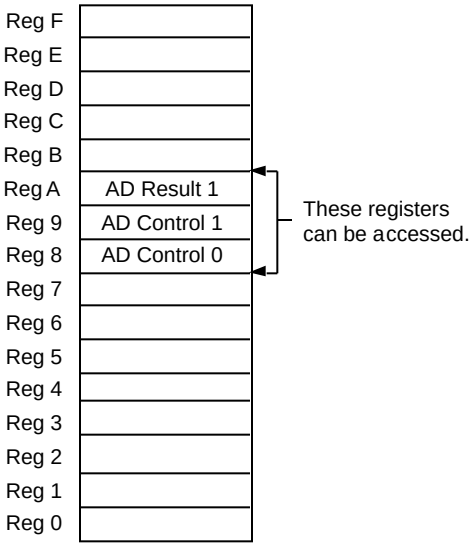


Figure 26. Bank C

Digital-to-Analog Converters

The Z86C84 has two Digital-to-Analog Converters (DACs). Each DAC is an 8-bit resistor string, with a programmable 0.25X, 0.5X, or 1X gain output buffer. The DAC output voltage settles after the internal data is latched into the DAC Data register. The top and bottom ends of the resistor ladder are register-selected to be connected to either the analog supply rails, AV_{CC} and A_{GND}, or two externally-provided reference voltages, VDHI and VDLO. External references are recommended to explicitly set the DAC output limits. Since the gain stage cannot drive to the supply rails, VDHI and VDLO must be within ranges shown in the specifications. If either reference approaches the analog supply rails, the output will be unable to span the reference voltage range. The externally provided reference voltages should not exceed the supply voltages. The DAC outputs are latch-up protected and can drive output loads (Figure 28).

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND

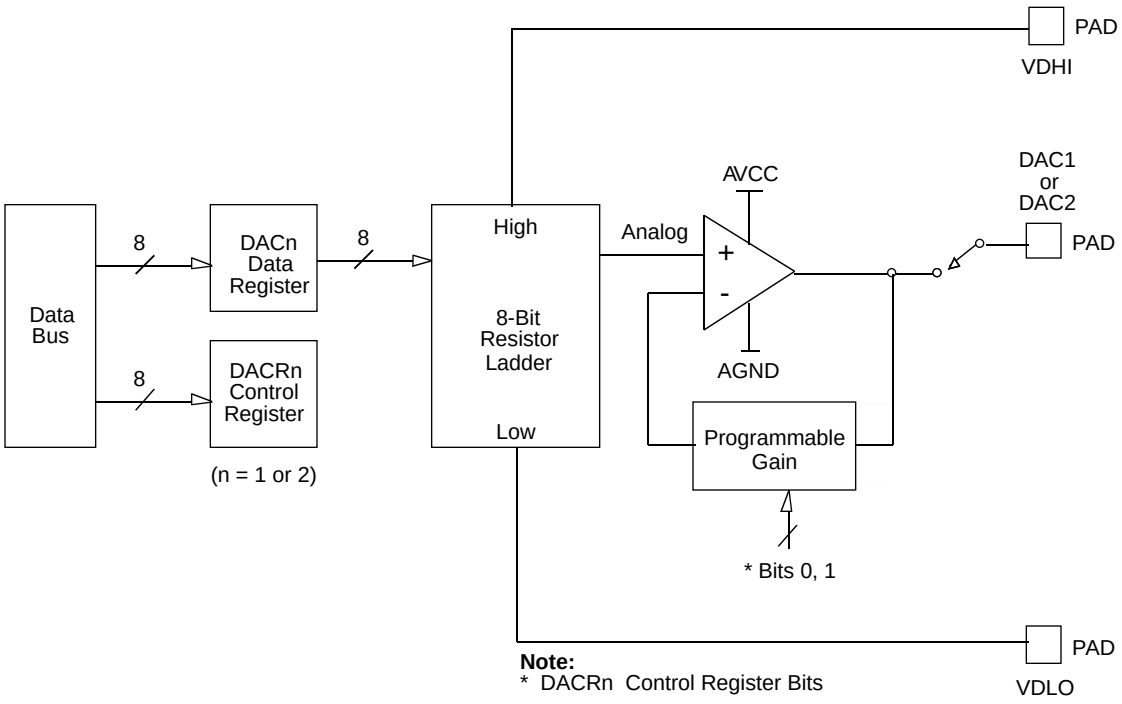


Figure 28. DAC Block Diagram

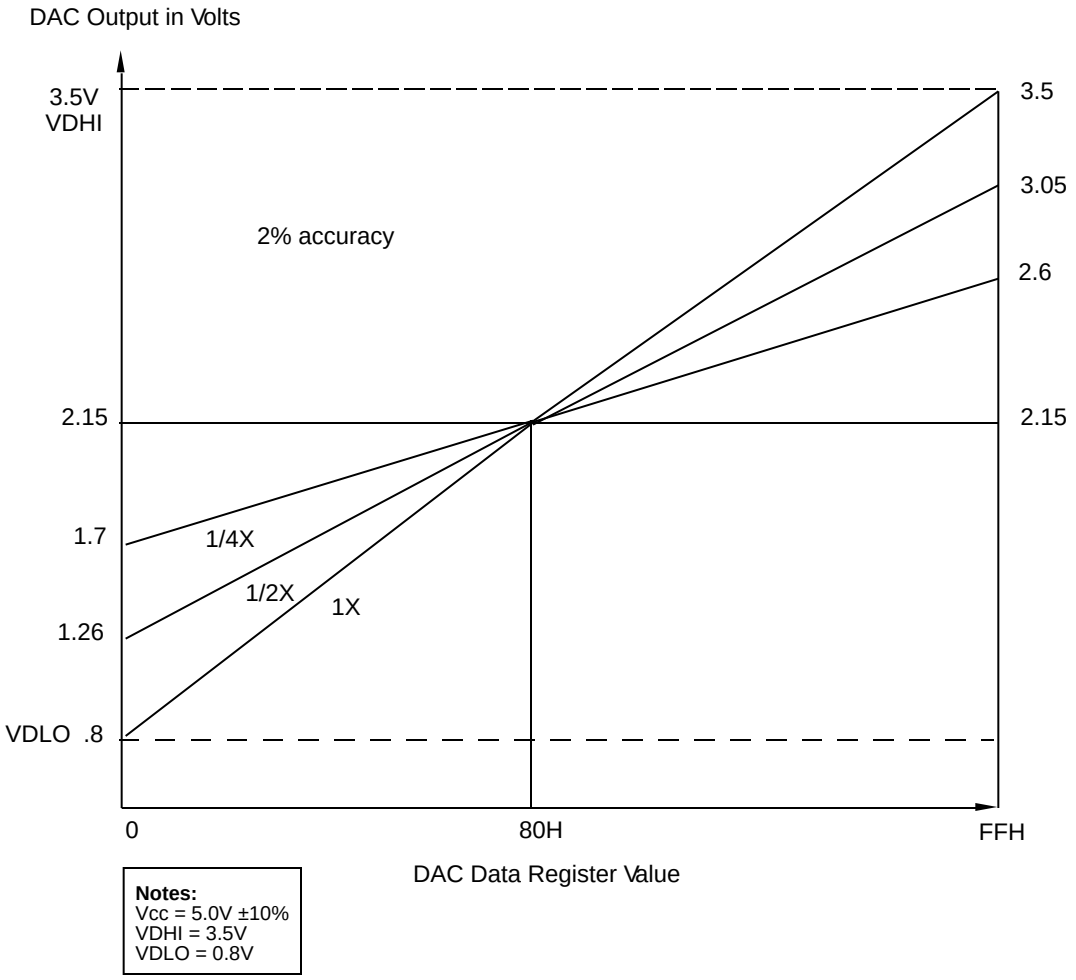


Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

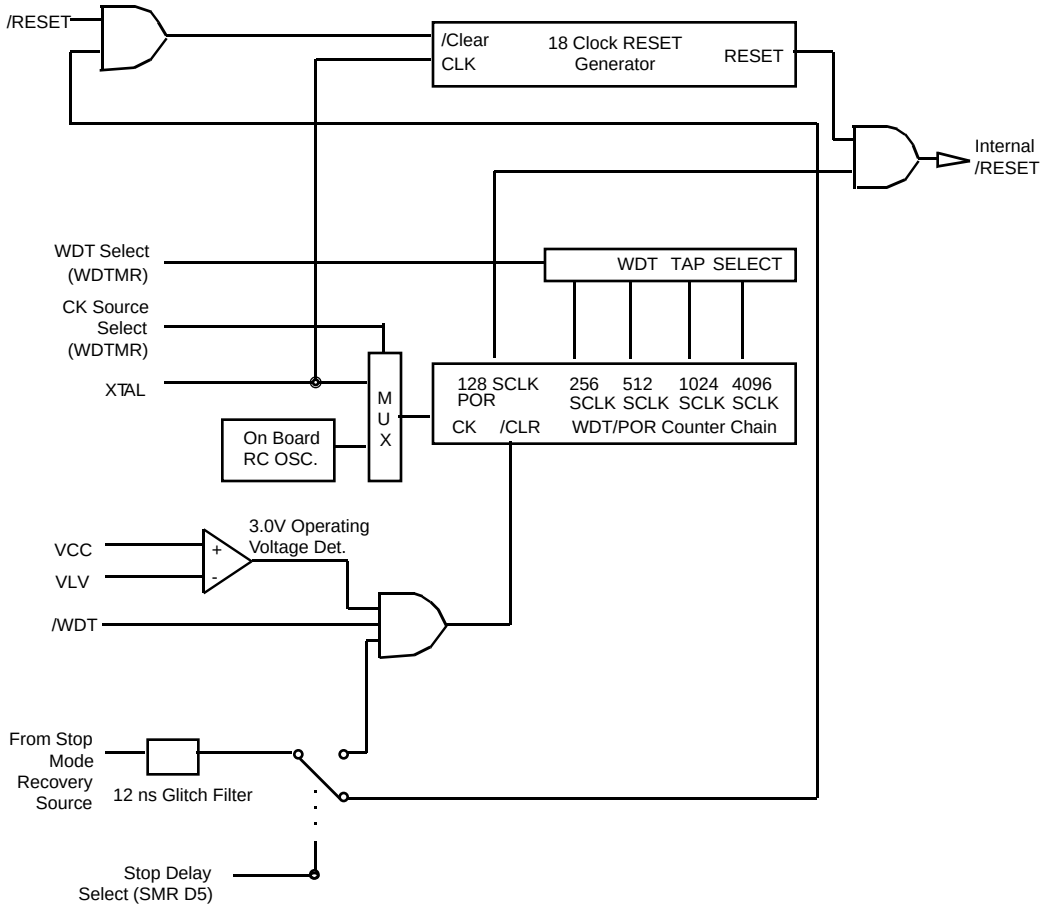


Figure 38. Resets and WDT

EXPANDED REGISTER FILE CONTROL REGISTERS (0C)

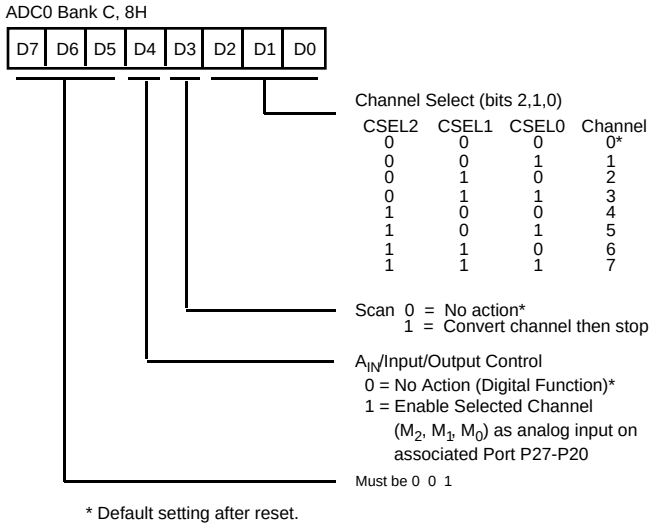


Figure 40. ADC Control Register 0 (Read/Write)

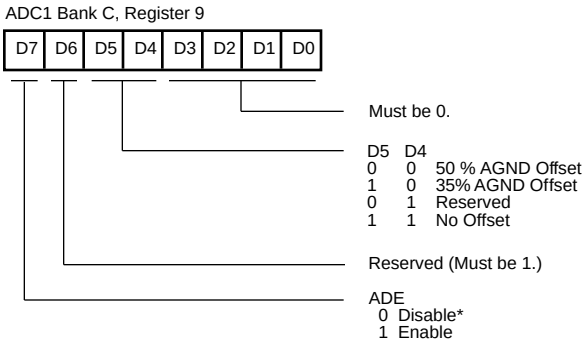


Figure 41. ADC Control Register 1 (Read/Write)

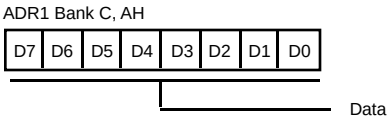


Figure 42. AD Result Register (Read Only)

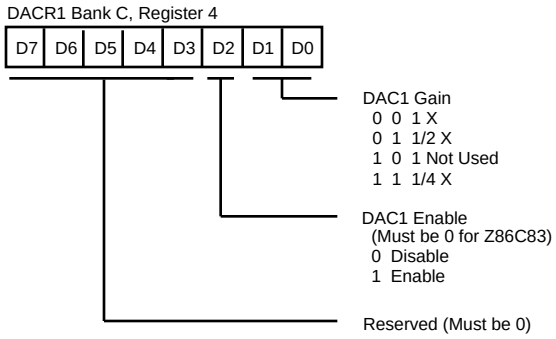


Figure 43. D/A 1 Control Register

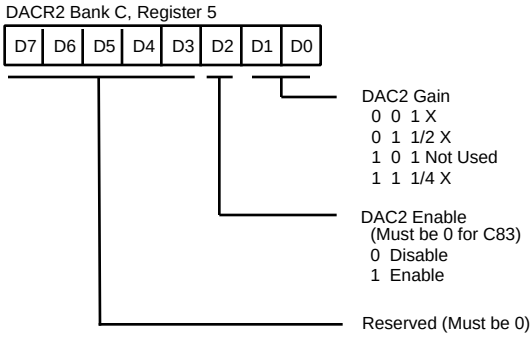


Figure 44. D/A 2 Control Register

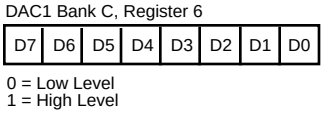


Figure 45. D/A 1 Data Register

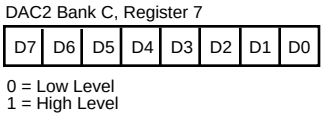


Figure 46. D/A 2 Data Register

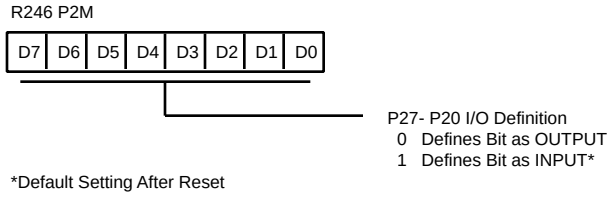


Figure 58. Port 2 Mode Register ($F6_H$: Write-Only)

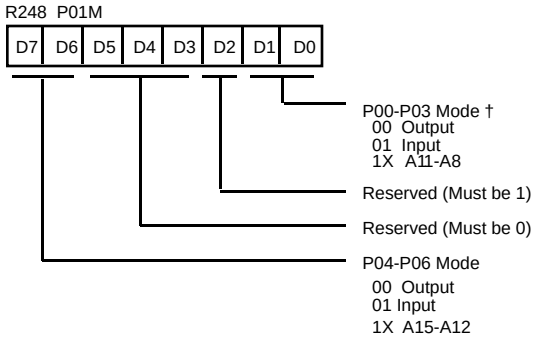


Figure 59. Port 0 and 1 Mode Register ($F8_H$: Write-Only)

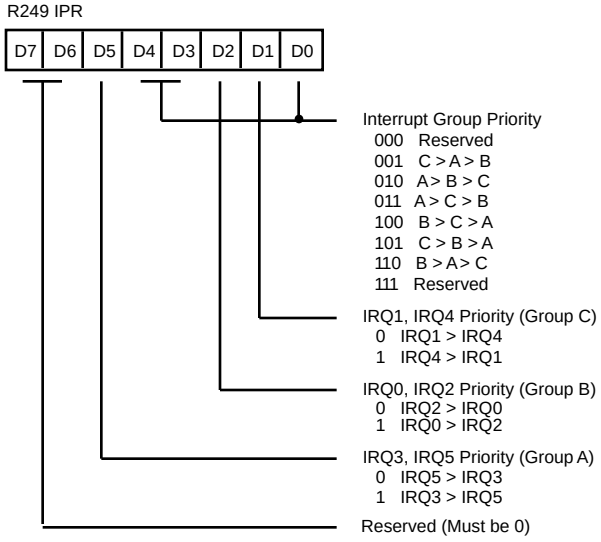


Figure 60. Interrupt Priority Register ($F9_H$: Write-Only)

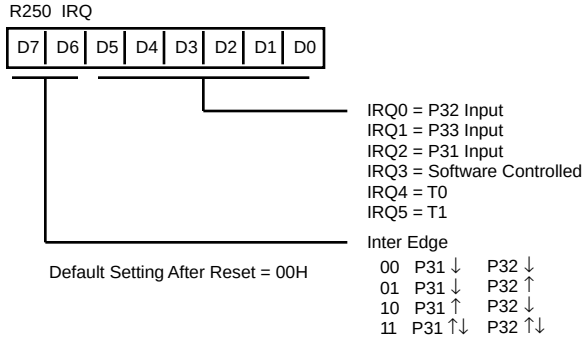


Figure 61. Interrupt Request Register (F_{AH}: Read/Write)

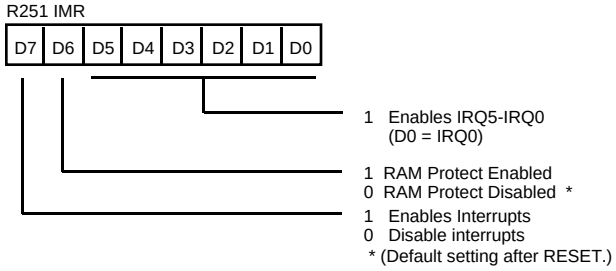


Figure 62. Interrupt Mask Register (F_{BH}: Read/Write)

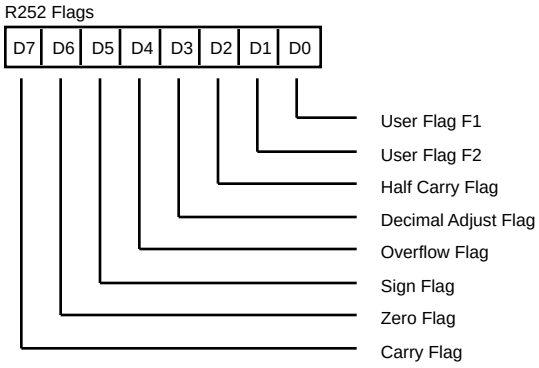
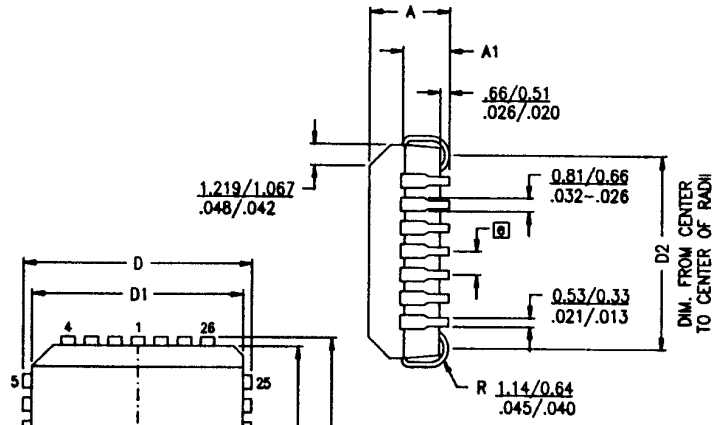


Figure 63. Flag Register (F_{CH}: Read/Write)

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
G	1.27 TYP		.050 TYP	

NOTES.
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 INCH.
3. DIMENSION : MM / INCH

Figure 70. 28-Pin PLCC Package Diagram

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