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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316vsc

PIN DESCRIPTION (Continued)

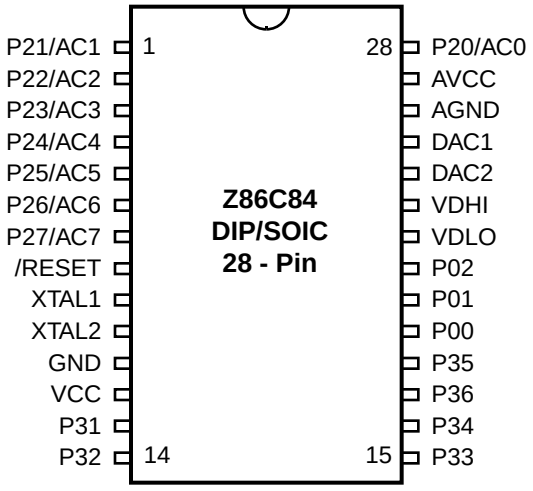


Figure 3. Z86C84 28-Pin DIP and SOIC Pin Configuration

Table 2. Z86C84 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-21	P00-P02	Port 0, Bits 0-3	Input/Output
22	VDLO	D/A Ref. Volt.,Low	Input
23	VDHI	D/A Ref. Volt.,High	Input
24-25	DAC2-1	D/A Converter	Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP, PLCC and SOIC Pin Description and Configuration are identical

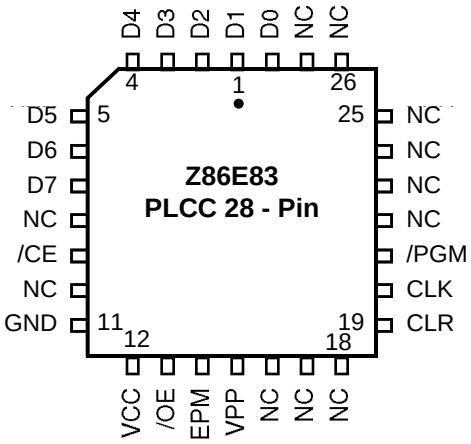


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

For Z86E83 Only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	Max	T_A = -40° C to +105° C Min	Max	Typical [13] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Ouput High Voltage	3.5V	V_{CC}-0.4				3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.5V		0.6			0.2	V	I_{OH} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OH} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2			0.3	V	I_{OH} = +6.0 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OH} = +10.0 mA	8
V_{RH}	Reset Input High Voltage	3.5V	0.8V_{CC}	V_{CC}			1.5	V		
		5.5V	0.8V_{CC}	V_{CC}	0.8V_{CC}	V_{CC}	2.1	V		
		3.5V	GND-0.3	0.2V_{CC}			1.1	V		
		5.5V	GND-0.3	0.2V_{CC}	GND-0.3	0.2V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25			10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V		-130			-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.5V		20			7	mA	@16 MHz	1,4
		5.5V		25		25	20	mA	@16 MHz	1,4
I_{CC1}	Standby Current (HALT Mode)	3.5V		4.5			2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		3.5V		3.4			1.5	mA	Clock divide by 16 @ 16 MHz	1,4
		5.5V		7.0		7.0	2.9	mA	Clock divide by 16 @ 16 MHz	1,4

CAPACITANCE (Continued)

Additional Timing Table (SKLK/TCLK = XTAL/2) For Z86C83/C84 Only

				T_A = 0°C to +70°C				T_A = -40°C to +150°C					
			VCC	12 MHz		16MHz		12 MHz		16 MHz			
No	Sym	Parameter	[6]	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
			5.5V	83	DC	62.5	DC	83	DC	62.5	DC	ns	1
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		15		15		15		15	ns	1
			5.5V		15		15		15		15	ns	1
3	TwC	Input Clock Width	3.0V	41		31		41		31		ns	1
			5.5V	41		31		41		31		ns	1
4	TwTinL	Timer Input Low Width	3.0V	100		100		100		100		ns	1
			5.5V	70		70		70		70		ns	1
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		5TpC		5TpC			1
			5.5V	5TpC		5TpC		5TpC		5TpC			1
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC		8TpC		8TpC			1
			5.5V	8TpC		8TpC		8TpC		8TpC			1
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100		100		100	ns	1
			5.5V		100		100		100		100	ns	1
8A	TwIL	Int. Request Low Time	3.0V	100		100		100		100		ns	1,2
			5.5V	70		70		70		70		ns	1,2
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,3
			5.5V	5TpC		5TpC		5TpC		5TpC			1,3
9	TwIH	Int. Request High Time	3.0V	5TpC		5TpC		5TpC		5TpC			1,2
			5.5V	5TpC		5TpC		5TpC		5TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		12		12		ns	
			5.5V	12		12		12		12		ns	
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		5TpC		5TpC		
			5.5V		5TpC		5TpC		5TpC		5TpC		
12	Twdt	Watch-Dog Timer Delay Time										WDTMR Reg	D1,D0
			5.5V	6.25		6.25		6.25		6.25		ms	0,0 [6]
			5.5V	12.5		12.5		12.5		12.5		ms	0,1 [6]
			5.5V	25		25		25		25		ms	1,0 [6]
			5.5V	100		100		100		100		ms	1,1 [6]
13	T_{POR}	Power On Reset Delay	3.0V	7	24	7	25	7	24	7	25	ms	6
			5.5V	3	13	3	14	3	13	3	14	ms	6

Notes:

1. Timing References used 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 0
5. The V_{CC} voltage specification of 3.0V guarantees 3.3V± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
6. Using internal on-board RC oscillator

PIN FUNCTIONS (Continued)

Port 2 (P27-P20) Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port and an 8-channel muxed input to the 8-bit ADC. When configured as a digital input, by programming the Port2 Mode register, the Port 2 register can be evaluated to read digital data applied to Port 2, or the ADC result register can be read to evaluate the analog signals applied to Port 2 after configuring the ADC Control Registers. The direction of each of the eight Port 2 I/O lines can be configured individually (Figure 11).

In addition, all four versions of the device provide the capability of connecting 10K (±20%) pull-up resistors to each of the Port 2 I/O lines individually. The pull-ups are connected when activated through software control of P2RES register (Figure 67) when the corresponding Port 2 pin is configured to be an input. The pull-up resistor of a Port 2 I/O line is automatically disabled when the corresponding I/O is an output, regardless of the state of the corresponding P2RES bit value.

Note: The Z86C83/C84 Emulator does not emulate the P2RES Register. Selection of the pull-ups are done via jumper settings on the emulator.

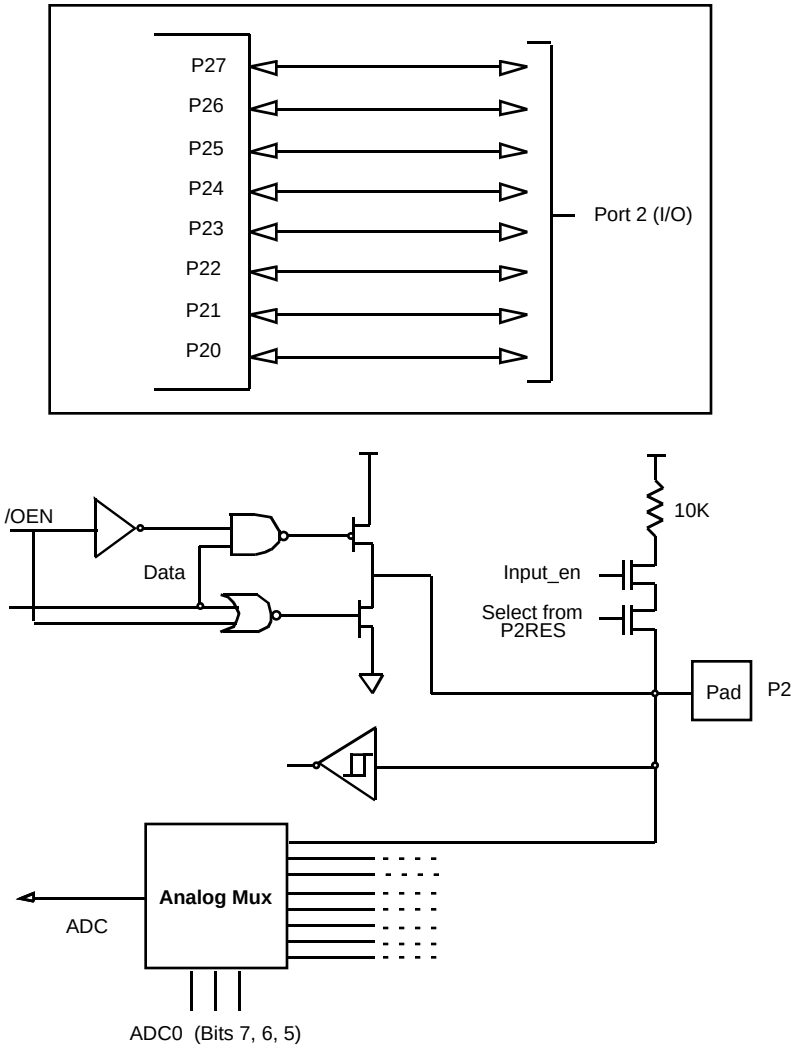


Figure 11. Port 2 Configuration

Port 3 (P36-P31) Port 3 is a 6-bit, CMOS-compatible port, with three fixed inputs (P33-P31) and three fixed outputs (P34-P36), configured under software control for Input/Output, Counter/Timers, interrupt, and port handshake. P31, P32, and P33 are standard CMOS inputs (no Auto Latches). Pins P34, P35, and P36 are push-pull output lines (Figure 11). Low EMI output buffers can be globally programmed by the software.

Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M bit 1). For Interrupt functions, Port 3, pin 3 is falling-edge interrupt input. P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and bit 7). P33 is the comparator reference voltage input when in Analog Mode. Access to Counter/Timers 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P31/P36 and P32/P35 (Table 10).

Port 3 also provides the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); timer input and output signals (T_{IN} and T_{OUT}).

Table 10. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D

Notes:
HS = Handshake Signals
D = /DAV
R = RDY

Auto Latch. The Auto-Latch instruction puts valid CMOS levels on CMOS inputs that are not externally driven. Whether this level is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Note: Pins 03, 04, 05, 06 have permanently enabled Auto Latches.

Comparator Inputs. Port 3, P31 and P32, each have a comparator front end. The comparator reference voltage, P33, is common to both comparators. In analog mode, the P33 input functions as a reference voltage to the comparators. In Analog Mode, the internal P33 register and its corresponding IRQ1 is connected to the Stop-Mode Recovery source selected by the SMR register. In this mode, any of the Stop-Mode Recovery sources are used to toggle the P33 bit or generate IRQ1. In Digital Mode, P33 can be used as a Port 3 register input or IRQ1 source. P34 outputs the comparator outputs by software programming the PCON Register bit D0 to 1.

Note: When enabling/or disabling the analog mode, the following is recommended:

1. allow two NOP delays before reading the comparator output

2. disable interrupts, switch to analog mode, clear interrupts, and then re-enable interrupts.

Port Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 13).

Bit 0 multiplexes comparator AN1 Output at P34. A "1" in this location brings the comparator output to P34 (Figure 14), and a "0" puts P34 into its standard I/O configuration.

Note: Only comparator output AN1 is multiplexed to a Port 3 output. Comparator AN2 output is not connected to any pins. Note that the PCON Register is reset upon the occurrence of a WDT RESET (not in STOP Mode), and Power-On Reset (POR).

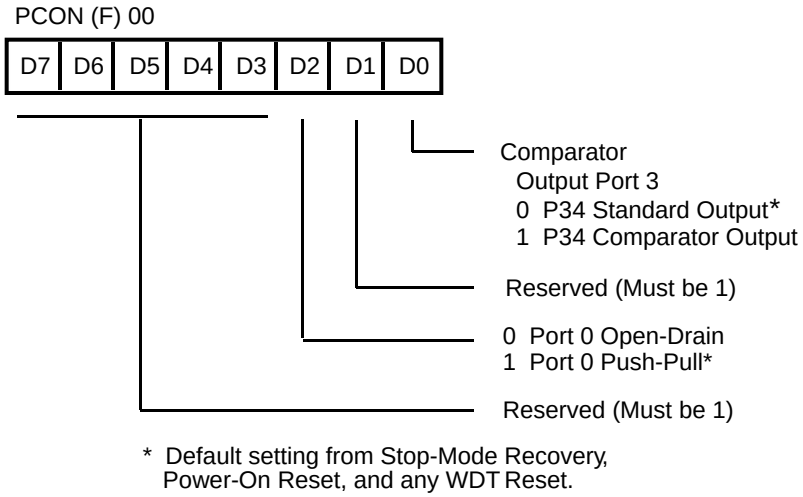


Figure 13. Port Configuration Register (PCON) (Write-Only)

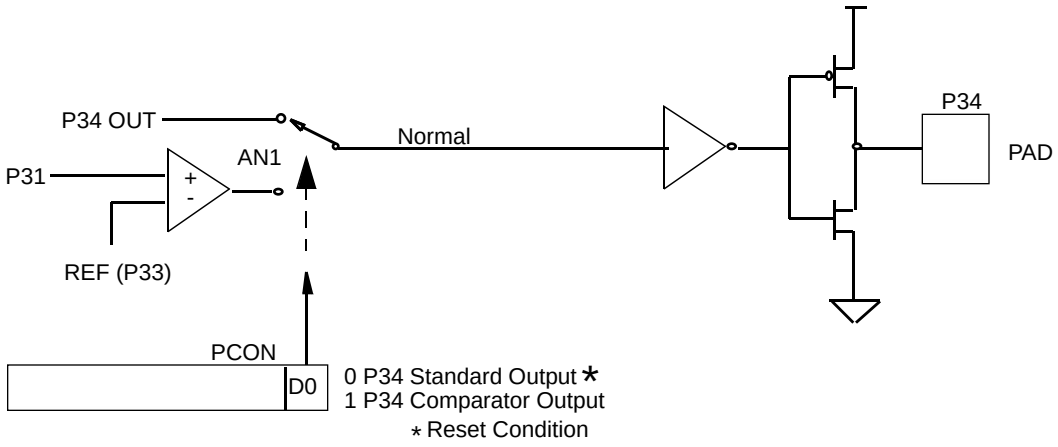


Figure 14. Port 3 P34 Output Configuration

FUNCTIONAL DESCRIPTION (Continued)

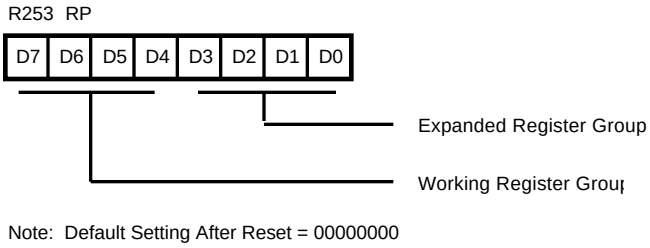


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

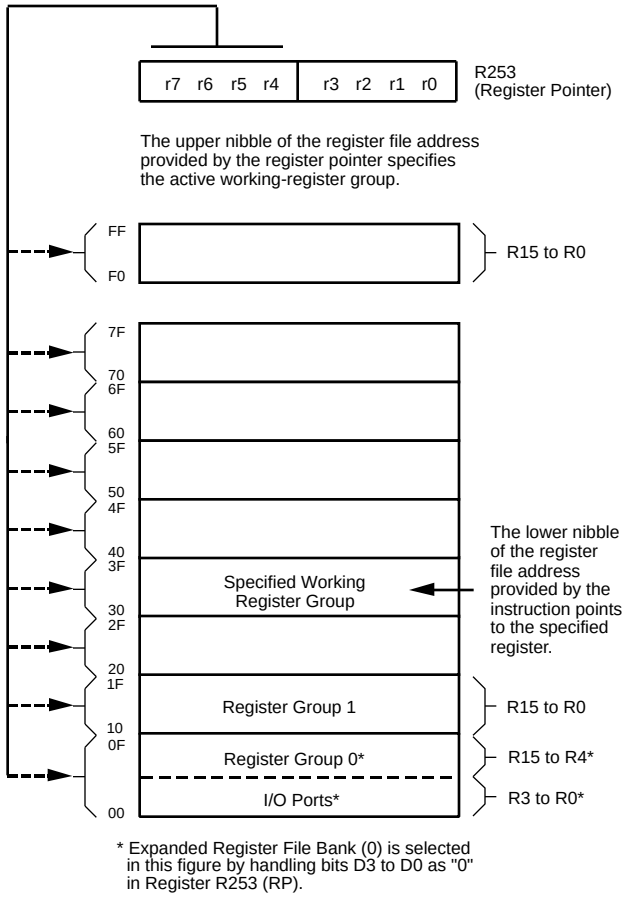


Figure 18. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 19).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, **but not the prescalers**, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divide-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

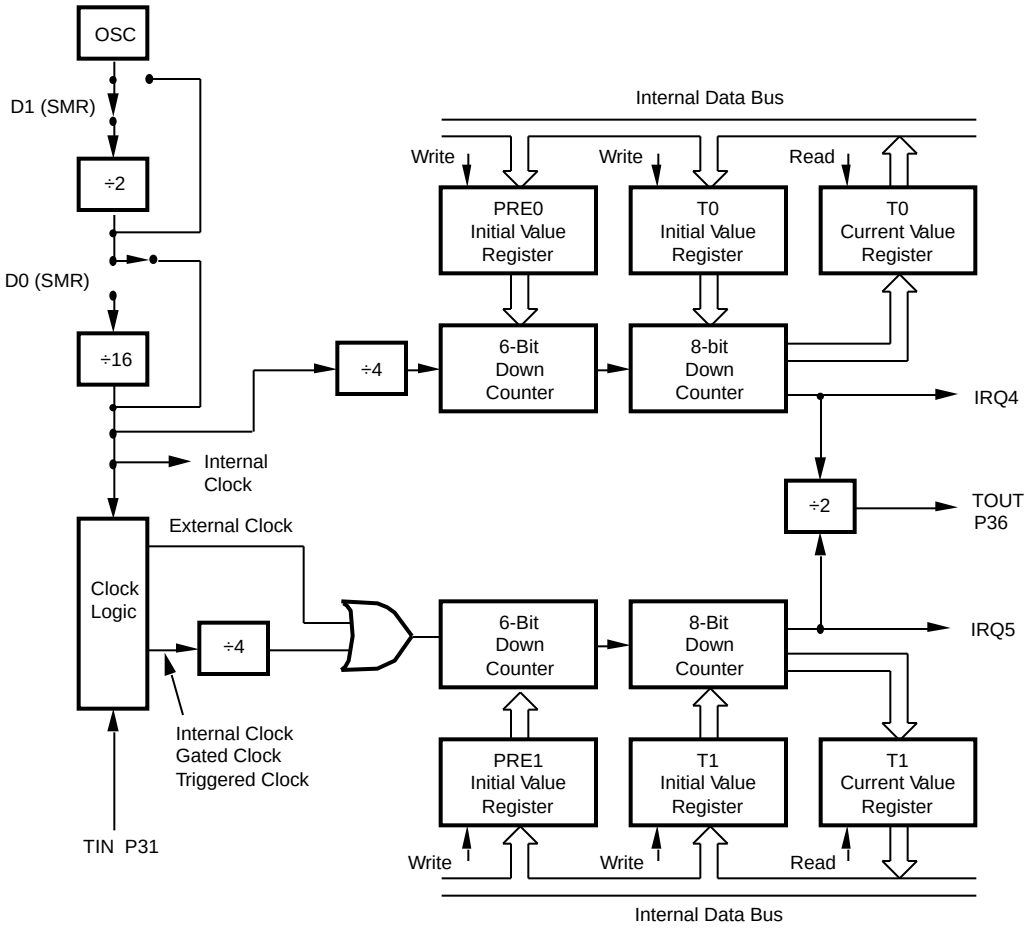


Figure 19. Counter/Timer Block Diagram

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 12.

Table 12. IRQ Register

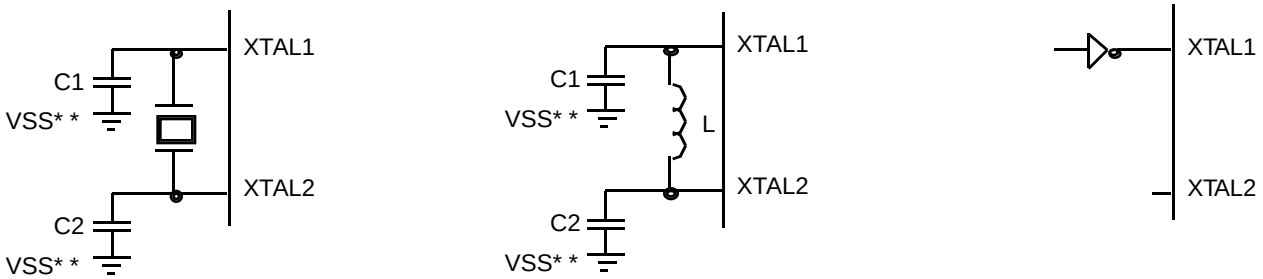
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when clocking from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator (Figure 21).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 21. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Analog-to-Digital Converter

The Analog-to-Digital (ADC) is an 8-bit half flash converter that uses two reference resistor ladders for its upper 4 bits (MSBs) and lower 4 bits (LSBs) conversion. Two reference voltage pins, AV_{CC} and A_{GND}, are provided for external reference voltage supplies. During the sampling period from one of the eight channel inputs, the converter is also being auto-zeroed before starting the conversion. The conversion time is dependent on the internal clock frequency. The minimum conversion time is 35 x SCLK (see Figure 22).

The ADC is controlled by the Z8 and its three registers (two Control and one Result) are mapped into the Extended Register File. A conversion can be initiated by writing to the ADC Control Register 0 after the ADC Control Register 1 is configured.

The start command is implemented in such a way as to begin a conversion at any time, if a conversion is in progress and a new start command is received, then the conversion in progress will be aborted and a new conversion will be initiated. This allows the programmed values to be changed without affecting a conversion-in-progress. The new values will take effect only after a new start command is received.

The ADC can be disabled (for low power) or enabled by a Control Register bit.

Though the ADC will function for a smaller input voltage and voltage reference, the noise and offsets remain constant over the specified electrical range. The errors of the converter will increase and the conversion time may also take slightly longer due to smaller input signals.

ADC Calibration Offset

Specially matched resistors are program-enabled to allow 35 percent or 50 percent offset from A_{GND}. They may selectively enable these resistors to offset the A_{GND} by 50 percent (2.5V to 5V) or 35 percent (1.75V to 5V) thereby allowing the 8-bit ADC across a narrower voltage range. This will allow significant resolution improvement within the reduced voltage range.

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND.

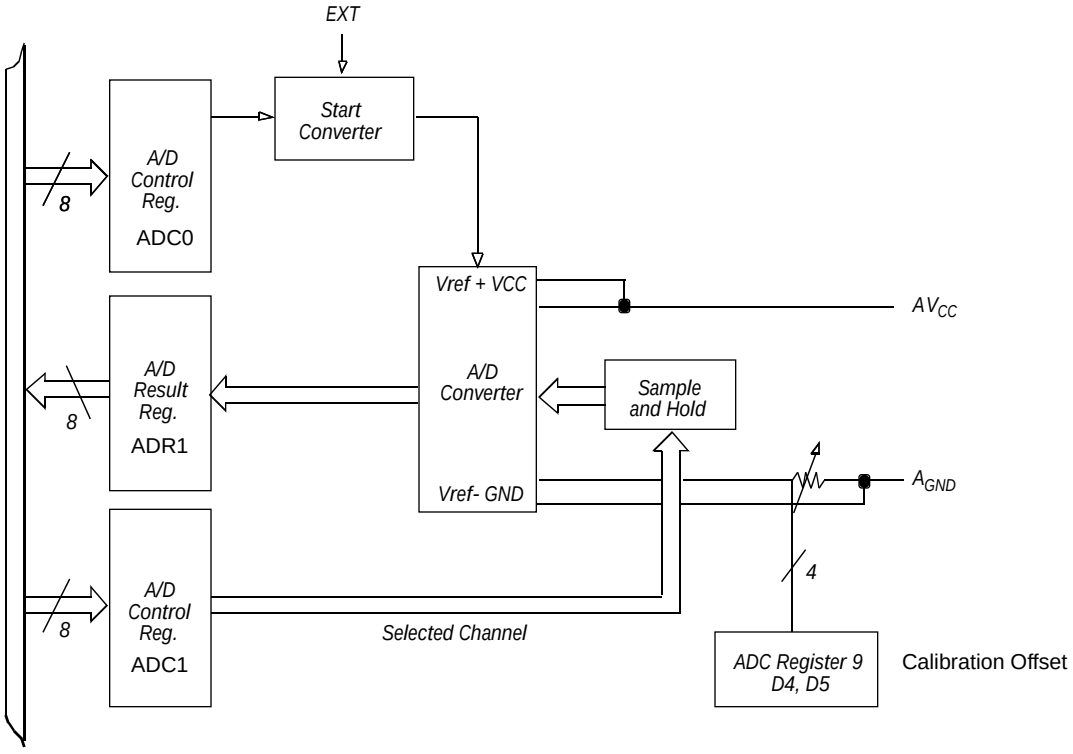


Figure 22. ADC Architecture

FUNCTIONAL DESCRIPTION (Continued)

Figure 27 shows the input circuit of the ADC. When conversion starts the analog input voltage is connected to the MSB and LSB flash converter inputs as shown in the Input Impedance CKT diagram. Effectively, shunting 31 parallel internal resistance of the analog switches and simultaneously charging 31 parallel 0.5 pF capacitors, which is equivalent to seeing a 400 Ohms input impedance in parallel with a 16 pF capacitor. Other input stray capacitance adds about 10 pF to the input load. For input source resistances up to 2 Kohms can be used under normal operating condition without any degradation of the input settling time. For larger input source resistance, increasing conversion cycle time or adding a capacitor to the input may be required to compensate the input settling time problem.

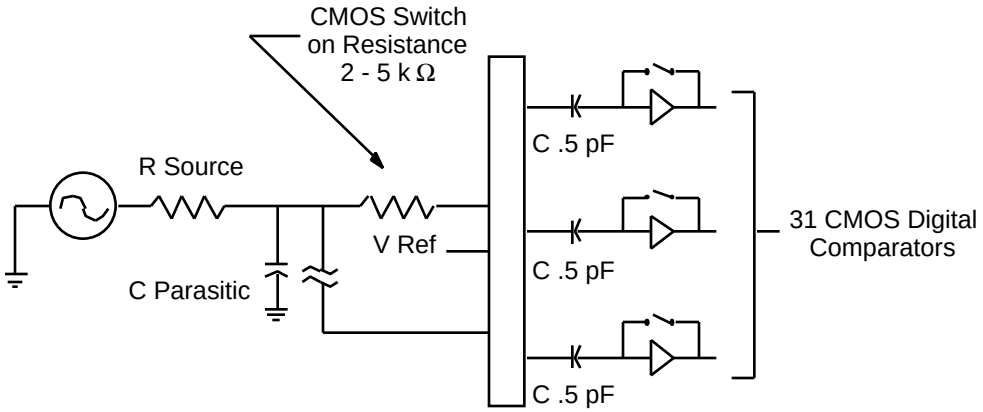


Figure 27. Input Impedance of ADC

Typical Z8 A/D Conversion Sequence

3. Set the register pointer to Extended Bank (C), that is, SRP #%0C instruction.

4. Next, set ADE flag by loading ADC1 Control Register Bank (C) Register 9, bit 7. Also, load bits 0-4 of this same register to select a AV_{CC} or A_{GND} offset value. A precision voltage divider connected to the A/D resistive ladder can offset conversion dynamic range to specified limits within the AV_{CC} and A_{GND} limits. By loading Bank (C) Register 9, bits 0-4, with the appropriate value it is possible to select from these groups:

   a. No Offset. The Converter Dynamic range is from 0V to 5.0V for AV_{CC} = 5.0V.

   b. 35 Percent A_{GND} Offset. The Converter Dynamic range is 1.75V - 5.0V for AV_{CC} = 5.0V.

   c. 50 Percent A_{GND} Offset. The Converter Dynamic range is 2.5V - 5.0V for AV_{CC} = 5.0V.

5. Select one of the eight A/D inputs for conversion by loading Bank (C) Register 8 with the desired attributes: Bits 0 - 2 select an A/D input, bits 3 and 4 select A/D conversion (or digital port I/O).

6. Set Bank (C) Register 8, bit 3 to enable A/D conversion. (This flag can be set concurrently with step 3.) This flag is automatically reset when the A/D conversion is completed, so a bit test can be performed to determine A/D readiness if necessary.

7. Read the A/D result in Bank (C) Register A. Please note that the A/D result is not valid (indeterminate) unless ADE flag (Register 9, bit 7) was previously set, otherwise A/D converter output is tri-stated.

Digital-to-Analog Converters

The Z86C84 has two Digital-to-Analog Converters (DACs). Each DAC is an 8-bit resistor string, with a programmable 0.25X, 0.5X, or 1X gain output buffer. The DAC output voltage settles after the internal data is latched into the DAC Data register. The top and bottom ends of the resistor ladder are register-selected to be connected to either the analog supply rails, AV_{CC} and A_{GND}, or two externally-provided reference voltages, VDHI and VDLO. External references are recommended to explicitly set the DAC output limits. Since the gain stage cannot drive to the supply rails, VDHI and VDLO must be within ranges shown in the specifications. If either reference approaches the analog supply rails, the output will be unable to span the reference voltage range. The externally provided reference voltages should not exceed the supply voltages. The DAC outputs are latch-up protected and can drive output loads (Figure 28).

Note: The AV_{CC} must be the same value as V_{CC} and A_{GND} must be the same value as GND

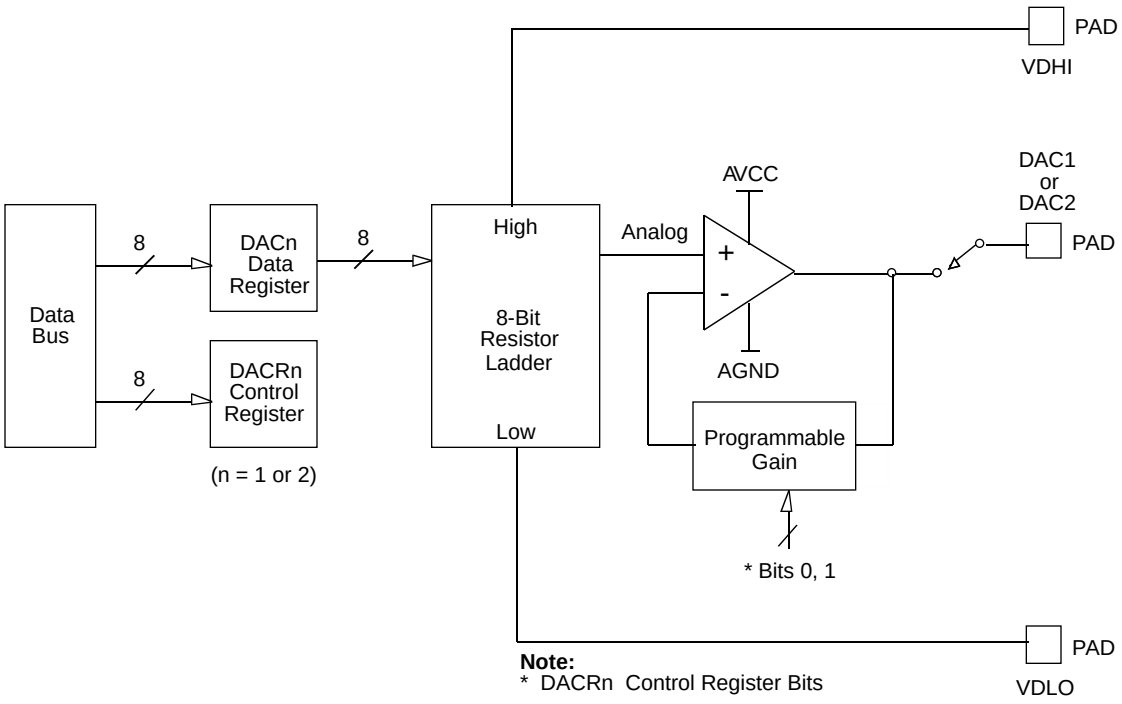


Figure 28. DAC Block Diagram

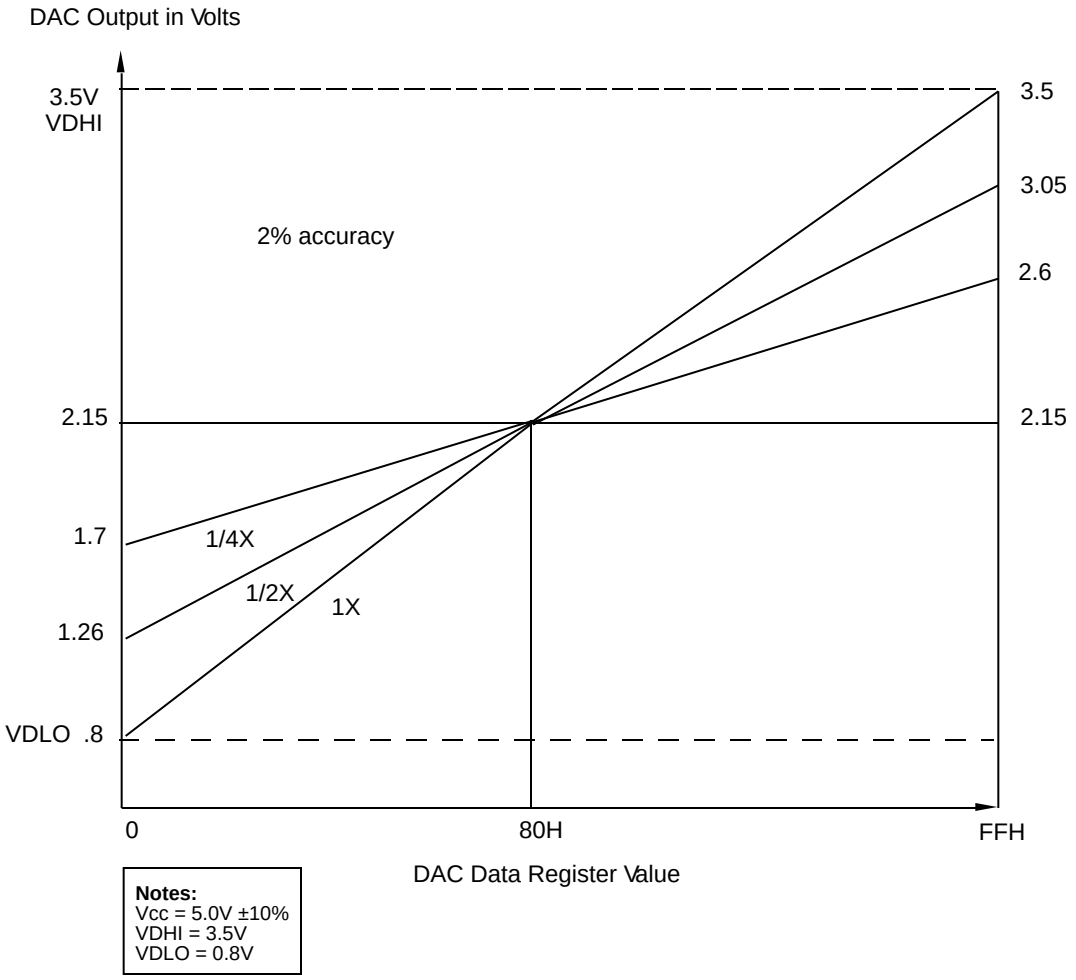


Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, that is**,**

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery (SMR) Register. This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 34 and Figure 35). All bits are Write-Only, except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR Register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR Register is located in Bank F of the Expanded Register Group at address 0BH. When the Stop-Mode Recovery sources are selected in this register, then SMR2 Register bits D0,D1 must be set to 0.

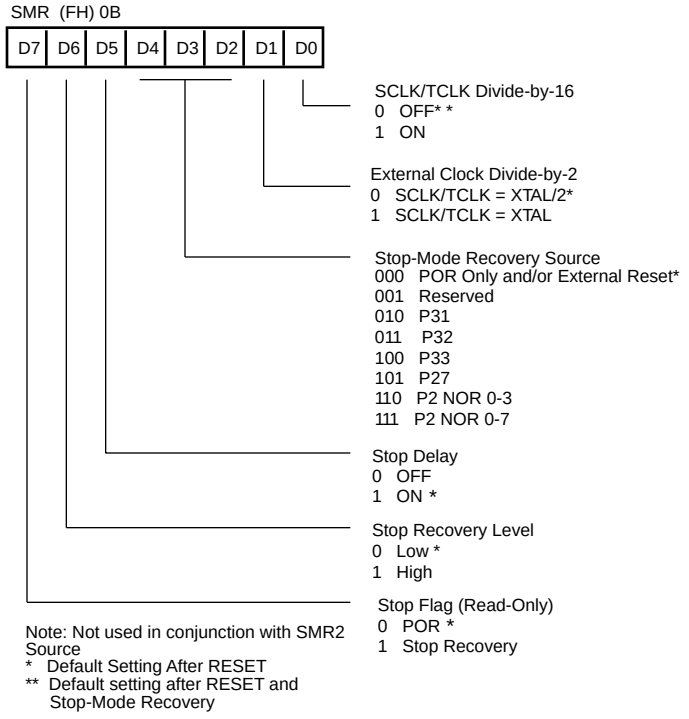


Figure 34. Stop-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

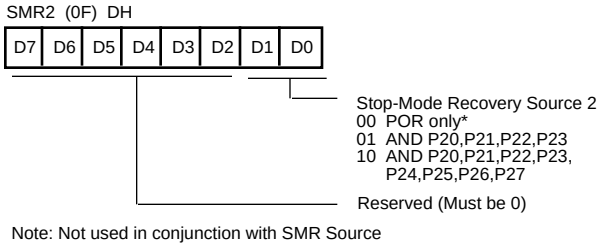


Figure 35. Stop-Mode Recovery Register 2 ([0F] DH: Write-Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery, WDT Time-out, and POR.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock HALT Mode frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 8 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

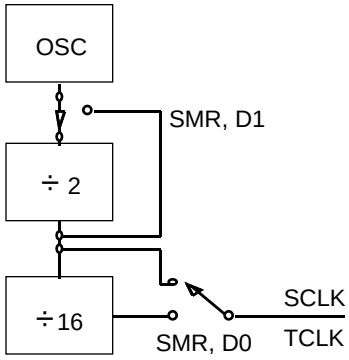


Figure 36. SCLK Circuit

Z8 CONTROL REGISTERS (Continued)

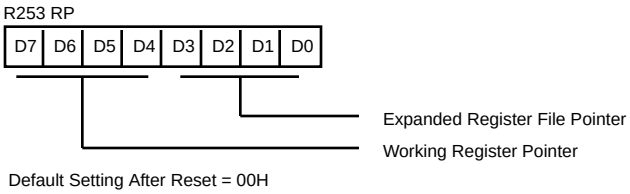


Figure 64. Register Pointer (F_{DH}: Read/Write)

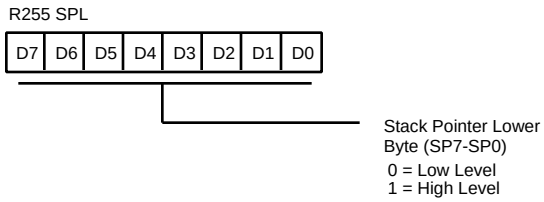


Figure 66. Stack Pointer (F_{FH}: Read/Write)

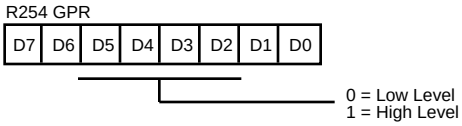


Figure 65. General-Purpose Register (F_{EH}: Read/Write)

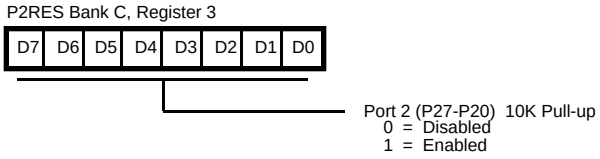
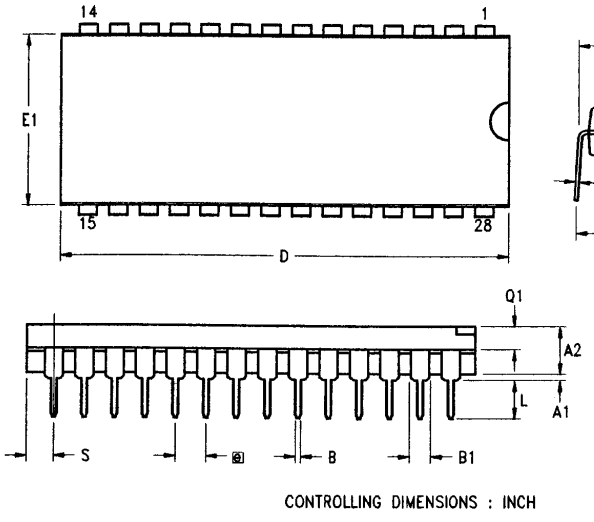


Figure 67. Port 2 Pull-up Register

PACKAGE INFORMATION



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

ORDERING INFORMATION

Z86C83 16 MHz			Z86E83 16 MHz		
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**	**28-Pin DIP**	**28-Pin SOIC**	**28-Pin PLCC**
Z86C8316PSC	Z86C8316SSC	Z86C8316VSC	Z86E8316PSC	Z86E8316SSC	Z86E8316VSC
Z86C8316PEC	Z86C8316SEC	Z86C8316VEC	Z86E8316PEC	Z86E8316SEC	Z86E8316VEC
Z86C84 16 MHz					
28-Pin DIP	**28-Pin SOIC**	**28-Pin PLCC**			
Z86C8416PSC	Z86C8416SSC	Z86C8416VSC			
Z86C8416PEC	Z86C8416SEC	Z86C8416VEC			

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP
S = Plastic SOIC

Temperature

S = 0°C to + 70°C
E = -40°C to +105°C

Speed

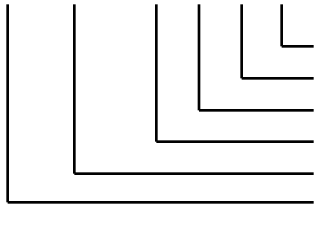
16 = 16 MHz

Environmental

C = Plastic Standard

Example:

Z 86C83 16 P S C is a Z86C83, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056