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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316vsc00tr

GENERAL DESCRIPTION (Continued)

By means of an expanded register file, the designer has access to additional control registers for configuring peripheral functions including the A/D and D/A converters, counter/timers, and I/O port functions (Figure 1).

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{CC}
Ground	GND	V_{SS}

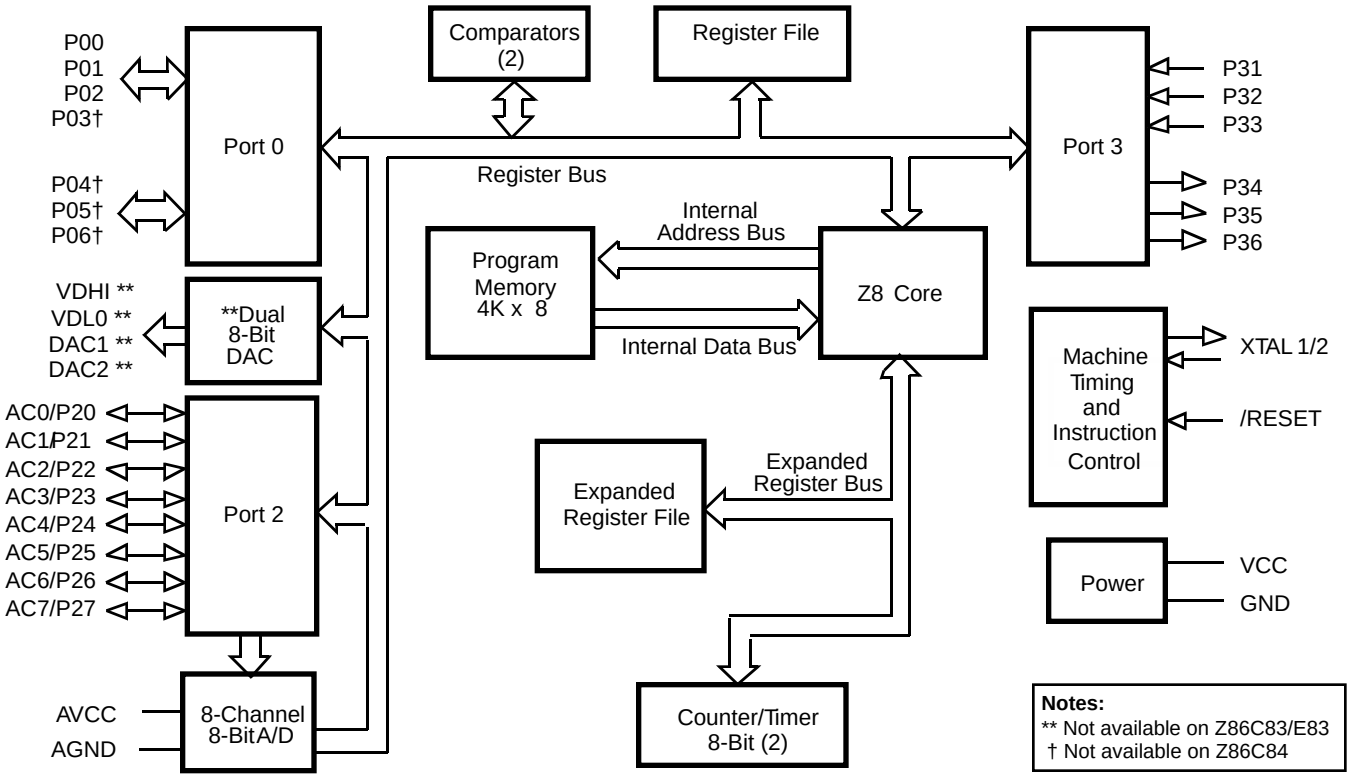


Figure 1. Z86C83/C84/E83 Functional Block Diagram

PIN DESCRIPTION (Continued)

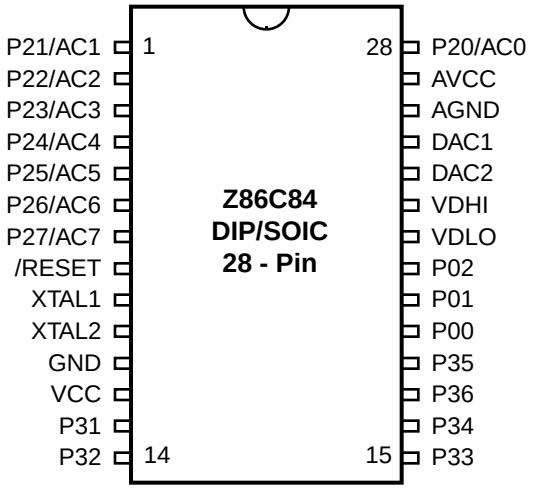


Figure 3. Z86C84 28-Pin DIP and SOIC Pin Configuration

Table 2. Z86C84 28-Pin DIP, SOIC, PLCC Pin Identification*

No	Symbol	Function	Direction
1-7	P21-P27 or AC1-AC7	Port 2, Bit 1-7 Analog In 1-7	Input/Output
8	/RESET	Reset	Input
9	XTAL1	Oscillator Clock	Input
10	XTAL2	Oscillator Clock	Output
11	GND	Ground	
12	V_{CC}	Power	
13-15	P31-P33	Port 3, Bits 1-3	Input
16	P34	Port 3, Bit 4	Output
17	P36	Port 3, Bit 6	Output
18	P35	Port 3, Bit 5	Output
19-21	P00-P02	Port 0, Bits 0-3	Input/Output
22	VDLO	D/A Ref. Volt.,Low	Input
23	VDHI	D/A Ref. Volt.,High	Input
24-25	DAC2-1	D/A Converter	Output
26	A_{GND}	Analog Ground	
27	AV_{CC}	Analog Power	
28	P20 or AC0	Port 2, Bit 0 Analog In 0	Input/Output

Note: * DIP, PLCC and SOIC Pin Description and Configuration are identical

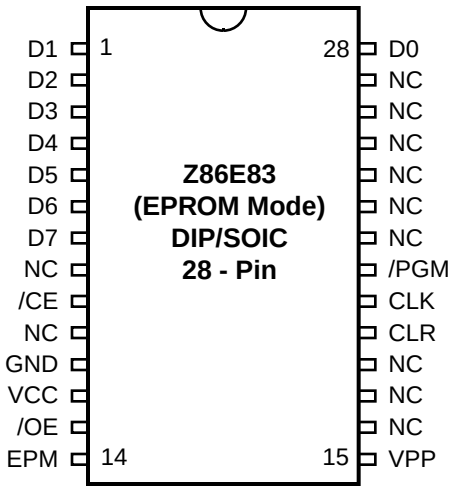


Figure 4. Z86E83 EPROM Programing Mode 28-Pin DIP and SOIC Pin Configuration

Table 3. Z86E83 EPROM Programming Mode 28-Pin DIP, PLCC and SOIC Pin Identification

No	Symbol	Function	Direction
1-7	D1-D7	Data 1,2,3,4,5,6,7	Input/Output
8	NC	No Connection	
9	/CE	Chip Enable	Input
10	NC	No Connection	
11	GND	Ground	
12	V_{CC}	Power	
13	/OE	Output Enable	Input
14	EPM	EPROM Program Mode	Input
15	V_{PP}	Program Voltage	Input
16-18	NC	No Connection	
19	CLR	Clear CLock	Input
20	CLK	Address	Input
21	/PGM	Program Mode	Input
22-27	NC	No Connection	
28	D0	Data 0	Input/Output

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 8).

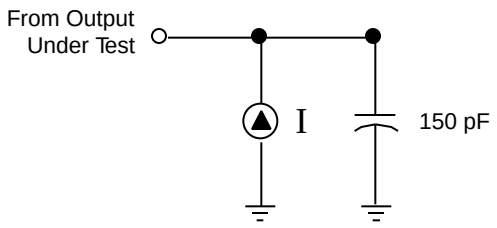


Figure 8. Test Load Diagram

V_{DD} SPECIFICATION

V_{DD} = 3.5V to 5.5V (Z86E83 only at 0° C to 70° C)

V_{DD} = 3.0V to 5.5V (Z86C83/C84)

V_{DD} = 4.5V to 5.5V (Z86E83 only at -40° C to 105° C)

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	15 pF
I/O capacitance	0	15 pF

Sym	Parameter	V_{cc} Note 3	T_A = 0° C to +70°C Min	Max	T_A = –40°C to +105°C Min	Max	Typical [13] @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (HALT Mode)	3.0V		4.5		4.5	2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	4
		3.0V		3.4		3.4	1.5	mA	Clock Divide-by-16 @ 16 MHz	4
		5.5V		7.0		7.0	2.9	mA	Clock Divide-by-16 @ 16 MHz	4
I_{CC2}	Standby Current (STOP Mode)	3.0V		8		15	1	µA	V_{IN} = 0V,V_{CC} Vcc WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.0V		500		600	310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11,14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11,14
V_{ICR}	Input Common Mode	3.0	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
	Voltage Range	5.5	0	V_{CC}- 1.0V	0	V_{CC}- 1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.0V		8		10	5	µA	0V < V_{IN} < V_{CC}	9
		5.5V		15		20	11	µA	0V < V_{IN} < V_{CC}	9
I_{ALH}	Auto Latch High Current	3.0V		-5		-7	-3	µA	0V < V_{IN} < V_{CC}	9
		5.5V		-8		-10	-6	µA	0V < V_{IN} < V_{CC}	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max Int. CLK Freq.	7

Notes:

1. Combined digital V_{CC} and Analog AV_{CC} supply currents.
2. GND = 0V.
3. V_{CC} voltage specification of 3.0V guarantees 3.3V ±0.3V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF.
6. Same as note [4] except inputs at V_{cc}.
7. The V_{LV} increases as the temperature decreases.
8. Standard Mode (not Low EMI).
9. Auto Latch (mask option) selected.
10. For analog comparator, inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating.
12. Excludes clock pins.
13. Typicals are at V_{CC} = 5.0V and 3.3V.
14. Internal RC selected
15. For Z86C83 only

AC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only. Low EMI Mode Only.

				T_A = 0°C to +70°C		T_A = -40° to +105°C			
				4 MHz		4 MHz			
No	**Symbol**	**Parameter**	**V_{CC} [6]**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	1,7,8
			5.5V	250	DC	250	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	3.0V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.0V	125		125		ns	1,7,8
			5.5V	125		125		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC		ns	1,7,8
			5.5V	3TpC		3TpC		ns	1,7,8
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			1,7,8
			5.5V	4TpC		4TpC			1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.0V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC		ns	1,3,7,8
			5.5V	3TpC		3TpC		ns	1,3,7,8
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC		ns	1,2,7,8
			5.5V	3TpC		3TpC		ns	1,2,7,8
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	4,8
			5.5V	12		12		ns	4,8
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P33-P31)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode delay is on.
5. Reg. WDTMR
6. The V_{CC} voltage specification of 3.0V guarantees 3.3V ± 0.3V, and the V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode
9. For LC oscillator and for oscillator driven by clock driver

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	T_A = 0° C to +70° C Max	T_A = -40° C to +105° C Min	T_A = -40° C to +105° C Max	Typical [13] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.5V		8			1	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.5V		500			310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
V_{ICR}	Input Common Mode	3.5V	0	V_{CC}-1.0V	0			V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.5V		8			5	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		15		20	11	µA	$0V<V_{IN}<V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V		-5			-3	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		-8		-10	-6	µA	$0V<V_{IN}<V_{CC}$	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max. Int. CLK Frequency	7

Notes:

1. Combined digital V_{CC} and analog AV_{CC} supply currents
2. GND = 0V
3. V_{CC} voltage specification of 3.5V guarantees 3.5V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V
4. All outputs unloaded, I/O pins floating, inputs at rail
5. CL1 = CL2 = 100 pF
6. Same as note [4] except inputs at V_{CC}
7. The V_{LV} increases as the temperature decreases
8. Standard Mode (not Low EMI)
9. Auto Latch (mask option) selected
10. For analog comparator, inputs when analog comparators are enabled
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating
12. Excludes clock pins
13. Typicals are at V_{CC} = 3.5V and 5.0V
14. Internal RC selected

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

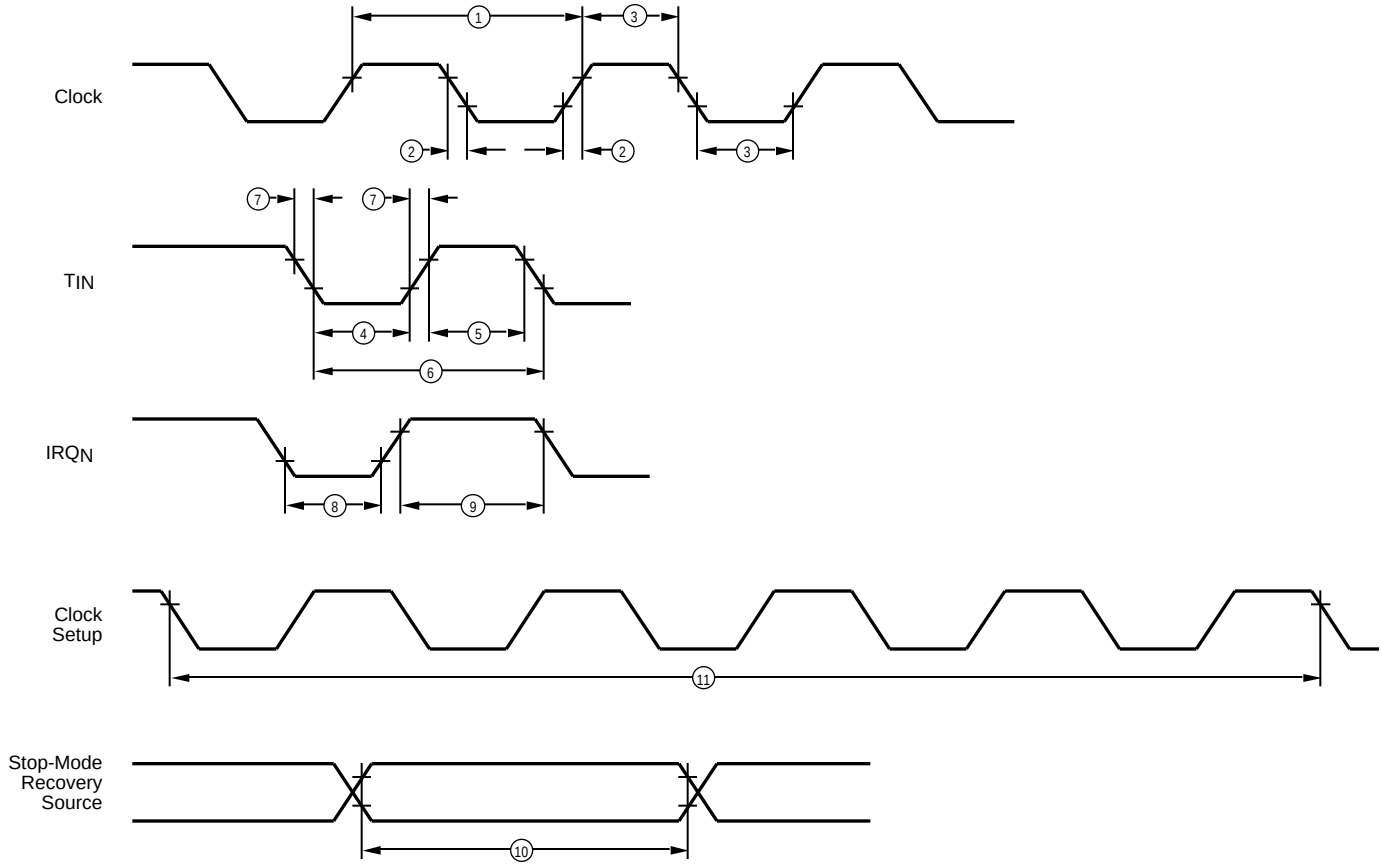


Figure 9. Additional Timing

For Z86E83

Table 8. A/D Converter Electrical Characteristics
V_{CC} = 3.5V

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	3.5			Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 9. A/D Converter Electrical Characteristics
V_{CC} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time	4.3		35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

PIN FUNCTIONS (Continued)

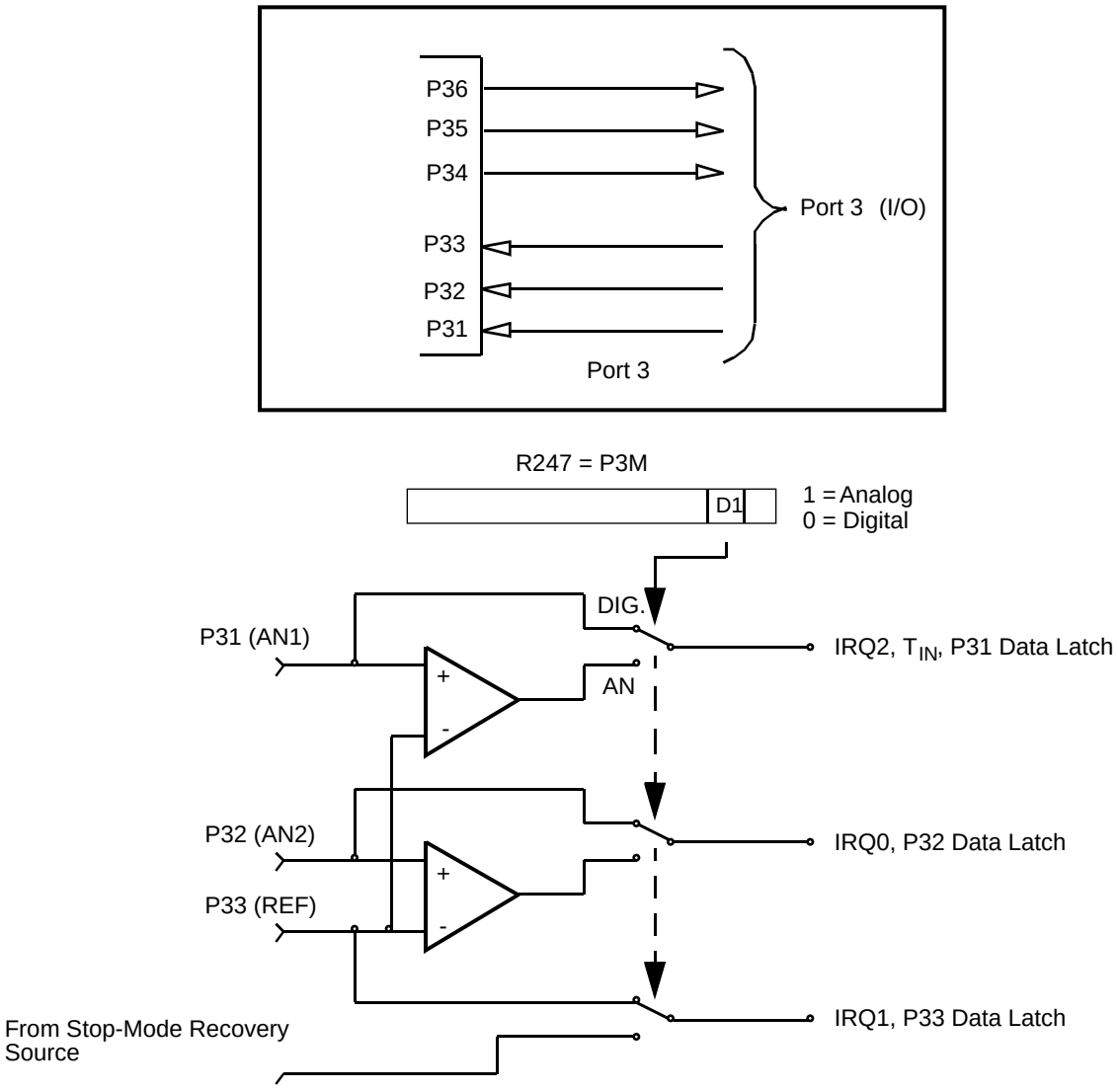


Figure 12. Port 3 Input Configuration

FUNCTIONAL DESCRIPTION (Continued)

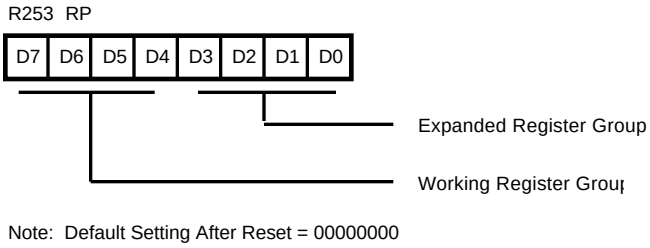


Figure 17. Register Pointer Register

Register File. The Register File consists of three I/O port registers, 237 general-purpose registers, 15 control and status registers, and four system configuration registers in the Expanded Register Group (Figure 16). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 18). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 17) addresses the starting location of the active working-register group.

Note: Register Bank E0-EF is only accessed either as working registers or through indirect addressing modes.

CAUTION: D4 of Control Register P01M (R251) must be 0.

R254. The C83/C84/E83 has one extra general-purpose register located at FEH (R254).

Stack. The C83/C84/E83 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 236 general-purpose registers. Register R254 cannot be used for stack.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. It will not keep its last state from a V_{LV} reset if the V_{CC} drops below 1.8V. This includes Register R254.

Note: Register Bank E0-EF is only accessed either as working register or through indirect addressing modes.

RAM Protect. The upper portion of the RAM's address spaces %80F to %EF (excluding the control registers) are protected from writing. The user activates this feature from the internal ROM code to turn off/on the RAM Protect by loading either a 0 or 1 into the Interrupt Mask (IMR) register, bit D6. A 1 in D6 enables RAM Protect.

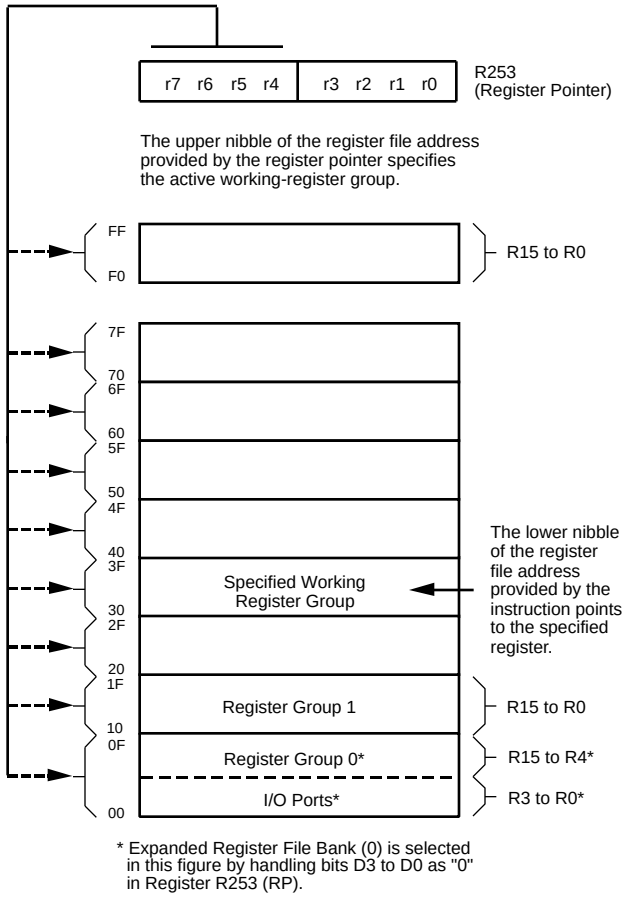


Figure 18. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has six different interrupts from six different sources. These interrupts are maskable, prioritized (Figure 20) and the six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers (Table 11). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This action disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt.

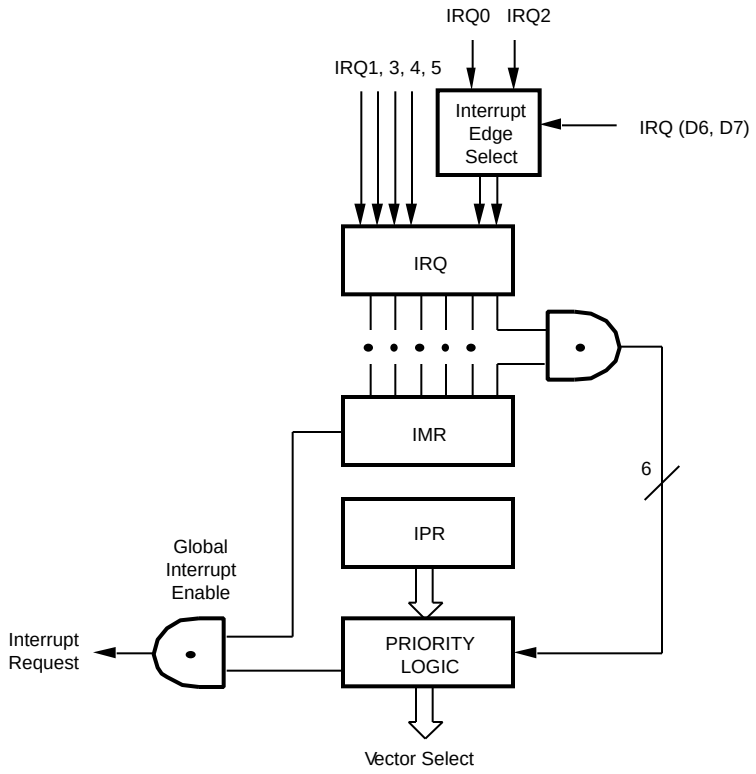


Figure 20. Interrupt Block Diagram

Table 11. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rise Fall Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Fall Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rise Fall Edge Triggered
IRQ3	IRQ3	6, 7	By User Software
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

All Z8 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select is located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 12.

Table 12. IRQ Register

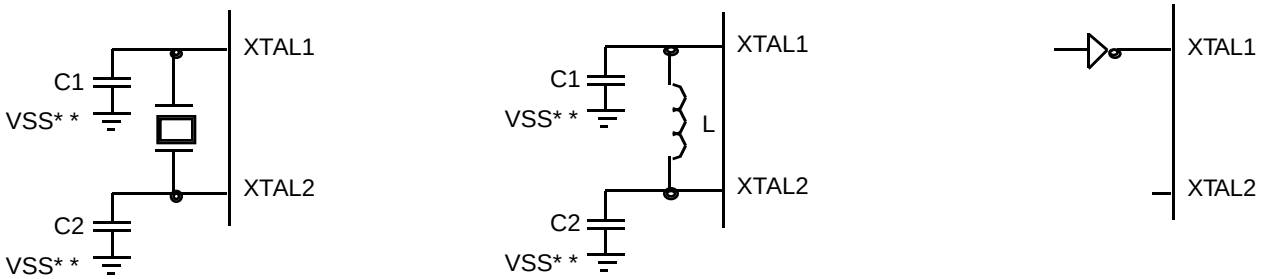
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 16 MHz max., with a series resistance (RS) of less than or equal to 100 Ohms when clocking from 1 MHz to 16 MHz.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to the device Ground pin to reduce Ground noise injection into the oscillator (Figure 21).

Note: For better noise immunity, the capacitors should be tied directly to the device Ground pin (V_{SS}).



Ceramic Resonator or Crystal
C1, C2 = 22 pF TYP *
f = 8 MHz

LC

External Clock

* Preliminary value including pin parasitics
* * Device ground pin

Figure 21. Oscillator Configuration

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake-up source of the STOP recovery (Figure 37 and Table 13). When the Stop-Mode Recovery Sources are selected in this register then SMR2 register bits D0,D1 must be set to zero. P33-P31 and Port 2 cannot wake up from STOP Mode if the input lines are configured as analog inputs to the Analog comparator or Analog-to-Digital Converter.

Note: If the Port 2 pin is configured as an output, this output level will be read by the SMR circuitry.

Table 13. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition (not in Analog Mode)
0	1	1	P32 transition (not in Analog Mode)
1	0	0	P33 transition (not in Analog Mode)
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Stop-Mode Recovery Delay Select (D5). This bit, if High, enables the T_{POR} /RESET delay after Stop-Mode Recovery. The default configuration of this bit is "1". A POR or WDT reset will override the selection and cause the reset delay to occur.

Stop-Mode Recovery Edge Select (D6). A "1" in this bit position indicates that a high level on the output to the exclusive Or-Gate input from the selected recovery source wakes the Z86C83/C84/E83 from STOP Mode. A "0" indicates low-level recovery. The default is 0 on POR. This bit is used for either SMR or SMR2.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device resets by POR/WDT reset. A "1" in this bit (warm) indicates that the device awakens by a Stop-Mode Recovery source.

Note: A WDT reset out of STOP Mode will also set this bit to a "1".

Stop-Mode Recovery Register 2 (SMR2). This register contains additional Stop-Mode Recovery sources. When the Stop-Mode Recovery sources are selected in this register then SMR Register Bits D2, D3, and D4 must be 0.

Table 14. Stop-Mode Recovery Source

SMR:10		Operation
D1	D0	Description of Action
0	0	POR and/or external reset recovery
0	1	Logical AND of P20 through P23
1	0	Logical AND of P20 through P27

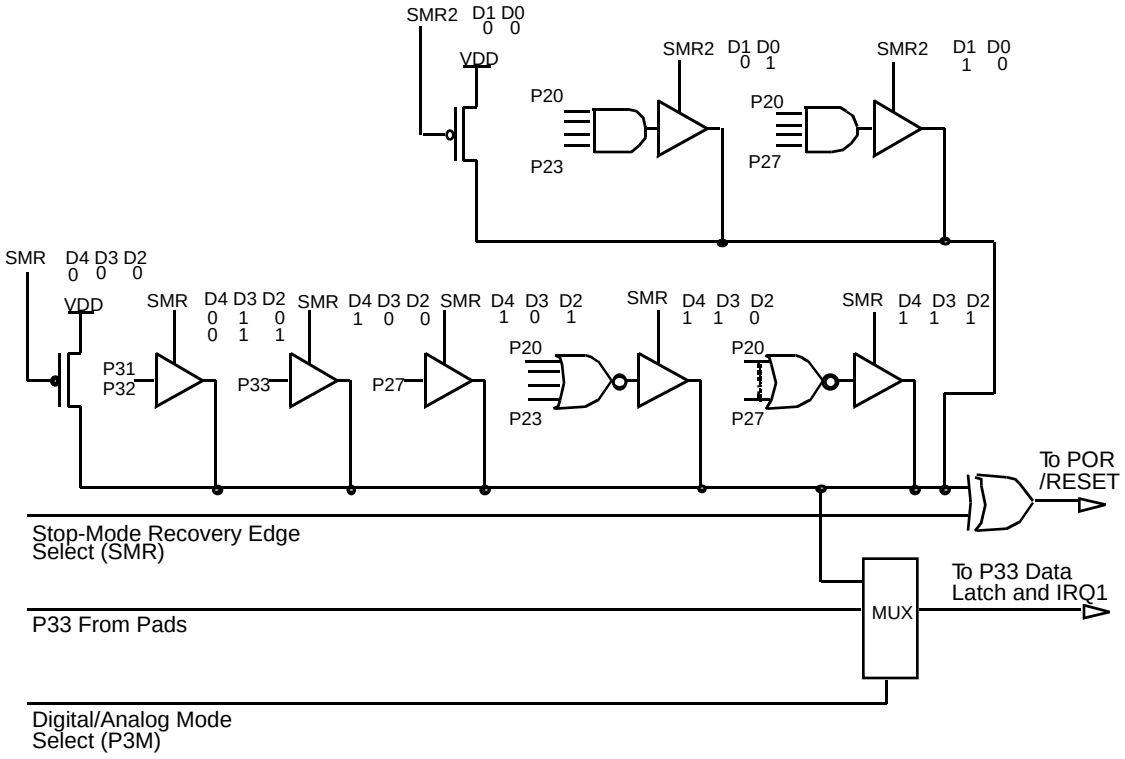


Figure 37. Stop-Mode Recovery Source

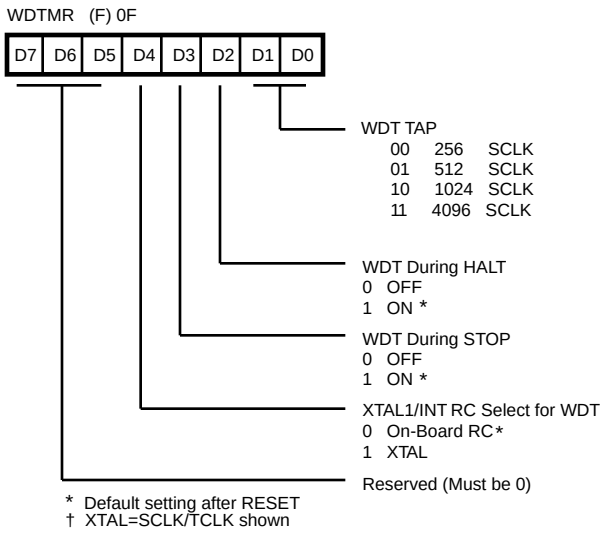


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 15.

Table 15. WDT Time Select (Min. @ 5.0V)

D1	D0	Time-Out of Internal RC OSC	Time-Out of SCLK Clock
0	0	6.25 ms min	256 SCLK
0	1	12.5 ms min	512 SCLK
1	0	25 ms min	1024 SCLK
1	1	100 ms min	4096 SCLK

Note: The minimum time shown is for V_{CC} @ 5.0V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. The default is "1".

Note: If WDT is permanently selected (always ON mode), the WDT will continue to run even if set not to run in STOP or HALT Mode.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A "1" indicates active during STOP. The default is "1". If bits D3 and D4 are both set to "1", the WDT only, is driven by the external clock during STOP Mode.

Notes:

1. If WDT is permanently selected (always ON mode) using internal on-board RC oscillator, the WDT will continue to run even if set not to run in STOP or HALT Mode.

2. WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a "1", the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. If the XTAL1 pin is selected as the oscillator source for the WDT, during STOP Mode, the oscillator will be stopped and the WDT will not run. This is true even if the WDT is selected to run during STOP Mode.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

ROM Protect. ROM Protect is mask or OTP bit-programmable. It is selected by the customer at the time the ROM code is submitted.

ROM Mask Selectable Options

There are two ROM mask options that must be selected at the time the ROM mask is ordered (ROM code submitted) for the Z86C83/C84 and three Z86E83 OTP bit options.

Table 16. Selectable Options

Option	Selection
Permanent WDT	Yes/No
ROM Protect	Yes/No
EPROM/TEST Mode Disable*	Yes/No

Note:
*For Z86E83 only
EPROM/TEST Mode Disable - On the Z86E83, the user can permanently disable entry into EPROM Mode and TEST Mode by programming this bit.

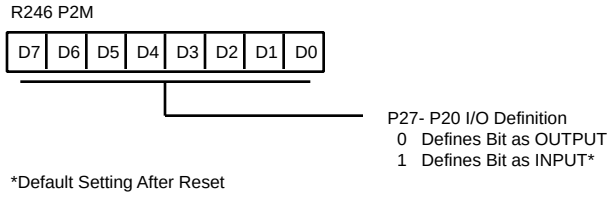


Figure 58. Port 2 Mode Register ($F6_H$: Write-Only)

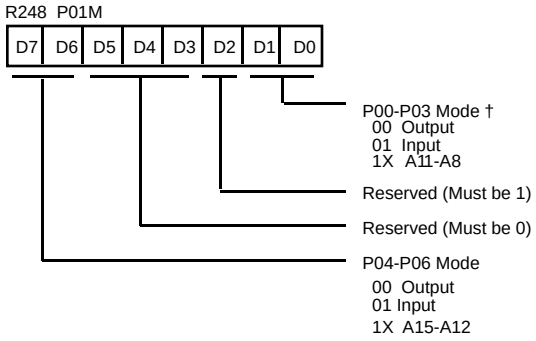


Figure 59. Port 0 and 1 Mode Register ($F8_H$: Write-Only)

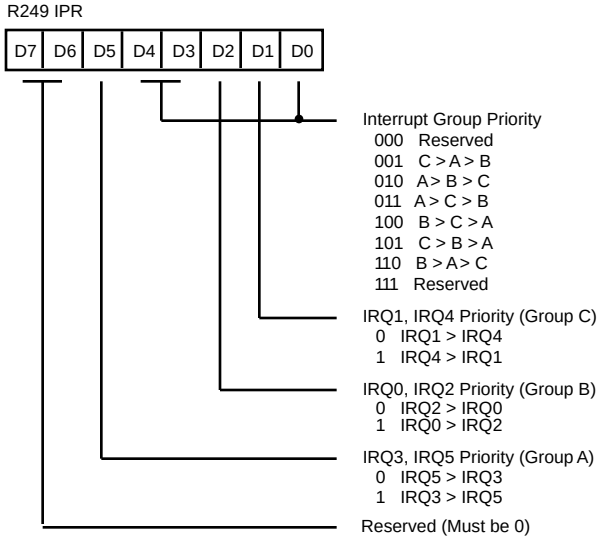


Figure 60. Interrupt Priority Register ($F9_H$: Write-Only)

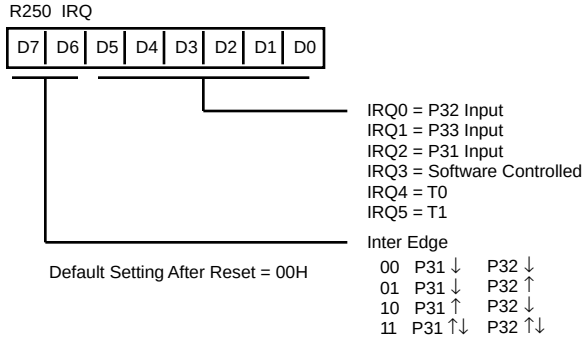


Figure 61. Interrupt Request Register (F_{AH}: Read/Write)

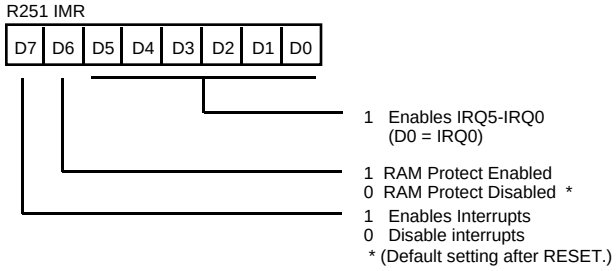


Figure 62. Interrupt Mask Register (F_{BH}: Read/Write)

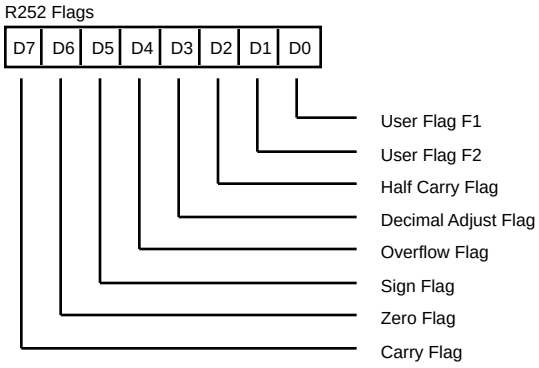


Figure 63. Flag Register (F_{CH}: Read/Write)

Z8 CONTROL REGISTERS (Continued)

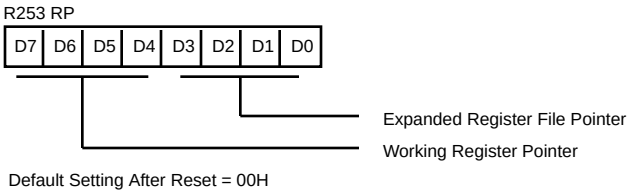


Figure 64. Register Pointer (F_{DH}: Read/Write)

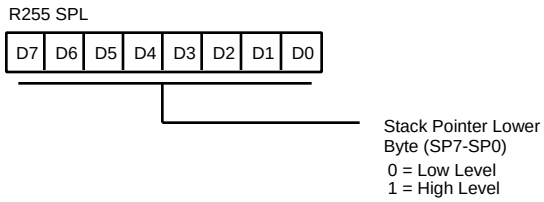


Figure 66. Stack Pointer (F_{FH}: Read/Write)

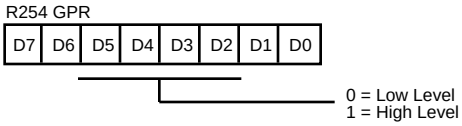


Figure 65. General-Purpose Register (F_{EH}: Read/Write)

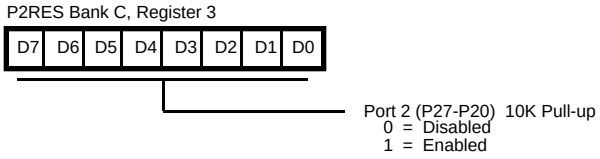
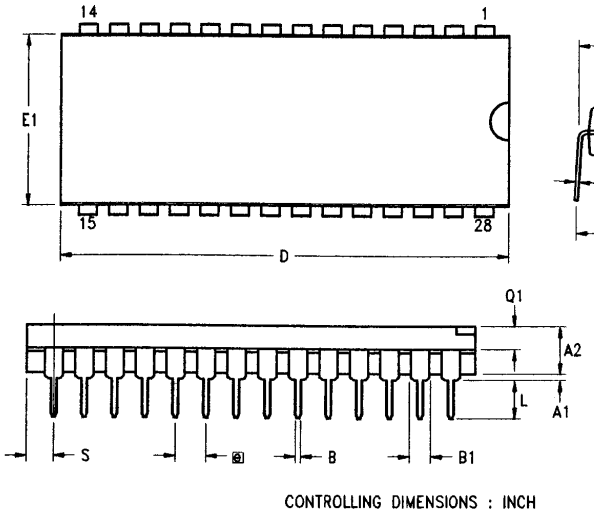


Figure 67. Port 2 Pull-up Register

PACKAGE INFORMATION



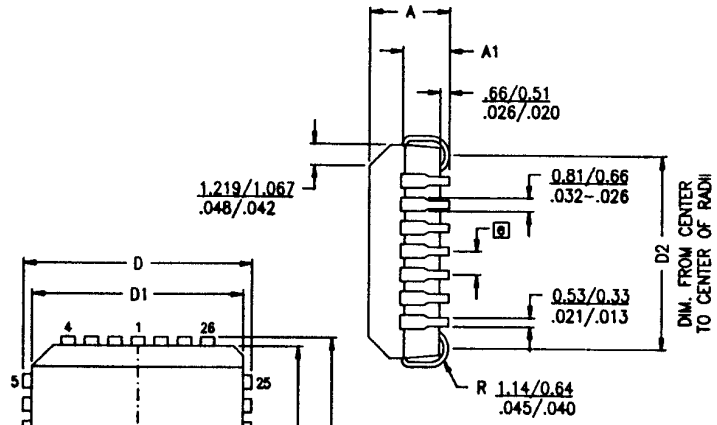
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

Figure 68. 28-Pin DIP Package Diagram

Figure 69. 28-Pin SOIC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
G	1.27 TYP		.050 TYP	

NOTES.
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 INCH.
3. DIMENSION : MM / INCH

Figure 70. 28-Pin PLCC Package Diagram