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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	21
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e8316vsg

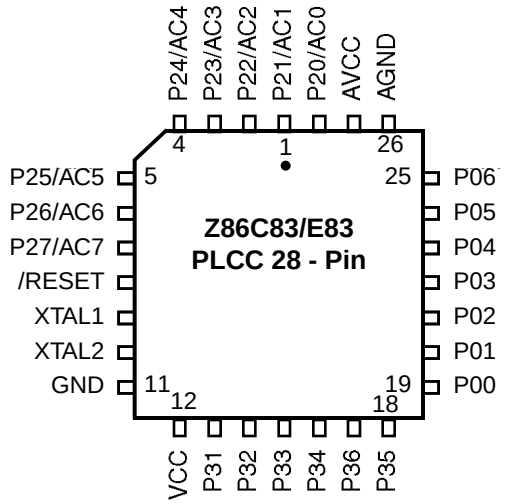


Figure 5. Z86C83 and Standard Mode Z86E83 28-Pin PLCC Pin Configuration

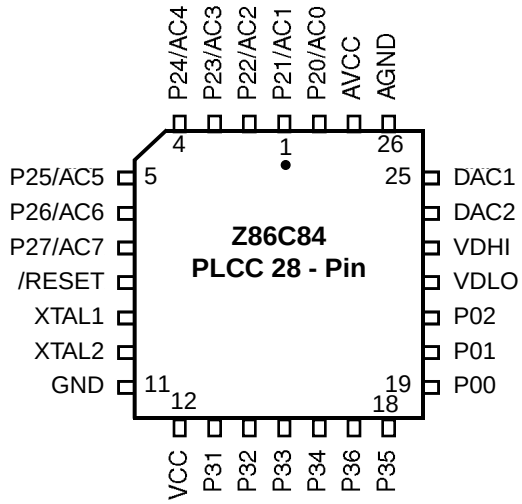


Figure 6. Z86C84 28-Pin PLCC Pin Configuration

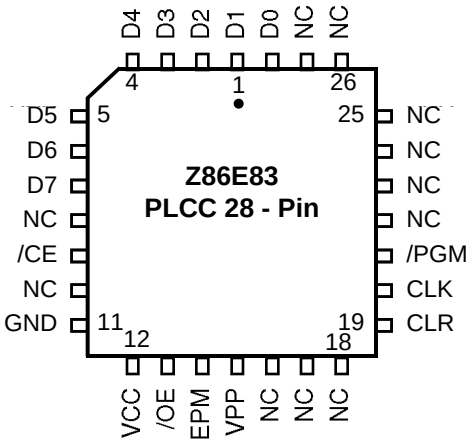


Figure 7. Z86E83 EPROM Programming Mode 28-Pin PLCC Pin Configuration

ABSOLUTE MAXIMUM RATING

Parameter	Min	Max	Units	Notes
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{CC} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on /RESET Pin with Respect to V_{SS}	–0.6	V_{CC}+1	V	2
Voltage on P32, P33 and /Reset Pin with Respect to V_{SS}	-0.6	V_{CC}+1	V	2,5
Total Power Dissipation		770	mW	
Maximum Current out of V_{SS}		140	mA	
Maximum Current into V_{CC}		125	mA	
Maximum Current into an Input Pin	–600	+600	µA	3
Maximum Current into an Open-Drain Pin	–600	+600	µA	4
Maximum Output Current Sinked by Any I/O Pin		25	mA	
Maximum Output Current Sourced by Any I/O Pin		25	mA	

Notes:
1. This applies to all pins except /RESET pin and where otherwise noted.
2. There is no input protection diode from pin to V_{CC}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.
5. For Z86E83 only

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package.
Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{CC} \times [I_{CC} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{CC} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 8).

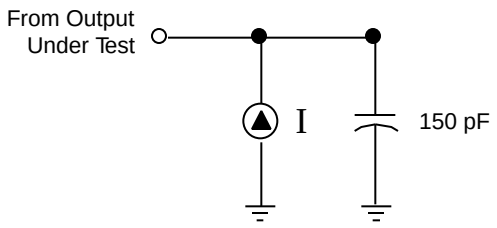


Figure 8. Test Load Diagram

V_{DD} SPECIFICATION

V_{DD} = 3.5V to 5.5V (Z86E83 only at 0° C to 70° C)

V_{DD} = 3.0V to 5.5V (Z86C83/C84)

V_{DD} = 4.5V to 5.5V (Z86E83 only at -40° C to 105° C)

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	15 pF
I/O capacitance	0	15 pF

DC ELECTRICAL CHARACTERISTICS

For Z86C83/C84 Only

Sym	Parameter	V_{CC} Note 3	T_A = 0° C to +70°C Min	T_A = 0° C to +70°C Max	T_A = –40°C to +105°C Min	T_A = –40°C to +105°C Max	Typical [13] @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	1.3	V		
		5.5V	0.7 V_{CC}	V_{CC} +0.3	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Output High Voltage	3.0V	V_{CC} -0.4		V_{CC} -0.4		3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC} -0.4		V_{CC} -0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.0V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.0V		1.2		1.2	0.3	V	I_{OL} = +6 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OL} = +10 mA	8
V_{RH}	Reset Input High Voltage	3.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.0V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.1	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.0V		25		25	10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		-130		-130	-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.0V		20		20	7	mA	@ 16 MHz	1,4
		5.5V		25		25	20	mA	@ 16 MHz	1,4
		5.0V		7		7	3	mA	@ 3.58 MHz	1,4,15
		5.5V		10		10	5	mA	@ 8 MHz	1,4,15

For Z86E83 Only

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	Max	T_A = -40° C to +105° C Min	Max	Typical [13] @25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V	Driven by External Clock Generator	
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	0.7 V_{CC}	V_{CC}+0.3			1.3	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	GND-0.3	0.2 V_{CC}			0.7	V		
		5.5V	GND-0.3	0.2 V_{CC}	GND-0.3	0.2 V_{CC}	1.5	V		
V_{OH1}	Ouput High Voltage	3.5V	V_{CC}-0.4				3.1	V	I_{OH} = -2.0 mA	8
		5.5V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OH} = -2.0 mA	8
V_{OL1}	Output Low Voltage	3.5V		0.6			0.2	V	I_{OH} = +4.0 mA	8
		5.5V		0.4		0.4	0.1	V	I_{OH} = +4.0 mA	8
V_{OL2}	Output Low Voltage	3.5V		1.2			0.3	V	I_{OH} = +6.0 mA	8
		5.5V		1.2		1.2	0.3	V	I_{OH} = +10.0 mA	8
V_{RH}	Reset Input High Voltage	3.5V	0.8V_{CC}	V_{CC}			1.5	V		
		5.5V	0.8V_{CC}	V_{CC}	0.8V_{CC}	V_{CC}	2.1	V		
		3.5V	GND-0.3	0.2V_{CC}			1.1	V		
		5.5V	GND-0.3	0.2V_{CC}	GND-0.3	0.2V_{CC}	1.7	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25			10	mV		10
		5.5V		25		25	10	mV		10
I_{IL}	Input Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	-1	1			<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V		-130			-25	µA		
		5.5V		-180		-180	-40	µA		
I_{CC}	Supply Current	3.5V		20			7	mA	@16 MHz	1,4
		5.5V		25		25	20	mA	@16 MHz	1,4
I_{CC1}	Standby Current (HALT Mode)	3.5V		4.5			2.0	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		5.5V		8		8	3.7	mA	V_{IN} = 0V, V_{CC} @ 16 MHz	1,4
		3.5V		3.4			1.5	mA	Clock divide by 16 @ 16 MHz	1,4
		5.5V		7.0		7.0	2.9	mA	Clock divide by 16 @ 16 MHz	1,4

Sym	Parameter	V_{CC} [3]	T_A = 0° C to +70° C Min	T_A = 0° C to +70° C Max	T_A = -40° C to +105° C Min	T_A = -40° C to +105° C Max	Typical [13] @25°C	Units	Conditions	Notes
I_{CC2}	Standby Current (STOP Mode)	3.5V		8			1	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		5.5V		10		20	2	µA	V_{IN} = 0V, V_{CC} WDT is not Running	1,6,11
		3.5V		500			310	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
		5.5V		800		1000	600	µA	V_{IN} = 0V, V_{CC} WDT is Running	1,6,11, 14
V_{ICR}	Input Common Mode	3.5V	0	V_{CC}-1.0V	0			V		10
		5.5V	0	V_{CC}-1.0V	0	V_{CC}-1.5V		V		10
I_{ALL}	Auto Latch Low Current	3.5V		8			5	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		15		20	11	µA	$0V<V_{IN}<V_{CC}$	9
I_{ALH}	Auto Latch High Current	3.5V		-5			-3	µA	$0V<V_{IN}<V_{CC}$	9
		5.5V		-8		-10	-6	µA	$0V<V_{IN}<V_{CC}$	9
V_{LV}	V_{CC} Low-Voltage Protection Voltage		2.0	3.3	2.2	3.5	3.0	V	2 MHz max. Int. CLK Frequency	7

Notes:

1. Combined digital V_{CC} and analog AV_{CC} supply currents
2. GND = 0V
3. V_{CC} voltage specification of 3.5V guarantees 3.5V, and V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V
4. All outputs unloaded, I/O pins floating, inputs at rail
5. CL1 = CL2 = 100 pF
6. Same as note [4] except inputs at V_{CC}
7. The V_{LV} increases as the temperature decreases
8. Standard Mode (not Low EMI)
9. Auto Latch (mask option) selected
10. For analog comparator, inputs when analog comparators are enabled
11. Clock must be forced Low, when XTAL 1 is clock-driven and XTAL2 is floating
12. Excludes clock pins
13. Typicals are at V_{CC} = 3.5V and 5.0V
14. Internal RC selected

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

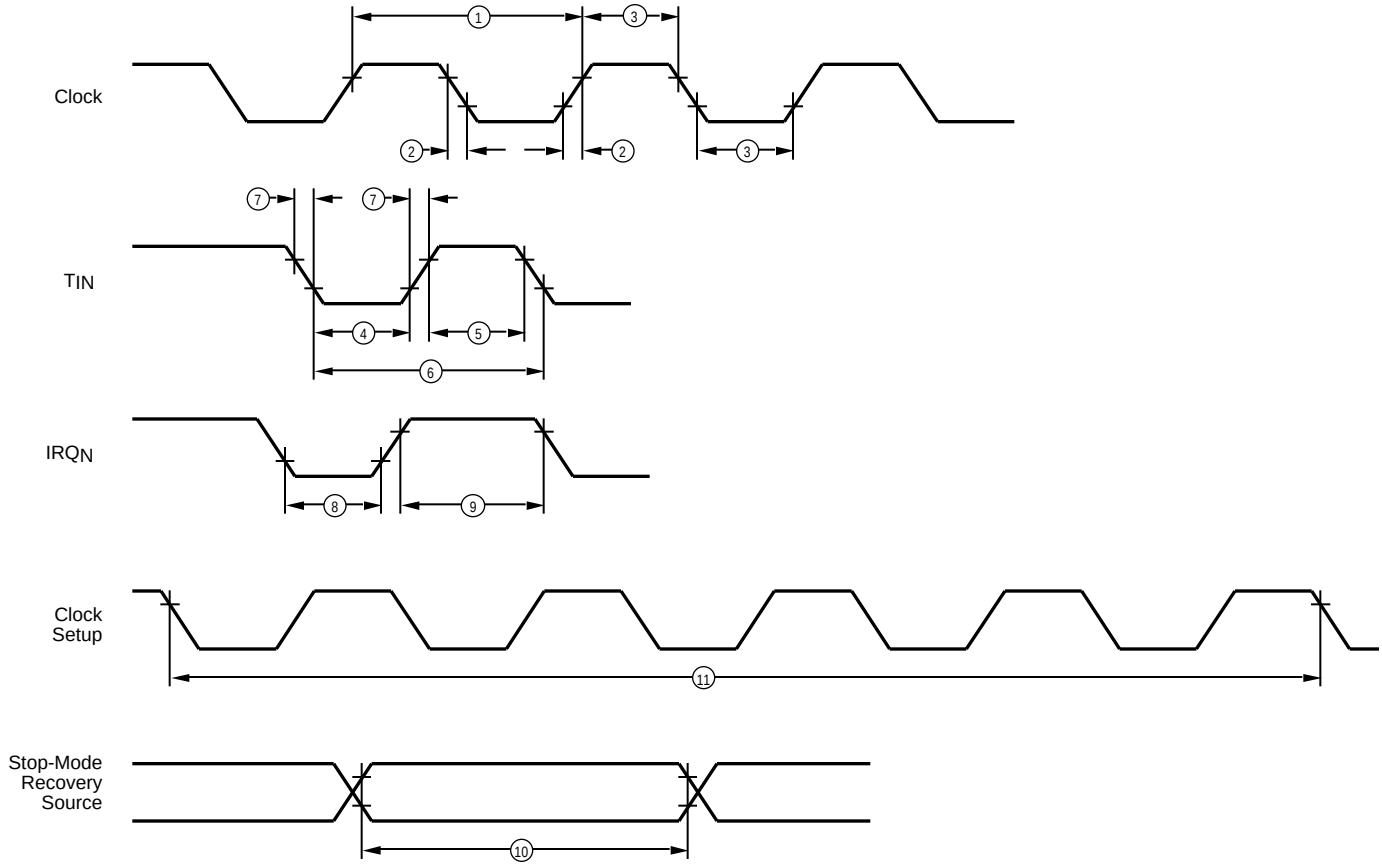


Figure 9. Additional Timing

CAPACITANCE (Continued)

For Z86C83/C84

Table 6. A/D Converter Electrical Characteristics
V_{cc} = 3.3V ± 10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	2.7	3.0	3.3	Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.0V – 3.6V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86C83/C84

Table 7. A/D Converter Electrical Characteristics
V_{cc} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 8. A/D Converter Electrical Characteristics
V_{CC} = 3.5V

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			5.0	mV
Supply Range	3.5			Volts
Power dissipation, no load		20	40	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time			35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 3.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

For Z86E83

Table 9. A/D Converter Electrical Characteristics
V_{CC} = 5.0V ±10%

Parameter	Minimum	Typical	Maximum	Units
Resolution		8		Bits
Integral non-linearity		0.5	1	LSB
Differential non-linearity		0.5	1	LSB
Zero Error at 25°C			45	mV
Supply Range	4.5	5.0	5.5	Volts
Power dissipation, no load		50	85	mW
Clock frequency			16	MHz
Input voltage range	VA_{LO}		VA_{HI}	Volts
Conversion time	4.3		35 x SCLK	µsec
Input capacitance on ANA	25		40	pF
VA_{HI} range	VA_{LO} +2.5		AV_{CC}	Volts
VA_{LO} range	AN_{GND}		AV_{CC}–2.5	Volts
VA_{HI} -–VA_{LO}	2.5		AV_{CC}	Volts

Notes:
Voltage: 4.5V –5.5V
Temp: 0-70°C
Conversion time is defined as the time from initiation of A-D conversion to storage of the digital result in the ADR register.
SCLK = Internal Z8 System Clock (Bus Speed)

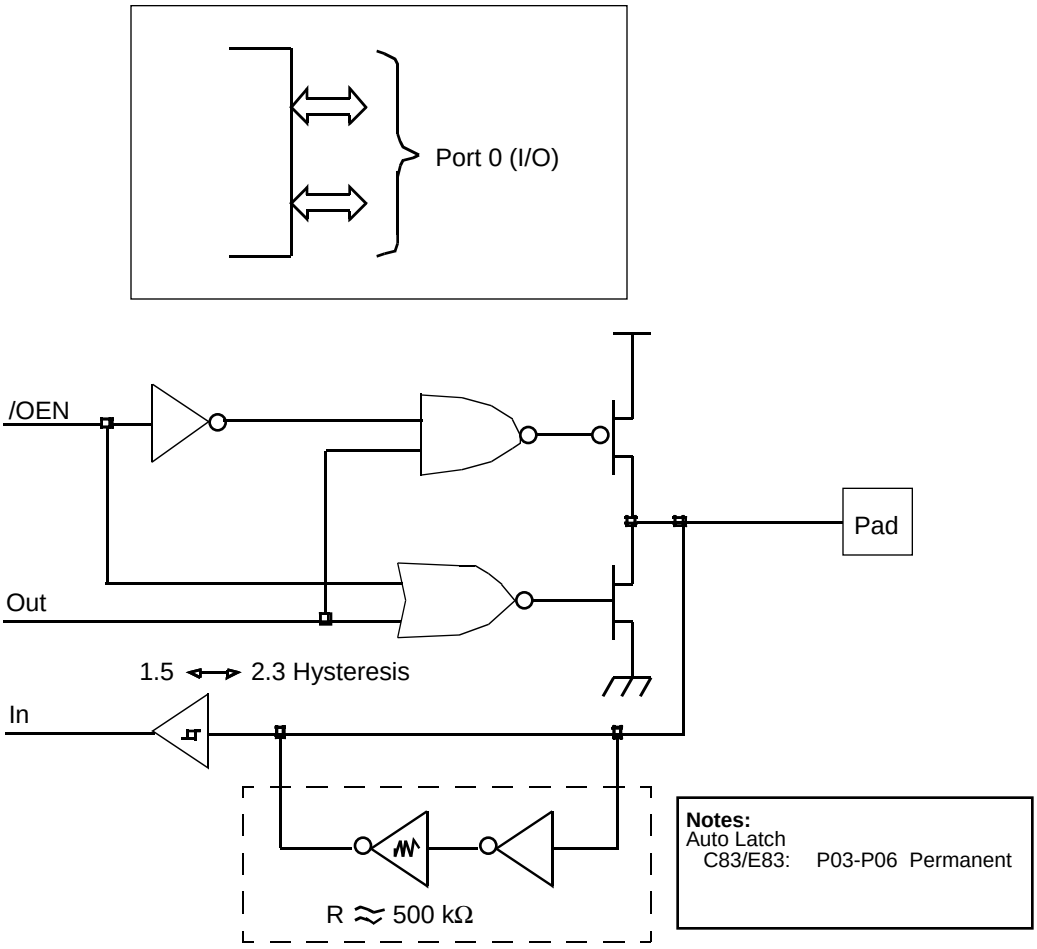


Figure 10. Port 0 Configuration

Port Configuration Register (PCON). The PCON configures the ports individually for comparator output on Port 3. The PCON Register is located in the Expanded Register File at Bank F, location 00 (Figure 13).

Bit 0 multiplexes comparator AN1 Output at P34. A "1" in this location brings the comparator output to P34 (Figure 14), and a "0" puts P34 into its standard I/O configuration.

Note: Only comparator output AN1 is multiplexed to a Port 3 output. Comparator AN2 output is not connected to any pins. Note that the PCON Register is reset upon the occurrence of a WDT RESET (not in STOP Mode), and Power-On Reset (POR).

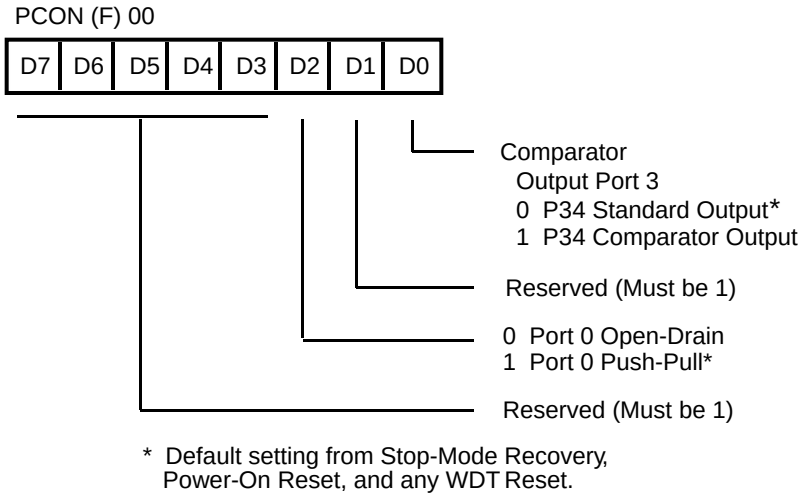


Figure 13. Port Configuration Register (PCON) (Write-Only)

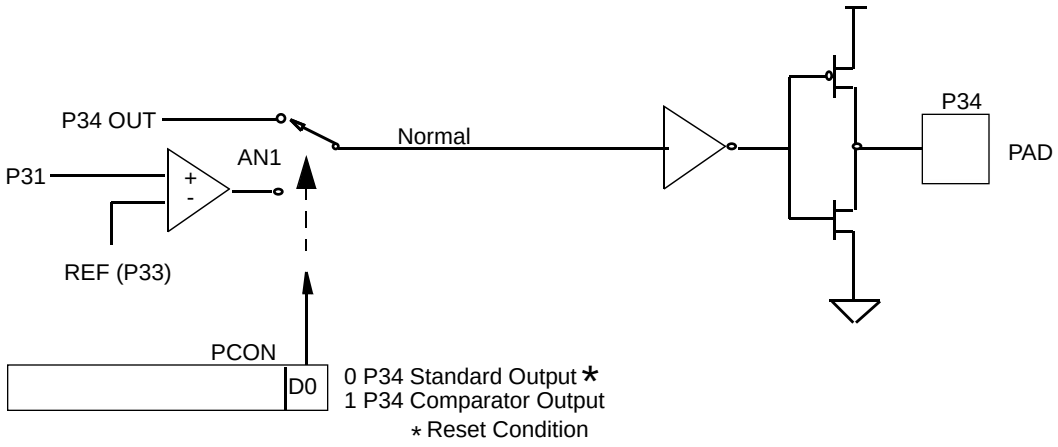


Figure 14. Port 3 P34 Output Configuration

FUNCTIONAL DESCRIPTION (Continued)

The D/A conversion for DAC1 is driven by writing 8-bit data to the DAC1 data register (Bank C, Register 06H). The D/A conversion for DAC2 is controlled by the DAC2 data register (Bank C, Register 07H). Each DAC data register is initialized to midrange 80H on power-up.

There are two DAC control registers: DACR1 (Bank C, Register 04H) for DAC1, and DACR2 (Bank C, Register 05H) for DAC2. Control register bits 0 and 1 set the DAC gain. When DAC data is 80H, the DAC output is constant for any gain setting (Figure 29 and Figure 31).

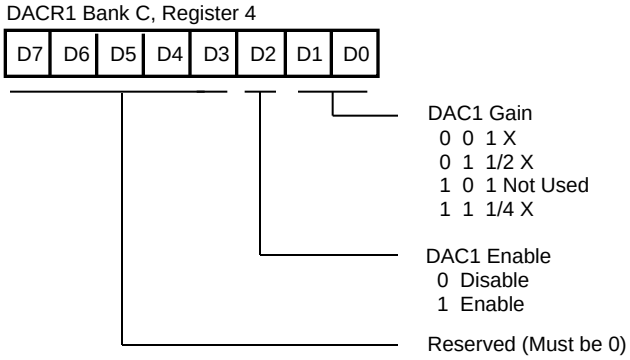


Figure 29. D/A 1 Control Register

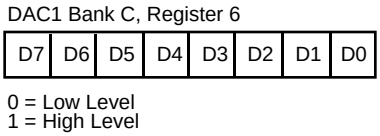


Figure 30. D/A 1 Data Register

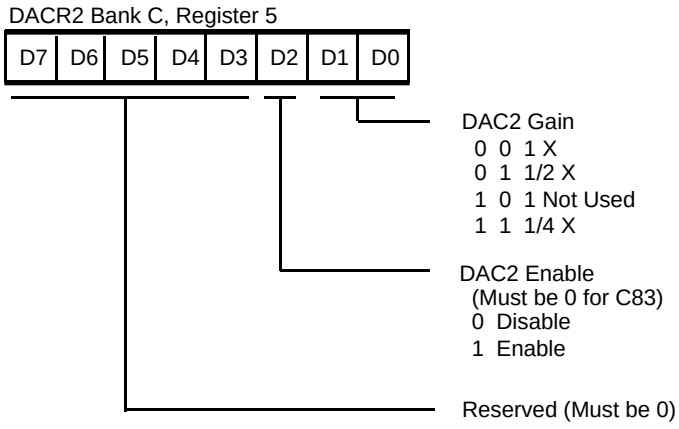


Figure 31. D/A 2 Control Register

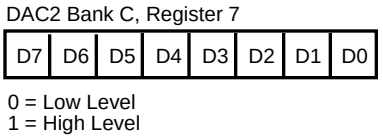


Figure 32. D/A 2 Data Register

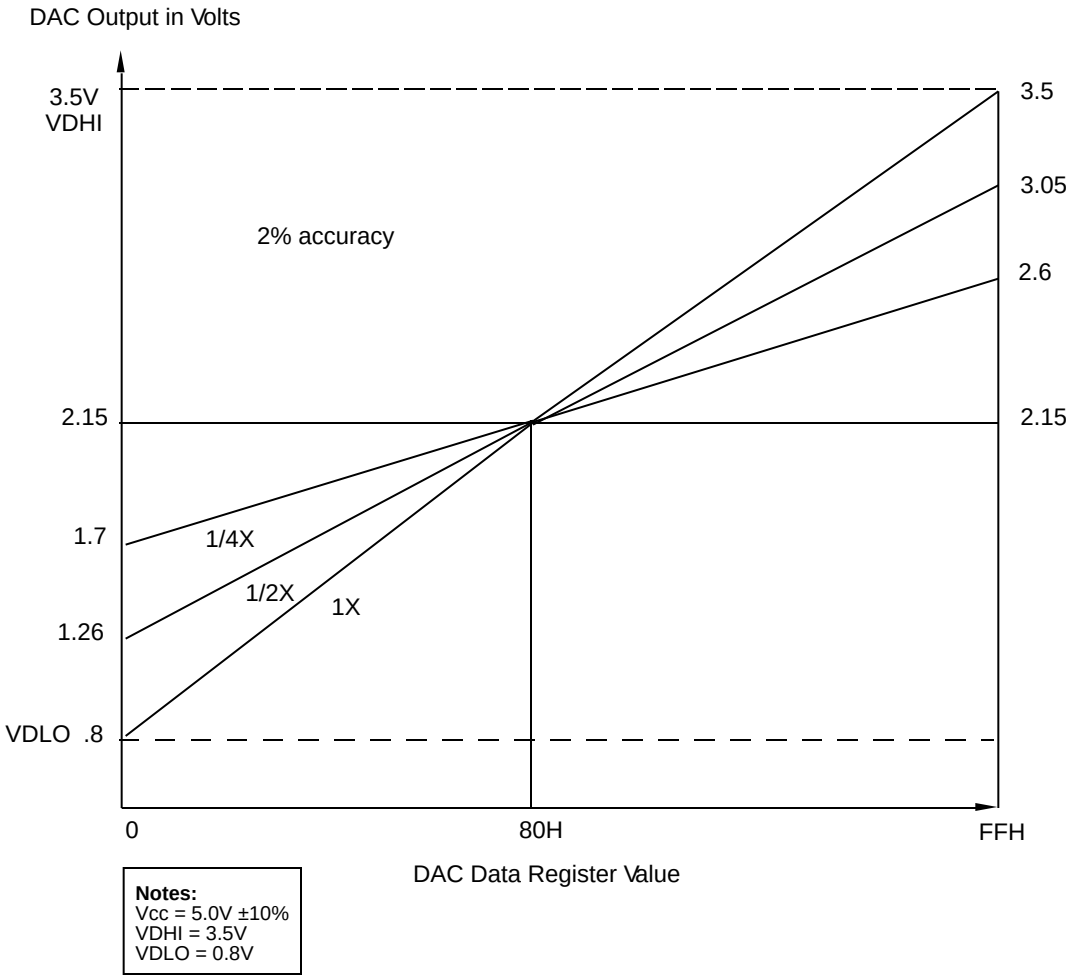


Figure 33. Gain Control on DAC

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator or by the XTAL oscillator is used for the POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK Status
- Stop-Mode Recovery (If D5 of SMR Register = 1)
- WDT Time-Out (Including from STOP Mode)

The POR time is T_{POR} minimum. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock and LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated (a POR or a WDT time-out). An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT. In case of a POR or a WDT time-out, program execution will restart at address 000CH.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA (typical) or less. The STOP Mode is terminated by a reset of either WDT time-out, POR, or Stop-Mode Recovery. This causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, that is**,**

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                        or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Stop-Mode Recovery (SMR) Register. This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 34 and Figure 35). All bits are Write-Only, except bit 7, which is Read-Only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4, or the SMR Register, specify the source of the Stop-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT. The SMR Register is located in Bank F of the Expanded Register Group at address 0BH. When the Stop-Mode Recovery sources are selected in this register, then SMR2 Register bits D0,D1 must be set to 0.

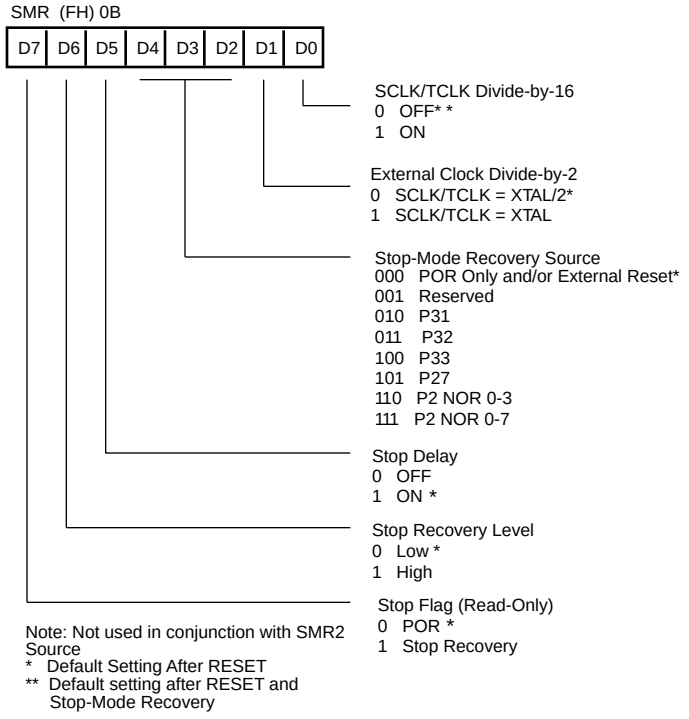


Figure 34. Stop-Mode Recovery Register (Write-Only Except Bit D7, Which Is Read-Only)

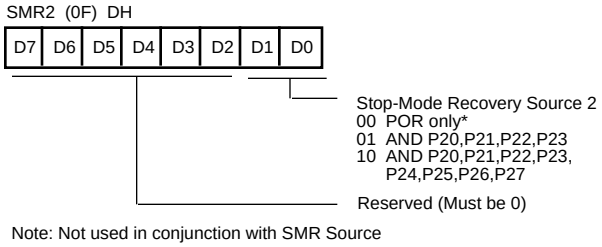


Figure 35. Stop-Mode Recovery Register 2 ([0F] DH: Write-Only)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The control selectively reduces device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic). This bit is reset to D0 = 0 after a Stop-Mode Recovery, WDT Time-out, and POR.

External Clock Divide-by-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock HALT Mode frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (that is, D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero. Maximum external clock frequency is 8 MHz when SMR Bit D1 = 1 where SCLK/TCLK = XTAL.

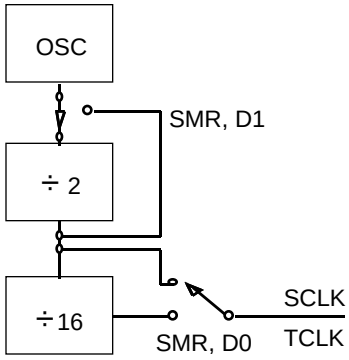


Figure 36. SCLK Circuit

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 38).

WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags. The WDTMR must be written to within 64 internal system clocks. After that, the WDTMR is write protected.

Note: WDT time-out while in Stop-Mode will not reset SMR, PCON, WDTMR, P2M, P3M, Ports 2 and 3 Data Registers, but will cause the reset delay to occur.

The Power-On Reset (POR) clock source is selected with bit 4 of the WDTMR. Bits 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to "1," the WDT is only driven by the external clock during STOP Mode. This feature makes it possible to wake up from STOP Mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 39). This register is accessible only during the first 60 processor cycles (60 SCLKs) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset or a Stop-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register group at address location 0FH.

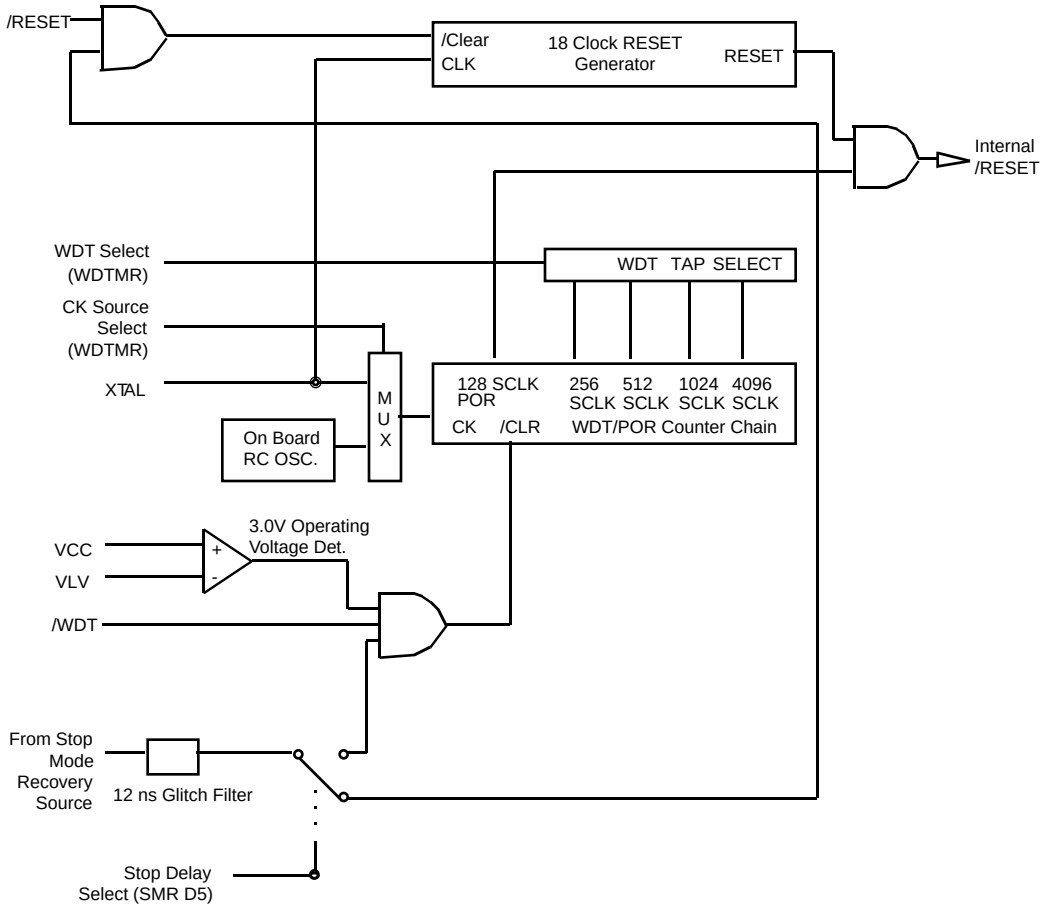


Figure 38. Resets and WDT

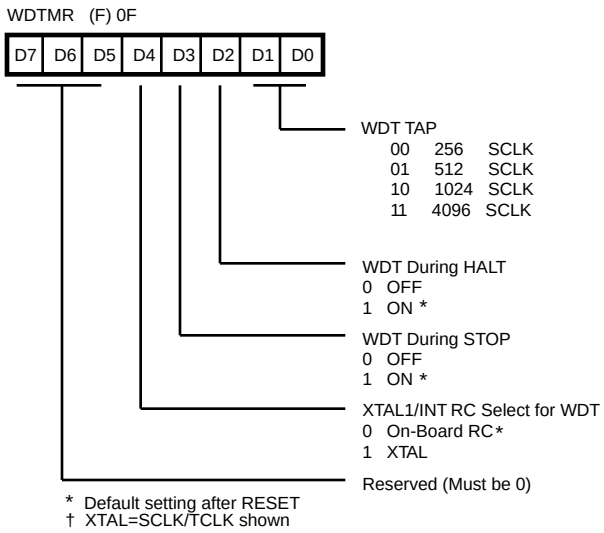


Figure 39. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D1, D0). Selects the WDT time-out period. It is configured as shown in Table 15.

Table 15. WDT Time Select (Min. @ 5.0V)

D1	D0	Time-Out of Internal RC OSC	Time-Out of SCLK Clock
0	0	6.25 ms min	256 SCLK
0	1	12.5 ms min	512 SCLK
1	0	25 ms min	1024 SCLK
1	1	100 ms min	4096 SCLK

Note: The minimum time shown is for V_{CC} @ 5.0V.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. The default is "1".

Note: If WDT is permanently selected (always ON mode), the WDT will continue to run even if set not to run in STOP or HALT Mode.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC has to be selected as the clock source to the POR counter. A "1" indicates active during STOP. The default is "1". If bits D3 and D4 are both set to "1", the WDT only, is driven by the external clock during STOP Mode.

Notes:

1. If WDT is permanently selected (always ON mode) using internal on-board RC oscillator, the WDT will continue to run even if set not to run in STOP or HALT Mode.

2. WDT instructions affect the Z (Zero), S (Sign), and V (Overflow) flags.

On-Board, Power-On-Reset RC or External XTAL1 Oscillator Select (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a "1", the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. If the XTAL1 pin is selected as the oscillator source for the WDT, during STOP Mode, the oscillator will be stopped and the WDT will not run. This is true even if the WDT is selected to run during STOP Mode.

V_{CC} Voltage Comparator. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. RESET is globally driven if V_{CC} is below the specified voltage (typically 2.6V).

ROM Protect. ROM Protect is mask or OTP bit-programmable. It is selected by the customer at the time the ROM code is submitted.

ROM Mask Selectable Options

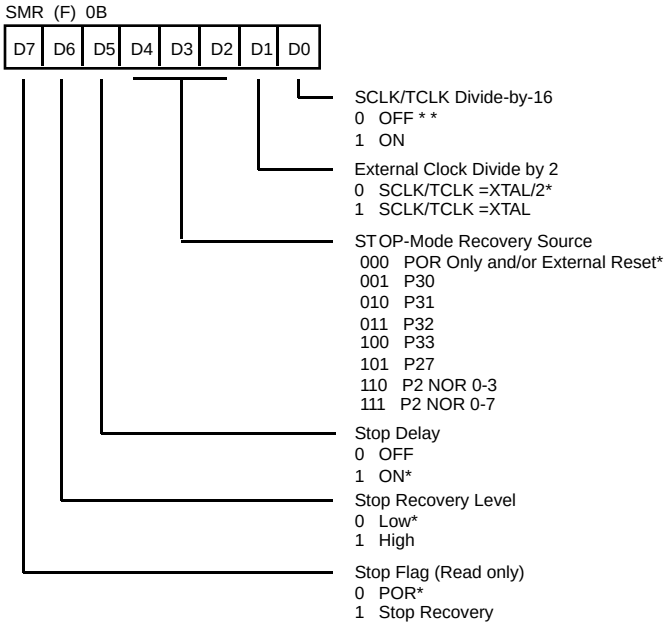
There are two ROM mask options that must be selected at the time the ROM mask is ordered (ROM code submitted) for the Z86C83/C84 and three Z86E83 OTP bit options.

Table 16. Selectable Options

Option	Selection
Permanent WDT	Yes/No
ROM Protect	Yes/No
EPROM/TEST Mode Disable*	Yes/No

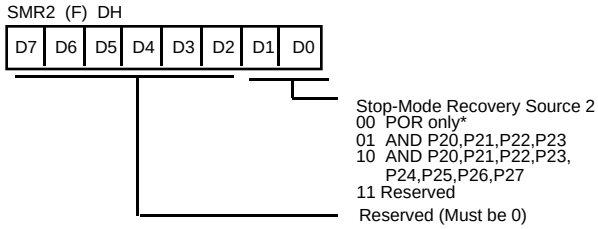
Note:
*For Z86E83 only
EPROM/TEST Mode Disable - On the Z86E83, the user can permanently disable entry into EPROM Mode and TEST Mode by programming this bit.

EXPANDED REGISTER FILE CONTROL REGISTERS



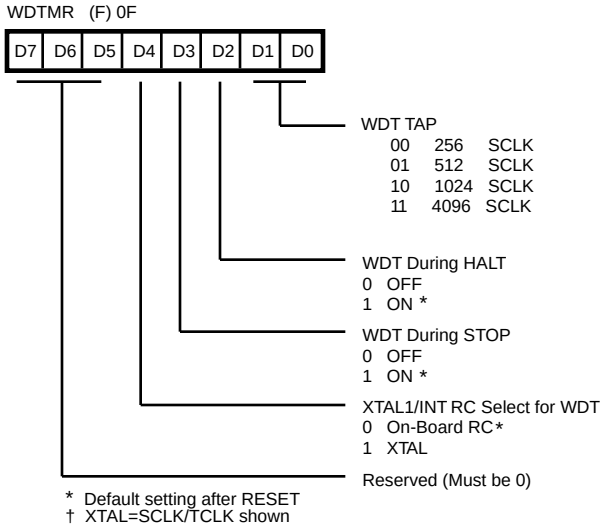
Note: Not used in conjunction with SMR2 Source
* Default setting after RESET.
* * Default setting after RESET and STOP-Mode Recovery.

Figure 47. Stop-Mode Recovery Register (Write-Only, except Bit 7 which is Read-Only)



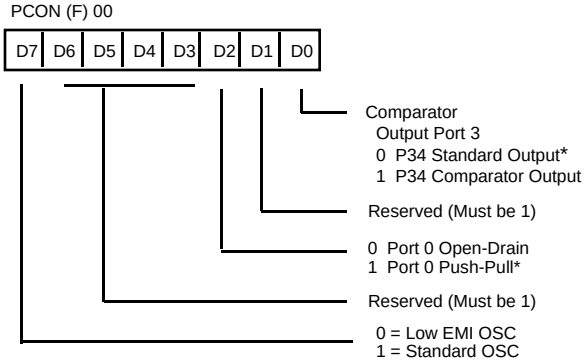
Note: Not used in conjunction with SMR Source

Figure 48. Watch-Dog Timer Mode Register 2



* Default setting after RESET
† XTAL=SCLK/TCLK shown

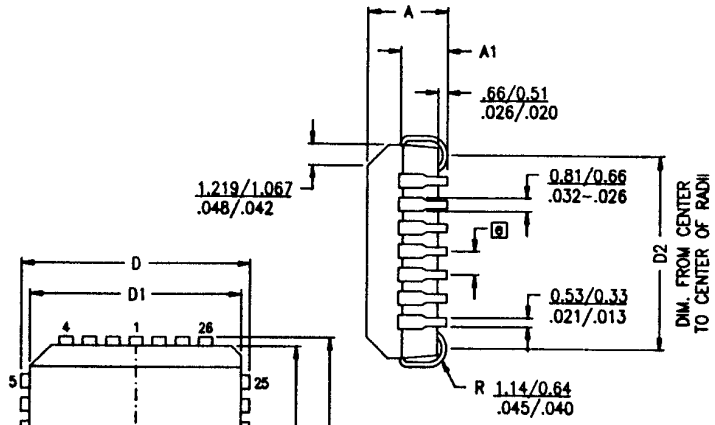
Figure 49. Watch-Dog Timer Mode Register (Write-Only)



* Default setting from Stop-Mode Recovery
Power-On Reset, and any WDT Reset.

Figure 50. Port Configuration Register (PCON) (Write-Only)

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	4.57	.165	.180
A1	2.41	2.92	.095	.115
D/E	12.32	12.57	.485	.495
D1/E1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
G	1.27 TYP		.050 TYP	

NOTES.
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 INCH.
3. DIMENSION : MM / INCH

Figure 70. 28-Pin PLCC Package Diagram

Zilog, Inc. 210 East Hacienda Ave.
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Telephone (408) 370-8000
FAX 408 370-8056