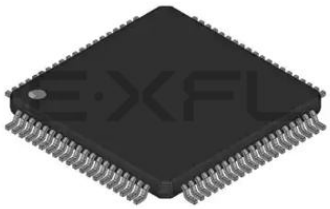
Infineon Technologies - XC2331D20F66LAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2331d20f66laakxuma1

XC233[01]D Data Sheet

Revision History: V1.3 2015-02

Previous Versions:
V1.0 2010-12
V1.1 2011-09
V1.2 2012-07

Page	Subjects (major changes since last revision)
6	Added SAK-XC2331D-20FxLR to Basic Device Types.
7	Moved SAK-XC2331D-20FxL from Basic Device Types to Special Device Types.
104	Added package type PG-LQFP-64-24.

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16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

XC233[01]D (XC2000 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XC233[01]D are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle @ 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1,024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels providing 64 interrupt nodes
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - 6 Kbytes on-chip data SRAM (DSRAM)
  - 4 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 160 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC) for Flash memory and through parity for RAMs

1.3 Definition of Feature Variants

The XC233[01]D types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
160 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C2'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$
96 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'0FFF_H$	$C4'0000_H$ … $C4'7FFF_H$

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
160	128	32
96	64	32

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC233[01]D types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
19 ADC0 channels	CH[11:0], CH13, CH[20:15]
2 CAN nodes	CAN0, CAN1 32 message objects
4 serial channels	U0C0, U0C1, U1C0, U1C1

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
44	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
45	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
46	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1D	I	St/B	**CAN Node 1 Receive Data Input**

3.1 Memory Subsystem and Organization

The memory space of the XC233[01]D is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC233[01]D **Memory Map** [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 bytes	
Reserved	$F0'0000_H$	$FF'FEFF_H$	< 1 Mbyte	Minus IMB registers.
Reserved for EPSRAM	$E8'1000_H$	$EF'FFFF_H$	508 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'0FFF_H$	up to 4 Kbytes	With Flash timing.
Reserved for PSRAM	$E0'1000_H$	$E7'FFFF_H$	508 Kbytes	Mirrors PSRAM
PSRAM	$E0'0000_H$	$E0'0FFF_H$	up to 4 Kbytes	Program SRAM.
Reserved for Flash	$C4'8000_H$	$DF'FFFF_H$	1760 Kbytes	
Flash 1	$C4'0000_H$	$C4'7FFF_H$	32 Kbytes	
Reserved for Flash	$C2'1000_H$	$C3'FFFF_H$	124 Kbytes	
Flash 0	$C0'0000_H$	$C2'0FFF_H$	132 Kbytes[3)]	
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	
External IO area[4)]	$21'0000_H$	$3F'FFFF_H$	1984 Kbytes	
Reserved	$20'B800_H$	$20'FFFF_H$	18 Kbytes	
USIC0-1 alternate regs.	$20'B000_H$	$20'B7FF_H$	2 Kbytes	Accessed via LXBus Controller
MultiCAN alternate regs.	$20'8000_H$	$20'AFFF_H$	12 Kbytes	Accessed via LXBus Controller
Reserved	$20'5000_H$	$20'7FFF_H$	12 Kbytes	
USIC0-1 registers	$20'4000_H$	$20'4FFF_H$	4 Kbytes	Accessed via LXBus Controller
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via LXBus Controller
External memory area	$01'0000_H$	$1F'FFFF_H$	1984 Kbytes	
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbytes	
Dual-port RAM (DPRAM)	$00'F600_H$	$00'FDFF_H$	2 Kbytes	
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbytes	

3.9 General Purpose Timer (GPT12E) Unit

The GPT12E unit is a very flexible multifunctional timer/counter structure which can be used for many different timing tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers organized in two separate modules, GPT1 and GPT2. Each timer in each module may either operate independently in a number of different modes or be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation: Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock and divided by a programmable prescaler. Counter Mode allows timer clocking in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes each timer has one associated port pin (TxIN) which serves as a gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The counting direction (up/down) for each timer can be programmed by software or altered dynamically by an external signal on a port pin (TxEUD), e.g. to facilitate position tracking.

In Incremental Interface Mode the GPT1 timers can be directly connected to the incremental position sensor signals A and B through their respective inputs TxIN and TxEUD. Direction and counting signals are internally derived from these two input signals, so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to the basic operating modes, T2 and T4 may be configured as reload or capture register for timer T3. A timer used as capture or reload register is stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at the associated input pin (TxIN). Timer T3 is reloaded with the contents of T2 or T4, triggered either by an external signal or a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be continuously generated without software intervention.

Note: Signals T2IN, T2EUD, T4EUD, T6IN and T6EUD are not connected to pins.

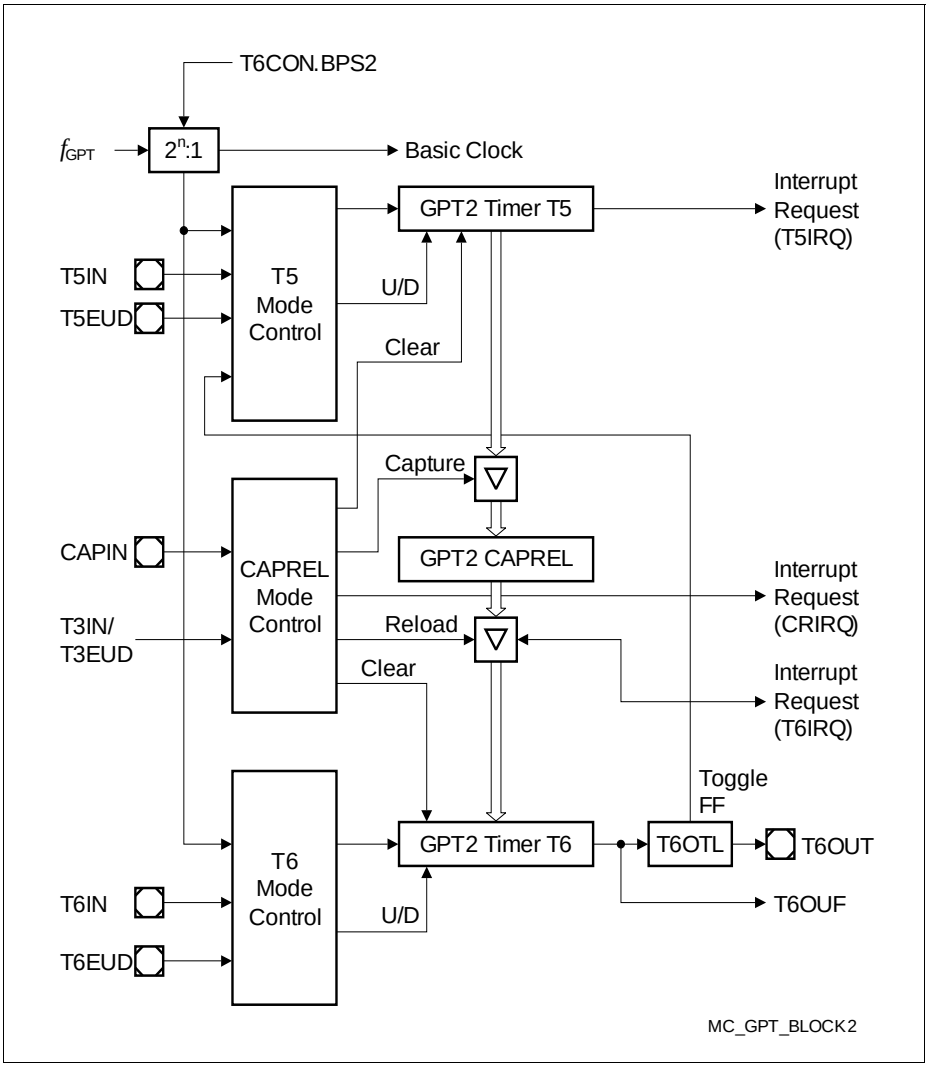

Figure 8 Block Diagram of GPT2

3.10 Real Time Clock

The Real Time Clock (RTC) module of the XC233[01]D can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  – a reloadable 10-bit timer
  – a reloadable 6-bit timer
  – a reloadable 6-bit timer
  – a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

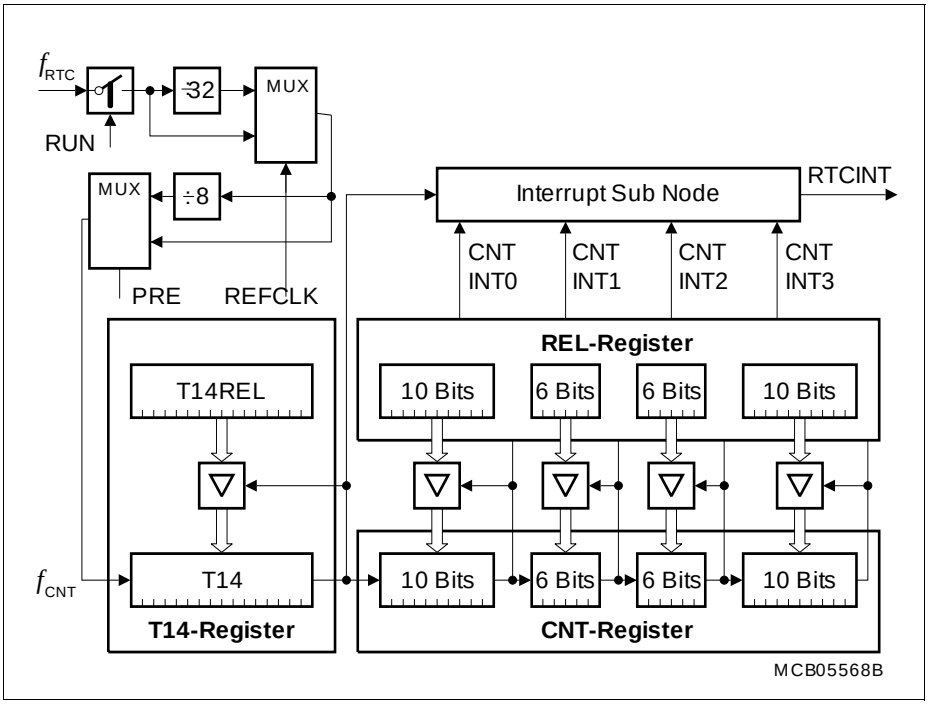

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

8) Value is controlled by on-chip regulator.

4.2 Voltage Range definitions

The XC233[01]D timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5.0	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC233[01]D and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC233[01]D provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC233[01]D.

4.3 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

The XC233[01]D can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1$ V/ms.

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XC233[01]D are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in **Section 4.7.4**.

4.3.1 DC Parameters for Upper Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Note: Operating Conditions apply.

Table 16 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 16 DC Characteristics for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs).	C_{IO} CC	–	–	10	pF	not subject to production test
Input Hysteresis[1)]	HYS CC	0.11 x V_{DDP}	–	–	V	R_S= 0 Ohm
Absolute input leakage current on pins of analog ports[2)]	$\|I_{OZ1}\|$ CC	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. [2)3)]	$\|I_{OZ2}\|$ CC	–	0.2	5	µA	$T_J \leq$ 110 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	10	µA	$T_J \leq$ 150 °C; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current[4)]	$\|I_{PLF}\|$ SR	220	–	–	µA	$V_{IN} \geq V_{IHmin}$ *(pulldown_enabled)*; $V_{IN} \leq V_{ILmax}$ *(pullup_enabled)*
Pull Level Keep Current[5)]	$\|I_{PLK}\|$ SR	–	–	30	µA	$V_{IN} \geq V_{IHmin}$ *(pullup_enabled)*; $V_{IN} \leq V_{ILmax}$ *(pulldown_enabled)*
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	

4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 20 ADC Parameters for All Voltage Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	9	20	pF	not subject to production test [1]
Total capacitance at an analog input	C_{AINT} CC	–	20	30	pF	not subject to production test [1]
Switched capacitance at the reference input	C_{AREFSW} CC	–	15	30	pF	not subject to production test [1]
Total capacitance at the reference input	C_{AREFT} CC	–	20	40	pF	not subject to production test [1]
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(10 + STC x t_{ADCI} + 2 x t_{SYS}				
Conversion time for 10-bit result[2]	t_{c10} CC	(12 + STC x t_{ADCI} + 2 x t_{SYS}				
Conversion time for 12-bit result[2]	t_{c12} CC	(16 + STC x t_{ADCI} + 2 x t_{SYS}				
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[5]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPB} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.
3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H)
4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H)
5) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

Table 21 ADC Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input resistance of the selected analog channel	R_{AIN} CC	–	0.9	1.5	kOhm	not subject to production test 1)
Input resistance of the reference input	R_{AREF} CC	–	0.5	1	kOhm	not subject to production test 1)
Differential Non-Linearity Error 2)3)4)5)	$\|EA_{DNL}\|$ CC	–	2.5	5.0	LSB	
Gain Error 2)3)4)5)	$\|EA_{GAIN}\|$ CC	–	2.5	6.0	LSB	
Integral Non-Linearity 2)3)4)5)	$\|EA_{INL}\|$ CC	–	2.0	4.0	LSB	
Offset Error 2)3)4)5)	$\|EA_{OFF}\|$ CC	–	2.0	4.0	LSB	
Analog clock frequency	f_{ADCI} SR	2	–	20	MHz	Std. reference input (V_{AREF})
		2	–	17.5	MHz	Alt. reference input (CH0)
Total Unadjusted Error 3)4)	|TUE| CC	–	2.5	5.5	LSB	6)7)
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	7.0	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	11.5	µs	

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 25 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V - 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

Table 26 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B - 011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

4.6 Flash Memory Parameters

The XC233[01]D is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC233[01]D's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	2[1)]		$N_{FL\_RD} \leq 1$
		–	–	1[2)]		$N_{FL\_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq$ 20 years
Flash wait states[3)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq$ 8 MHz
		2	–	–		$f_{SYS} \leq$ 13 MHz
		3	–	–		$f_{SYS} \leq$ 17 MHz
		4	–	–		$f_{SYS} >$ 17 MHz
Erase time per sector/page	t_{ER} CC	–	7[4)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[4)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{ER} \leq$ 1,000 cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

Table 27 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{ER} SR	–	–	15000	cycles	$t_{RET} \geq$ 5 years; Valid for up to 64 user selected sectors (data storage)
		–	–	1000	cycles	$t_{RET} \geq$ 20 years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC233[01]D Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7.4 Pad Properties

The output pad drivers of the XC233[01]D can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 30 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	3.0	mA	Driver_Strength = Medium
		–	–	5.0	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	1.6	mA	Driver_Strength = Strong
		–	–	0.25	mA	Driver_Strength = Weak

Table 37 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 37 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	100[1)]	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	87	92	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

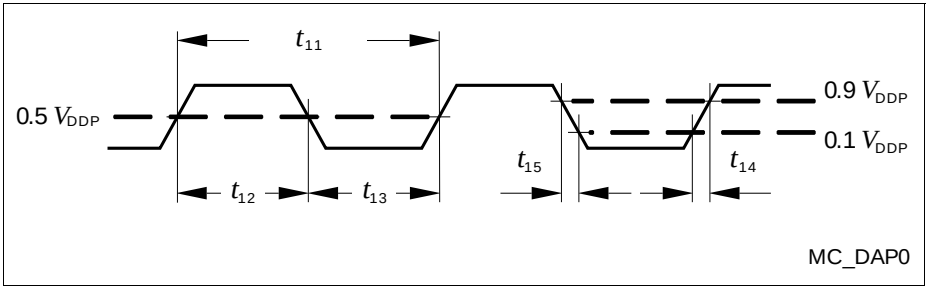

Figure 22 Test Clock Timing (DAP0)

5 Package and Reliability

The XC2000 Family devices use the package type:

- PG-LQFP (Plastic Green - Low Profile Quad Flat Package)

The following specifications must be regarded to ensure proper integration of the XC233[01]D in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 40 Package Parameters (PG-LQFP-64-22/-24)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	5.4 × 5.4	mm	–
Power Dissipation	P_{DISS}	–	0.7	W	–
Thermal resistance Junction-Ambient	$R_{\Theta JA}$	–	65	K/W	No thermal via, 2-layer[1)]
			47	K/W	No thermal via, 4-layer[2)]
			45	K/W	4-layer, no pad[3)]
			32	K/W	4-layer, pad[4)]

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) without thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

4) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.
Board layout examples are given in an application note.

Package Compatibility Considerations

The XC233[01]D is a member of the XC2000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In