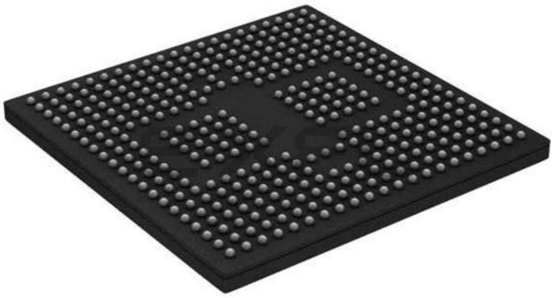

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit 24-Core
Speed	4000MIPS
Connectivity	-
Peripherals	-
Number of I/O	176
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	374-LFBGA
Supplier Device Package	374-FBGA (18x18)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xlf224-1024-fb374-c40

on events generated by hardware resources such as the I/O pins, communication channels and timers. Once triggered, a core runs independently and concurrently to other cores, until it pauses to wait for more events. Section 6.2

- **Channels and channel ends** Tasks running on logical cores communicate using channels formed between two channel ends. Data can be passed synchronously or asynchronously between the channel ends assigned to the communicating tasks. Section 6.5
- **xCONNECT Switch and Links** Between tiles, channel communications are implemented over a high performance network of xCONNECT Links and routed through a hardware xCONNECT Switch. Section 6.6
- **Ports** The I/O pins are connected to the processing cores by Hardware Response ports. The port logic can drive its pins high and low, or it can sample the value on its pins optionally waiting for a particular condition. Section 6.3
- **Clock blocks** xCORE devices include a set of programmable clock blocks that can be used to govern the rate at which ports execute. Section 6.4
- **Memory** Each xCORE Tile integrates a bank of SRAM for instructions and data, and a block of one-time programmable (OTP) memory that can be configured for system wide security features. Section 9
- **PLL** The PLL is used to create a high-speed processor clock given a low speed external oscillator. Section 7
- **Flash** The device has a built-in 2MBflash. Section 8
- **JTAG** The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory. Section 10

1.1 Software

Devices are programmed using C, C++ or xC (C with multicore extensions). XMOS provides tested and proven software libraries, which allow you to quickly add interface and processor functionality such as USB, Ethernet, PWM, graphics driver, and audio EQ to your applications.

1.2 xTIMEcomposer Studio

The xTIMEcomposer Studio development environment provides all the tools you need to write and debug your programs, profile your application, and write images into flash memory or OTP memory on the device. Because xCORE devices operate deterministically, they can be simulated like hardware within xTIMEcomposer: uniquely in the embedded world, xTIMEcomposer Studio therefore includes a static timing analyzer, cycle-accurate simulator, and high-speed in-circuit instrumentation.

xTIMEcomposer can be driven from either a graphical development environment, or the command line. The tools are supported on Windows, Linux and MacOS X

4 Signal Description

This section lists the signals and I/O pins available on the XLF224-1024-FB374. The device provides a combination of 1bit, 4bit, 8bit and 16bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

- PD/PU: The IO pin has a weak pull-down or pull-up resistor. On GPIO pins this resistor can be enabled. This resistor is designed to ensure defined logic input state for unconnected pins. It should not be used to pull external circuitry. Note that the resistors are highly non-linear and only a maximum pull current is specified in Section 12.2.
- ST: The IO pin has a Schmitt Trigger on its input.
- IOT: The IO pin is powered from VDDIOT (X1) or VDDIOT_2 (X3), not VDDIO
- IO: the pin is powered from VDDIO

Power pins (9)			
Signal	**Function**	**Type**	**Properties**
GND	Digital ground	GND	
OTP_VCC	OTP power supply	PWR	
PLL_AGND	Analog ground for PLL	PWR	
PLL_AVDD	Analog PLL power	PWR	
VDD	Digital tile power	PWR	
VDD33	Peripheral power	PWR	
VDDIO	Digital I/O power	PWR	
VDDIOT	Digital I/O power (top)	PWR	
VDDIOT_2	Digital I/O power (top, X3)	PWR	

JTAG pins (6)			
Signal	**Function**	**Type**	**Properties**
RST_N	Global reset input	Input	IO, PU, ST
TCK	Test clock	Input	IO, PD, ST
TDI	Test data input	Input	IO, PU
TDO	Test data output	Output	IO, PD
TMS	Test mode select	Input	IO, PU
TRST_N	Test reset input	Input	IO, PU, ST

Signal	Function	Type	Properties
X1D67	$X_0L2^{1}_{out}$ $32A^{16}$	I/O	IO, PD
X1D68	$X_0L2^{2}_{out}$ $32A^{17}$	I/O	IO, PD
X1D69	$X_0L2^{3}_{out}$ $32A^{18}$	I/O	IO, PD
X1D70	$X_0L2^{4}_{out}$ $32A^{19}$	I/O	IO, PD
X2D00	$1A^{0}$	I/O	IO, PD
X2D02	$4A^{0}$ $8A^{0}$ $16A^{0}$ $32A^{20}$	I/O	IO, PD
X2D03	$4A^{1}$ $8A^{1}$ $16A^{1}$ $32A^{21}$	I/O	IO, PD
X2D04	$4B^{0}$ $8A^{2}$ $16A^{2}$ $32A^{22}$	I/O	IO, PD
X2D05	$4B^{1}$ $8A^{3}$ $16A^{3}$ $32A^{23}$	I/O	IO, PD
X2D06	$4B^{2}$ $8A^{4}$ $16A^{4}$ $32A^{24}$	I/O	IO, PD
X2D07	$4B^{3}$ $8A^{5}$ $16A^{5}$ $32A^{25}$	I/O	IO, PD
X2D08	$4A^{2}$ $8A^{6}$ $16A^{6}$ $32A^{26}$	I/O	IO, PD
X2D09	$4A^{3}$ $8A^{7}$ $16A^{7}$ $32A^{27}$	I/O	IO, PD
X2D11	$1D^{0}$	I/O	IO, PD
X2D12	$1E^{0}$	I/O	IO, PD
X2D13	$1F^{0}$	I/O	IO, PD
X2D14	$4C^{0}$ $8B^{0}$ $16A^{8}$ $32A^{28}$	I/O	IO, PD
X2D15	$4C^{1}$ $8B^{1}$ $16A^{9}$ $32A^{29}$	I/O	IO, PD
X2D16	$X_2L4^{4}_{in}$ $4D^{0}$ $8B^{2}$ $16A^{10}$	I/O	IO, PD
X2D17	$X_2L4^{3}_{in}$ $4D^{1}$ $8B^{3}$ $16A^{11}$	I/O	IO, PD
X2D18	$X_2L4^{2}_{in}$ $4D^{2}$ $8B^{4}$ $16A^{12}$	I/O	IO, PD
X2D19	$X_2L4^{1}_{in}$ $4D^{3}$ $8B^{5}$ $16A^{13}$	I/O	IO, PD
X2D20	$4C^{2}$ $8B^{6}$ $16A^{14}$ $32A^{30}$	I/O	IO, PD
X2D21	$4C^{3}$ $8B^{7}$ $16A^{15}$ $32A^{31}$	I/O	IO, PD
X2D22	$1G^{0}$	I/O	IO, PD
X2D23	$1H^{0}$	I/O	IO, PD
X2D24	$X_2L7^{0}_{in}$ $1I^{0}$	I/O	IO, PD
X2D25	$X_2L7^{0}_{out}$ $1J^{0}$	I/O	IO, PD
X2D26	$X_2L7^{3}_{out}$ $4E^{0}$ $8C^{0}$ $16B^{0}$	I/O	IO, PD
X2D27	$X_2L7^{4}_{out}$ $4E^{1}$ $8C^{1}$ $16B^{1}$	I/O	IO, PD
X2D28	$4F^{0}$ $8C^{2}$ $16B^{2}$	I/O	IO, PD
X2D29	$4F^{1}$ $8C^{3}$ $16B^{3}$	I/O	IO, PD
X2D30	$4F^{2}$ $8C^{4}$ $16B^{4}$	I/O	IO, PD
X2D31	$4F^{3}$ $8C^{5}$ $16B^{5}$	I/O	IO, PD
X2D32	$4E^{2}$ $8C^{6}$ $16B^{6}$	I/O	IO, PD
X2D33	$4E^{3}$ $8C^{7}$ $16B^{7}$	I/O	IO, PD
X2D34	$X_2L7^{1}_{out}$ $1K^{0}$	I/O	IO, PD
X2D35	$X_2L7^{2}_{out}$ $1L^{0}$	I/O	IO, PD
X2D36	$1M^{0}$ $8D^{0}$ $16B^{8}$	I/O	IO, PD
X2D49	$X_2L5^{4}_{in}$ $32A^{0}$	I/O	IO, PD
X2D50	$X_2L5^{3}_{in}$ $32A^{1}$	I/O	IO, PD
X2D51	$X_2L5^{2}_{in}$ $32A^{2}$	I/O	IO, PD
X2D52	$X_2L5^{1}_{in}$ $32A^{3}$	I/O	IO, PD

(continued)

Signal	Function						Type	Properties
X2D53	$X_2L5^0_{in}$					$32A^4$	I/O	IO, PD
X2D54	$X_2L5^0_{out}$					$32A^5$	I/O	IO, PD
X2D55	$X_2L5^1_{out}$					$32A^6$	I/O	IO, PD
X2D56	$X_2L5^2_{out}$					$32A^7$	I/O	IO, PD
X2D57	$X_2L5^3_{out}$					$32A^8$	I/O	IO, PD
X2D58	$X_2L5^4_{out}$					$32A^9$	I/O	IO, PD
X2D61	$X_2L6^4_{in}$					$32A^{10}$	I/O	IO, PD
X2D62	$X_2L6^3_{in}$					$32A^{11}$	I/O	IO, PD
X2D63	$X_2L6^2_{in}$					$32A^{12}$	I/O	IO, PD
X2D64	$X_2L6^1_{in}$					$32A^{13}$	I/O	IO, PD
X2D65	$X_2L6^0_{in}$					$32A^{14}$	I/O	IO, PD
X2D66	$X_2L6^0_{out}$					$32A^{15}$	I/O	IO, PD
X2D67	$X_2L6^1_{out}$					$32A^{16}$	I/O	IO, PD
X2D68	$X_2L6^2_{out}$					$32A^{17}$	I/O	IO, PD
X2D69	$X_2L6^3_{out}$					$32A^{18}$	I/O	IO, PD
X2D70	$X_2L6^4_{out}$					$32A^{19}$	I/O	IO, PD
X3D00	$X_2L7^2_{in}$	$1A^0$					I/O	IO, PD
X3D01	$X_2L7^1_{in}$	$1B^0$					I/O	IO, PD
X3D02	$X_2L4^0_{in}$		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	I/O	IO, PD
X3D03	$X_2L4^0_{out}$		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	I/O	IO, PD
X3D04	$X_2L4^1_{out}$		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	I/O	IO, PD
X3D05	$X_2L4^2_{out}$		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	I/O	IO, PD
X3D06	$X_2L4^3_{out}$		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	I/O	IO, PD
X3D07	$X_2L4^4_{out}$		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	I/O	IO, PD
X3D08	$X_2L7^4_{in}$		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	I/O	IO, PD
X3D09	$X_2L7^3_{in}$		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	I/O	IO, PD
X3D10		$1C^0$					I/O	IOT, PD
X3D11		$1D^0$					I/O	IOT, PD
X3D12		$1E^0$					I/O	IO, PD
X3D13		$1F^0$					I/O	IO, PD
X3D14			$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	I/O	IO, PD
X3D15			$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	I/O	IO, PD
X3D20			$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	I/O	IO, PD
X3D21			$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	I/O	IO, PD
X3D23		$1H^0$					I/O	IO, PD
X3D24		$1I^0$					I/O	IO, PD
X3D25		$1J^0$					I/O	IO, PD
X3D26			$4E^0$	$8C^0$	$16B^0$		I/O	IOT, PD
X3D27			$4E^1$	$8C^1$	$16B^1$		I/O	IOT, PD
X3D28			$4F^0$	$8C^2$	$16B^2$		I/O	IOT, PD
X3D29			$4F^1$	$8C^3$	$16B^3$		I/O	IOT, PD
X3D30			$4F^2$	$8C^4$	$16B^4$		I/O	IOT, PD
X3D31			$4F^3$	$8C^5$	$16B^5$		I/O	IOT, PD

(continued)

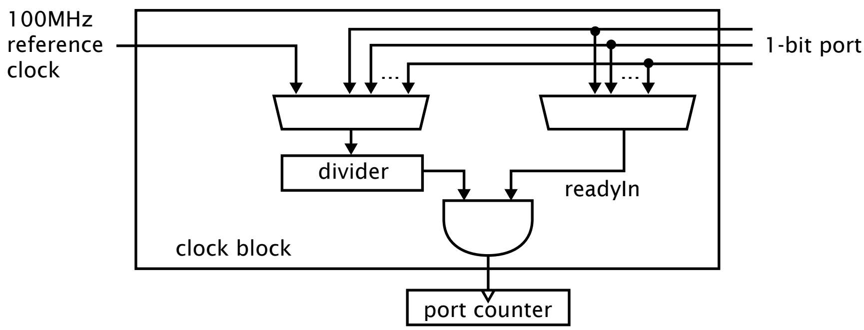

Figure 5: Clock block diagram

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming

Figure 7 also lists the values of OD, F and R, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

OD, F and R must be chosen so that $0 \leq R \leq 63$, $0 \leq F \leq 4095$, $0 \leq OD \leq 7$, and $260\,MHz \leq F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \leq 1.3GHz$. The OD, F, and R values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value during and after deassertion of the system reset.

If a different tile frequency is required (eg, 500 MHz), then the PLL must be reprogrammed after boot to provide the required tile frequency. The XMOS tools perform this operation by default. Further details on configuring the clock can be found in the xCORE-200 Clock Frequency Control document.

8 Boot Procedure

The device is kept in reset by driving RST_N low. When in reset, all GPIO pins have a pull-down enabled. The processor must be held in reset until VDDIOL is in spec for at least 1 ms. When the device is taken out of reset by releasing RST_N the processor starts its internal reset process. After 15-150 μs (depending on the input clock) the processor boots.

Pin X2D06 must be pulled high with an external pull-up whilst the chip comes out of reset, to ensure that tile 2 will boot from link. X2D04, X2D05, and X2D07 should be kept low whilst the chip comes out of reset.

The device boots from a QSPI flash (IS25LQ016B) that is embedded in the device. The QSPI flash is connected to the ports on Tile 0 as shown in Figure 8. An external 1K resistor must connect X0D01 to VDDIOL. X0D10 should ideally not be connected. If X0D10 is connected, then a 150 ohm series resistor close to the device is recommended. X0D04..X0D07 should be not connected.

Figure 8: QSPI port connectivity

The xCORE Tile boot procedure is illustrated in Figure 9. If bit 5 of the security register (see §9.1) is set, the device boots from OTP. Otherwise, the device boots from the internal flash.

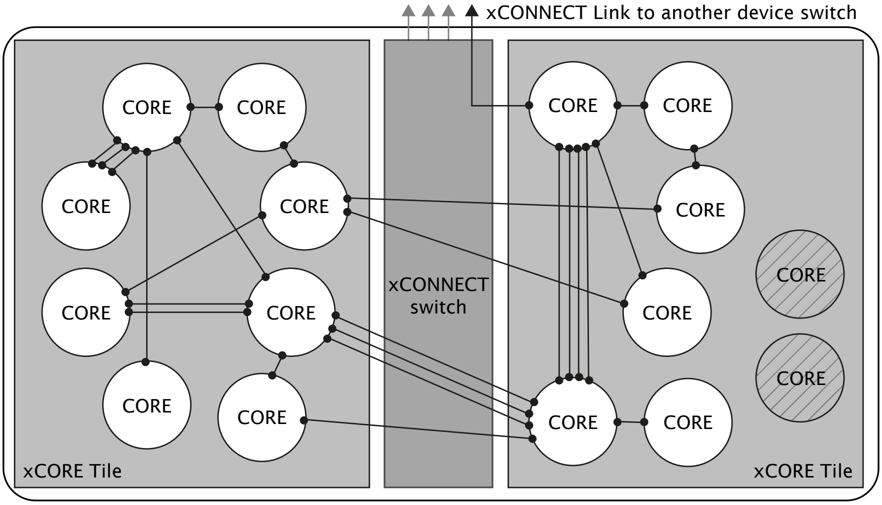

Figure 6: Switch, links and channel ends

and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-LF Link Performance and Design Guide, X2999.

7 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 7:

Figure 7: PLL multiplier values and MODE pins

Oscillator Frequency	MODE 1	MODE 0	Tile Frequency	PLL Ratio	PLL settings *OD*	*F*	*R*
3.25-10 MHz	0	0	130-400 MHz	40	1	159	0
9-25 MHz	1	1	144-400 MHz	16	1	63	0
25-50 MHz	1	0	167-400 MHz	8	1	31	0
50-100 MHz	0	1	196-400 MHz	4	1	15	0