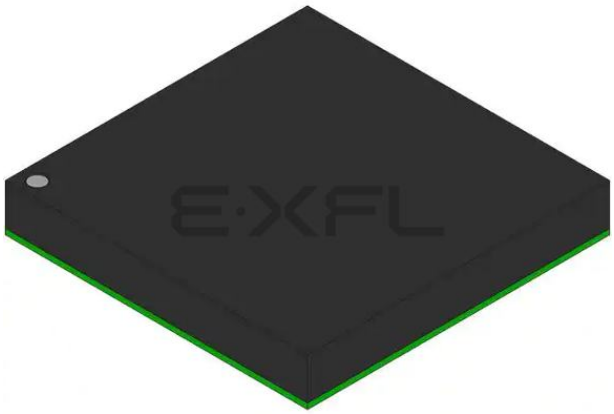


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 95°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx512cjm6c

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_INT_REQ	When using the MC13892 power management IC, the PMIC_INT_REQ high-priority interrupt input on i.MX51 should be either floated or tied to NVCC_SRTC_POW with a 4.7 kΩ to 68 kΩ resistor. This avoids a continuous current drain on the real-time clock backup battery due to a 100 kΩ on-chip pull-up resistor. PMIC_INT_REQ is not used by the Freescale BSP (board support package) software. The BSP requires that the general-purpose INT output from the MC13892 be connected to the i.MX51 GPIO input GPIO1_8 configured to cause an interrupt that is not high-priority. The original intent was for PMIC_INT_REQ to be connected to a circuit that detects when the battery is almost depleted. In this case, the I/O must be configured as alternate mode 0 (ALT0 = power fail).
POR_B	This cold reset negative logic input resets all modules and logic in the IC. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Memory repair – Configuration of memory repair per fuse settings • Cold reset logic of WDOG – Some WDOG logic is only reset by POR_B. See WDOG chapter in *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details.
RREFEXT	Determines the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required.
SGND, SVCC, and SVDDGP	These sense lines provide the ability to sense actual on-chip voltage levels on their respective supplies. SGND monitors differentials of the on-chip ground versus an external power source. SVCC monitors on-chip VCC, and SVDDGP monitors VDDGP. Freescale recommends connection of the SVCC and SVDDGP signals to the feedback inputs of switching power-supplies or to test points.
STR	This signal is reserved for Freescale manufacturing use. The user should float this signal.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

4.6 Module Timing

This section contains the timing and electrical parameters for the modules in the i.MX51 processor.

4.6.1 Reset Timings Parameters

Figure 12 shows the reset timing and Table 45 lists the timing parameters.

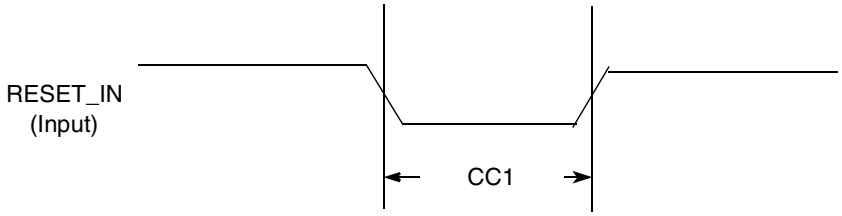


Figure 12. Reset Timing Diagram

Table 45. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN to be qualified as valid (input slope = 5 ns)	50	—	ns

4.6.5 DPLL Electrical Parameters

Table 48 shows the DPLL electrical parameters.

Table 48. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output Duty Cycle	—	48.5	50	51.5	%
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 47.

2 The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user.Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15.Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider.According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 Tdck is the time period of the output clock, dpdck_2.

4.6.6 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among different signals of NFC at the module level in the different operational modes.

Timing parameters in Figure 14, Figure 15, Figure 16, Figure 17, Figure 19, and Table 50 show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B. Timing parameters in Figure 14, Figure 15, Figure 16, Figure 18, Figure 19, and Table 50 show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

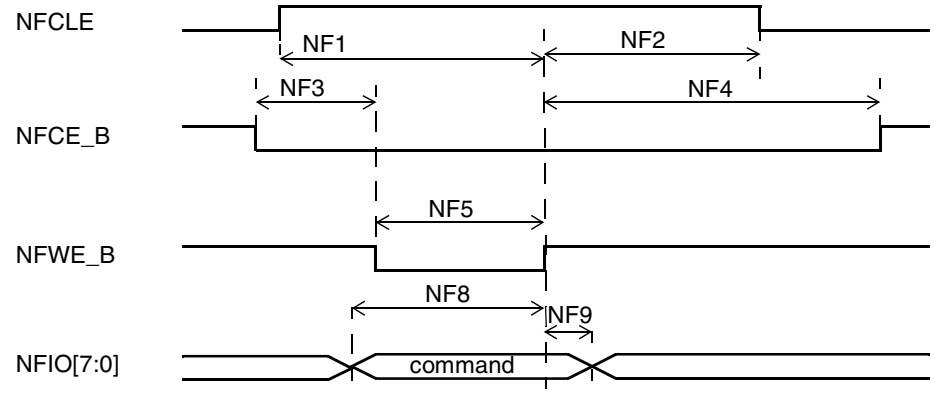


Figure 14. Command Latch Cycle Timing

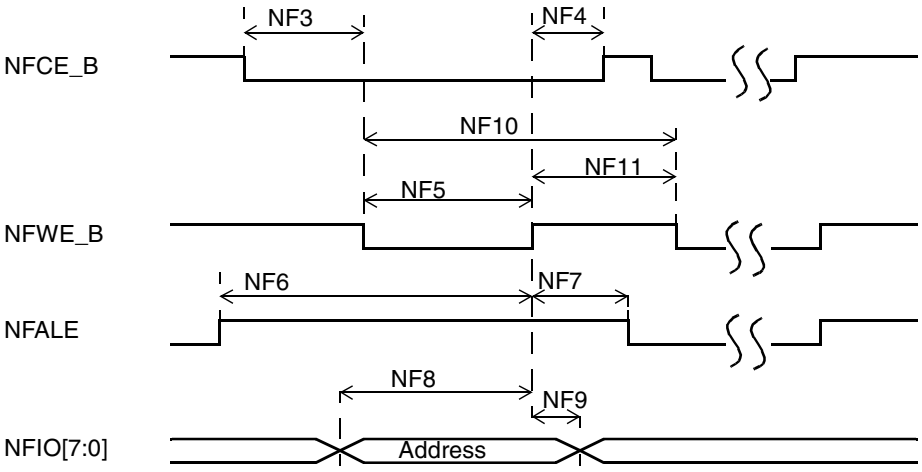


Figure 15. Address Latch Cycle Timing

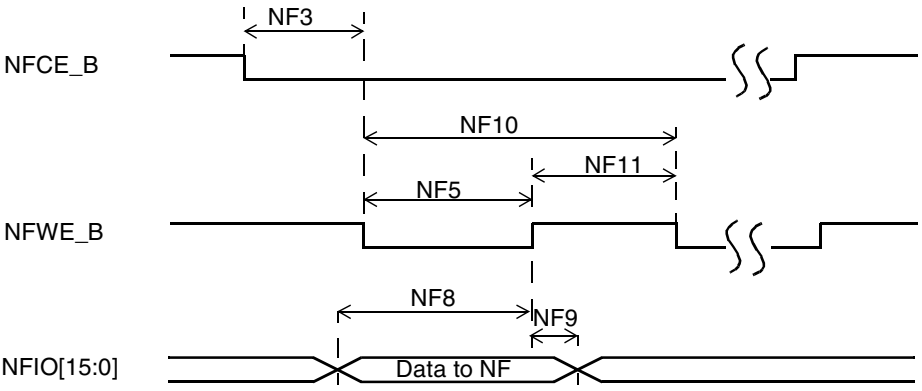


Figure 16. Write Data Latch Timing

Figure 33 shows the timing diagram for mDDR SDRAM write cycle. The timing parameters for this diagram is shown in Table 56.

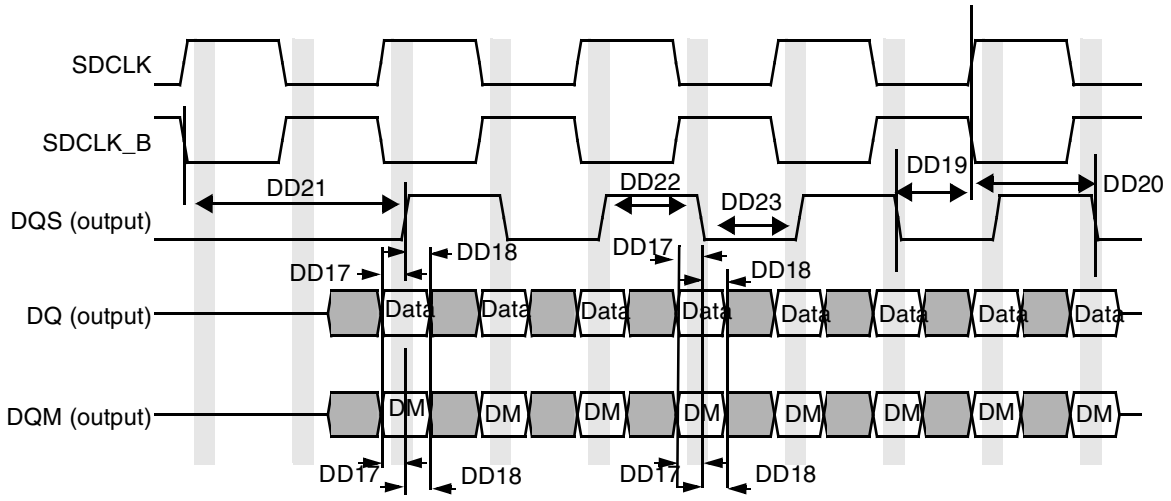


Figure 33. mDDR SDRAM Write cycle Timing Diagram

Table 56. mDDR SDRAM Write Cycle Parameter Table[1]

ID	Parameter	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD17	DQ and DQM setup time to DQS	t_{DS}[3]	0.48	—	0.6	—	0.8	—	ns
DD18	DQ and DQM hold time to DQS	t_{DH}[1]	0.48	—	0.6	—	0.8	—	ns
DD19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.2	—	0.2	—	0.2	—	tCK
DD20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.2	—	0.2	—	0.2	—	tCK
DD21	Write command to first DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DD22	DQS high level width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DD23	DQS low level width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	tCK

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

3 This parameter is affected by pad timing. If the slew rate is < 1 V/ns, 0.1 ns should be increased to this value.

1 Test conditions are: Capacitance 15 pF for DDR contacts. Recommended drive strengths: Medium for SDCLK and High for address and controls.

2 SDCLK and DQS related parameters are measured from the 50% point. For example, a high is defined as 50% of the signal value and a low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK_B.

Figure 36 shows the timing diagram for DDR2 SDRM write cycle. The timing parameters for this diagram appear in Table 60.

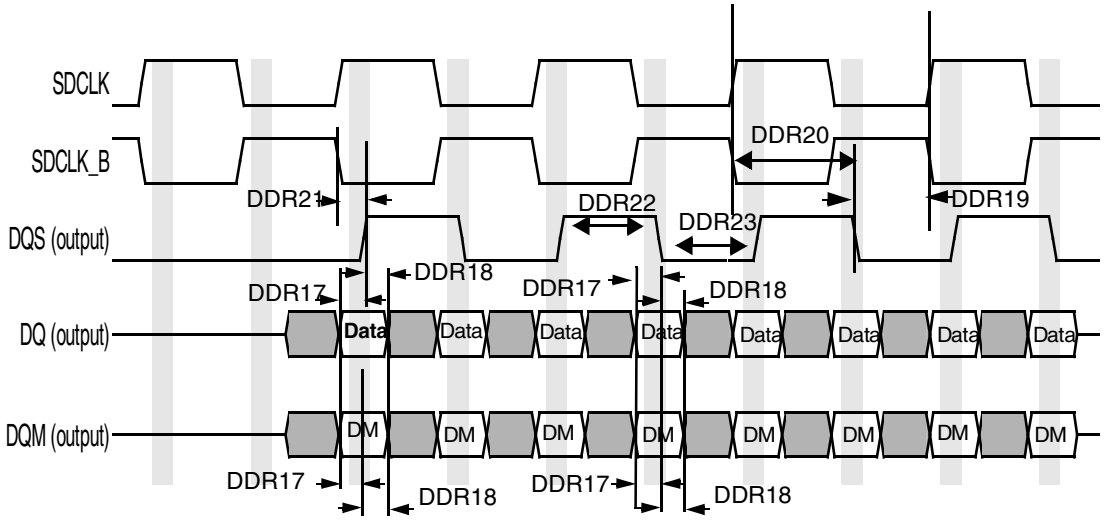


Figure 36. DDR2 SDRAM Write Cycle Timing Diagram

Table 60. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR17	DQ & DQM setup time to DQS	t_{DS}	0.8[1]	—	ns
DDR18	DQ & DQM hold time to DQS	t_{DH}	0.8[2]	—	ns
DDR19	DQS falling edge to SDCLK output setup time	t_{DSS}	1.6	—	ns
DDR20	DQS falling edge SDCLK output hold time	t_{DSH}	2.4	—	ns
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.7	0.3	ns
DDR22	DQS high level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low level width	t_{DQSL}	0.35	—	tCK

1 - In order to meet these setup/hold values, write calibration should be performed to place the DQS in the middle of DQ window. The minimum window width is 1.6ns (DDR17+DDR18).
- From DDR controller perspective, the timing is the same for both differential and single ended mode.

2 - In order to meet these setup/hold values, write calibration should be performed to place the DQS in the middle of DQ window. The minimum window width is 1.6ns (DDR17+DDR18).
- From DDR controller perspective, the timing is the same for both differential and single ended mode.

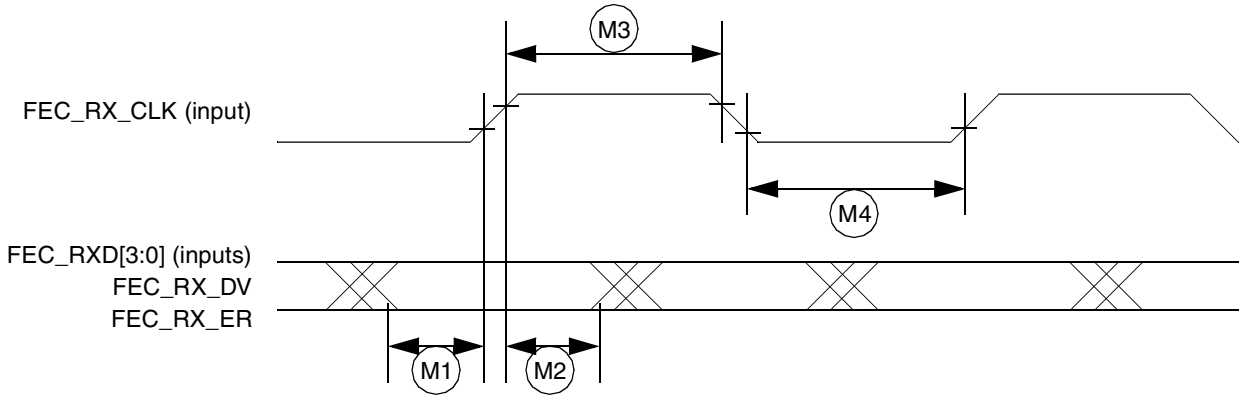


Figure 43. MII Receive Signal Timing Diagram

4.7.4.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 71 lists MII transmit channel timing parameters and Figure 44 shows MII transmit signal timing diagram for the values listed in Table 71.

Table 71. MII Transmit Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

1 FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

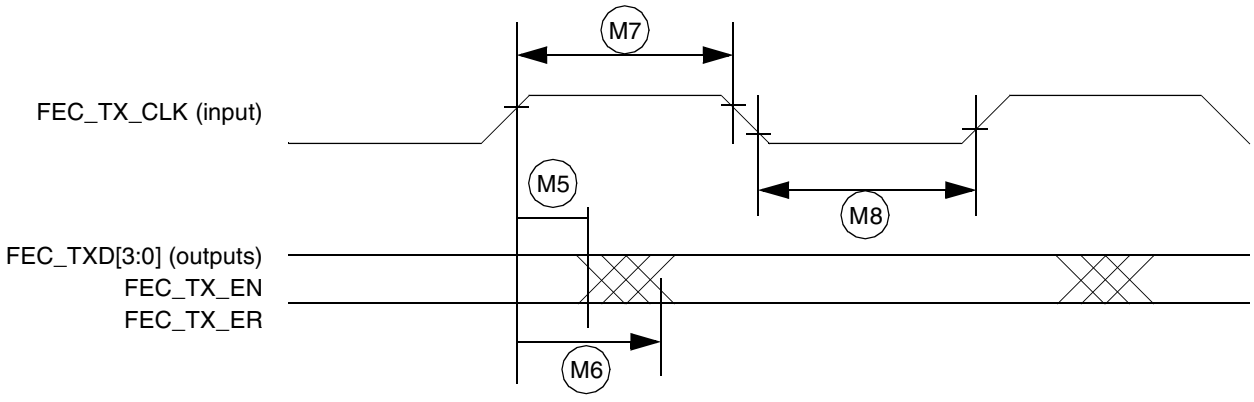


Figure 44. MII Transmit Signal Timing Diagram

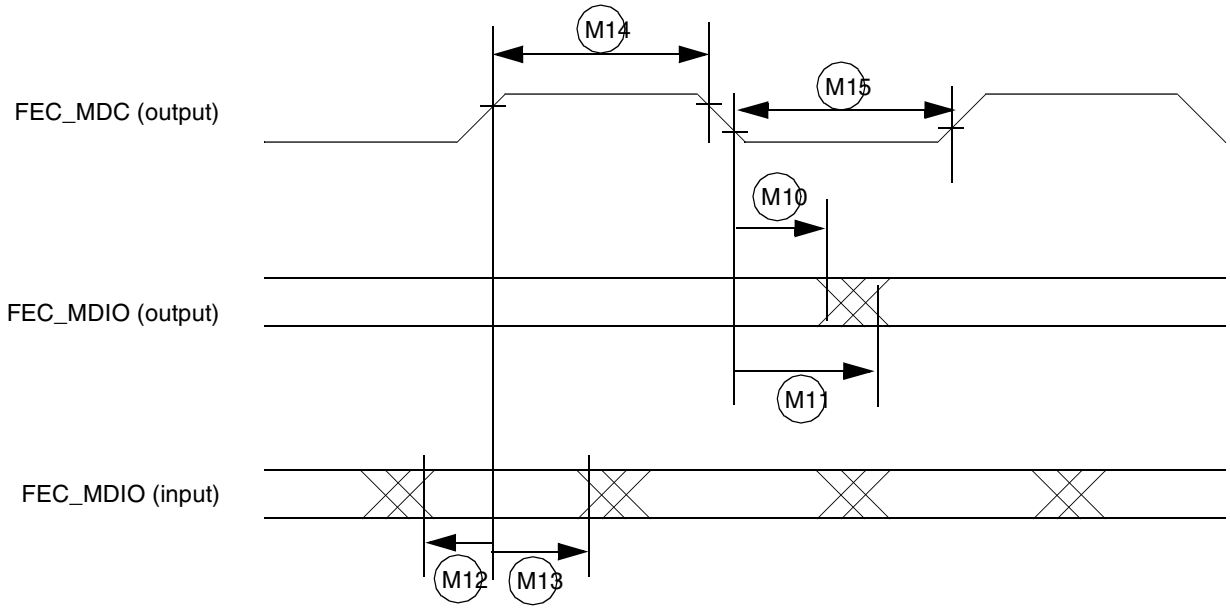


Figure 46. MII Serial Management Channel Timing Diagram

4.7.5 Frequency Pre-Multiplier (FPM) Electrical Parameters (CKIL)

The FPM is a DPLL that converts a signal operating in the kilohertz region into a clock signal operating in the megahertz region. The output of the FPM provides the reference frequency for the on-chip DPLLs. Parameters of the FPM are listed in Table 74.

Table 74. FPM Specifications

Parameter	Min	Typ	Max	Unit
Reference clock frequency range—CKIL	32	32.768	256	kHz
FPM output clock frequency range	8	—	33	MHz
FPM multiplication factor (test condition is changed by a factor of 2)	128	—	1024	—
Lock-in time[1]	—	—	312.5	µs
Cycle-to-cycle frequency jitter (peak to peak)	—	8	20	ns

[1] pIrf = 1 cycle assumed missed + x cycles for reset deassert + y cycles for calibration and lock x[ts] = {2,3,5,9}; y[ts] = {7,8,10,14}; where ts is the chosen time scale of the reference clock. In this case reference clock = 32 kHz which makes ts = 0, therefore total time required for achieving lock is 10(1+2+7) cycles or 312.5 µs.

4.7.6 High-Speed I^{2}C (HS-I^{2}C) Timing Parameters

This section describes the timing parameters of the HS-I^{2}C module. This module can operate in the following modes: Standard, Fast and High speed.

NOTE

See the errata for the HS-I^{2}C module in the i.MX51 Chip Errata. There are two standard I^{2}C modules that have no errata.

4.7.8.6.1 TV Encoder Performance Specifications

All the parameters in the table are defined under the following conditions:

Rset = 1.05 kΩ ±1%, resistor on VREFOUT pin to Ground

Rload = 37.5 Ω ±1%, output load to Ground

The TV encoder output specifications are shown in Table 82.

Table 82. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL)[2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	Rset = 1.05 kΩ ±1% Rload = 37.5 Ω±1%	1.24	1.35	1.45	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 9.28 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2, 3]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0-4.0 MHz	–0.1	—	0.1	dB
	5.75 MHz	–0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	–70	—	dB
Chroma PM Noise	—	—	–47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%

4.7.8.7.2 Asynchronous Parallel Interface Timing Parameters

Figure 63 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 84 shows the timing characteristics at display access level. Table 83 shows the timing characteristics at the logical level—from configuration perspective. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

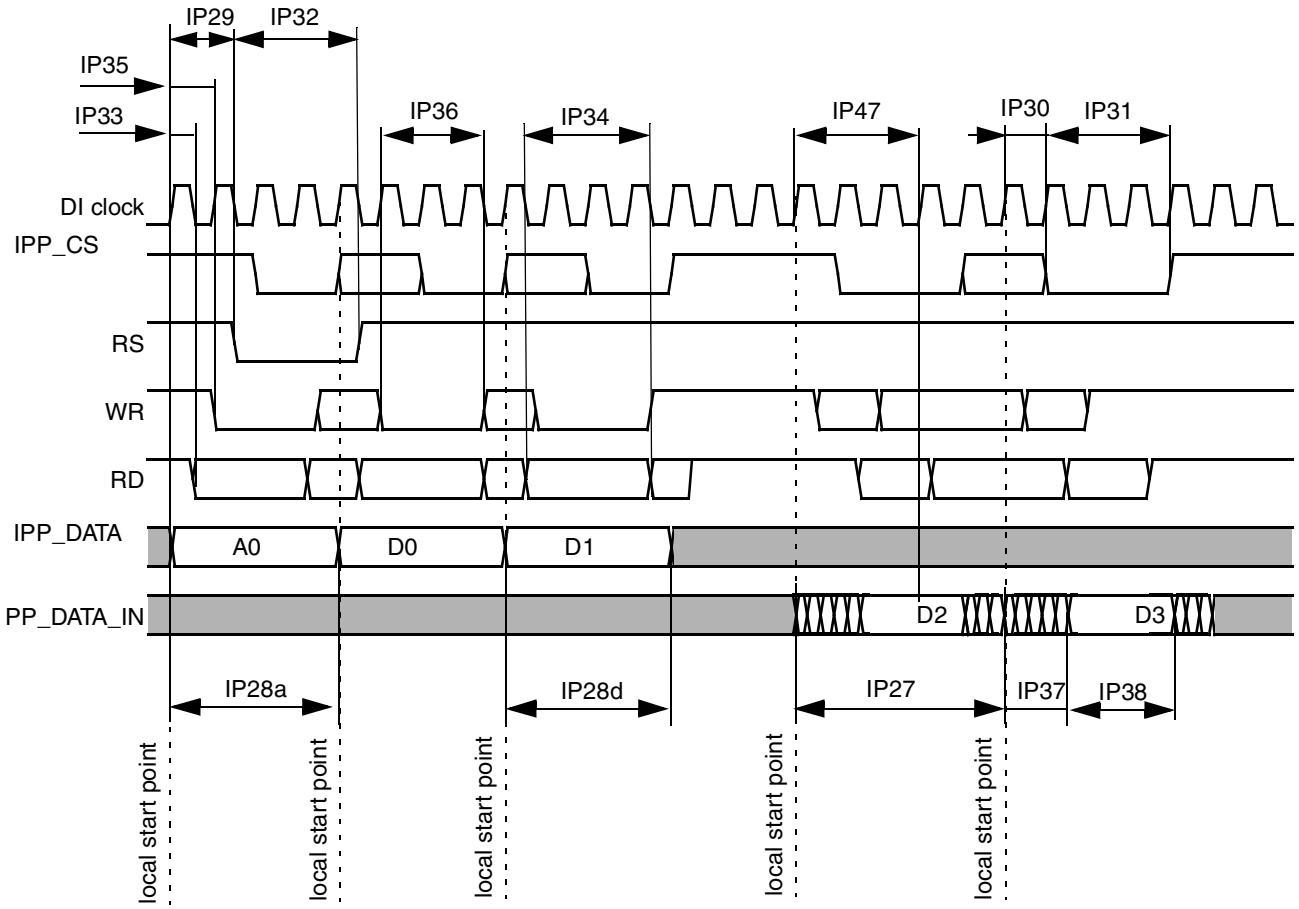


Figure 63. Asynchronous Parallel Interface Timing Diagram

Table 83. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP27	Read system cycle time	Tcycr	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns

Table 90 and Figure 73 define the AC characteristics of all the P-ATA interface signals on all data transfer modes.

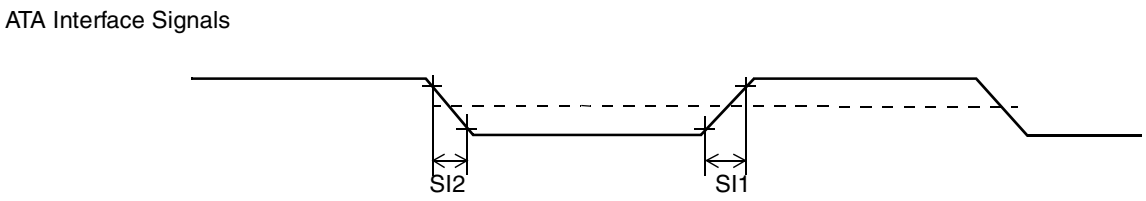


Figure 73. P-ATA Interface Signals Timing Diagram

Table 90. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface.[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface (see note)	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user needs to use level shifters for 5.0 V compatibility on the ATA interface. The i.MX51 P-ATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-4) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX51 P-ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

Table 101. AUDMUX Port Allocation (continued)

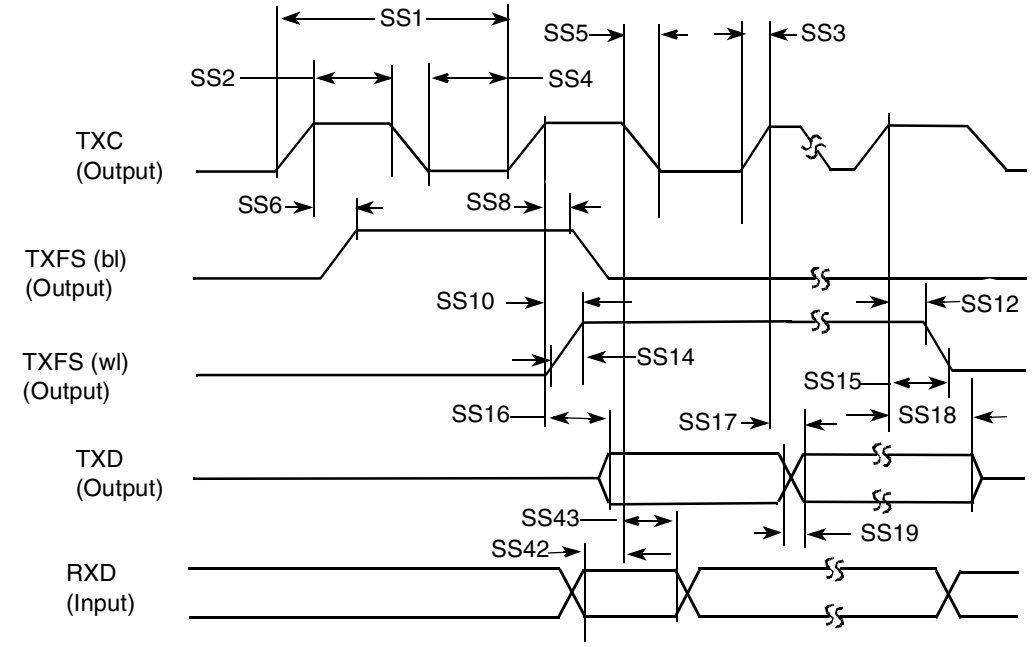
Port	Signal Nomenclature	Type and Access
AUDMUX port 6	AUD6	External—EIM or DISP2 via IOMUX
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.15.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter internal clock timing and Table 102 lists the timing parameters for the SSI transmitter internal clock.

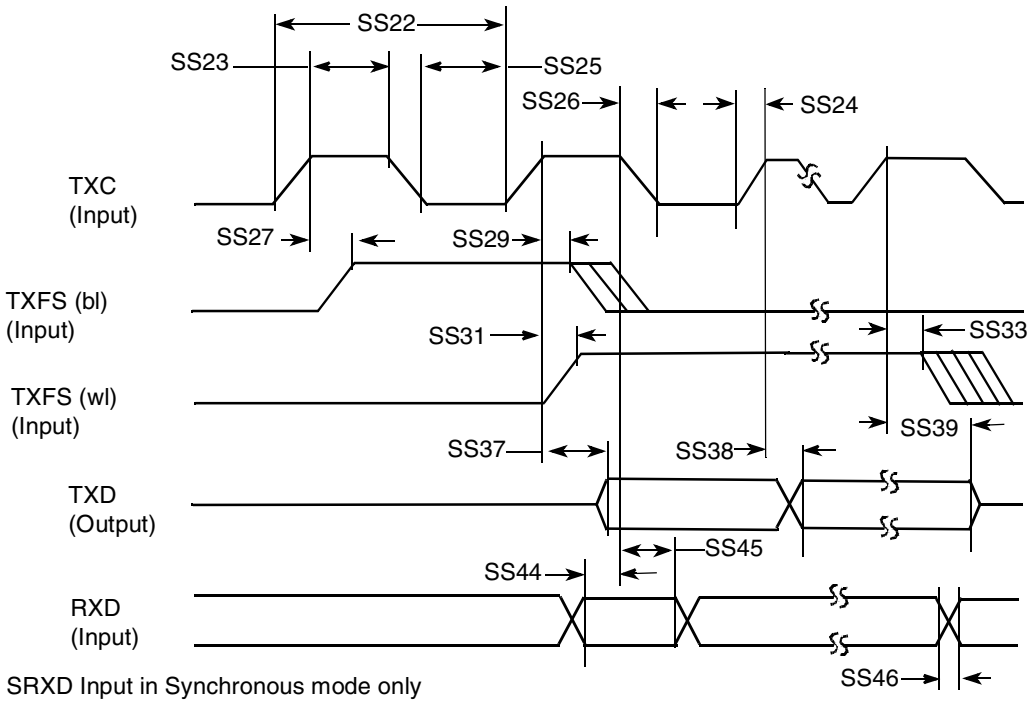


Note: SRXD input in synchronous mode only

Figure 92. SSI Transmitter Internal Clock Timing Diagram

4.7.15.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter external clock timing and Table 104 lists the timing parameters for the SSI transmitter external clock.



Note: SRXD Input in Synchronous mode only

Figure 94. SSI Transmitter External Clock Timing Diagram

Table 104. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	30	ns

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_IPU7	H22
NVCC_IPU8	V22
NVCC_IPU9	L16
NVCC_NANDF_A	J8
NVCC_NANDF_B	H8
NVCC_NANDF_C	H9
NVCC_OSC	AD22
NVCC_PER10	H12
NVCC_PER11	H11
NVCC_PER12	H15
NVCC_PER13	H14
NVCC_PER14	V9
NVCC_PER15	H16
NVCC_PER17	J16
NVCC_PER3	V10
NVCC_PER5	D20
NVCC_PER8	J15
NVCC_PER9	H10
NVCC_SRTC_POW	V12
NVCC_TV_BACK	AC22
NVCC_USBPHY	P16
RREFEXT	K18
SGND	P10
SVCC	N13
SVDDGP	M11
TVDAC_DHVDD	AB21
VBUS	L22
VCC	N12, N14, N15, P12, P13, P14, P15, R13, R14, R15, T14, T15, T16, U14, U15, U16
VDD_ANA_PLL_A	AD4
VDD_ANA_PLL_B	AC24
VDD_DIG_PLL_A	AD3
VDD_DIG_PLL_B	AB23
VDD_FUSE	P6

Table 129. 13 x 13 mm No Connect Assignments (continued)

Ball Status	Ball Assignments
NC	AA20
NC	AA21

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_D0_CS	U21	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	AB23	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J18	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	Y22	NVCC_IPU2	GPIO	Output	High
DI1_PIN12	AA22	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	T20	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	H20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	G23	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	G22	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J21	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	J20	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	K18	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	H23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	N20	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	N21	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[3]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[3]	E21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[3]	F20	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[3]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[3]	G19	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[3]	E23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[3]	F21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[3]	G20	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[3]	H18	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	U22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[3]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[3]	H19	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[3]	F22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[3]	G21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	U23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	T22	NVCC_HS6	HSGPIO	Input	Keeper

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper

6 Revision History

Table 135 provides a revision history for this data sheet.

Table 135. i.MX51 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	10/2012	• In Table 25, "I/O Leakage Current," on page 31, updated supply rail names for SD1 and SD2 to NVCC_PER15 and NVCC_PER17, respectively. • Updated Section 4.6.7.3, “General WEIM Timing-Synchronous Mode.” • Updated Section 4.6.7.4, “Examples of WEIM Synchronous Accesses.” • Updated Section 4.6.7.5, “General WEIM Timing-Asynchronous Mode.”
Rev. 5	03/2012	• In Table 4, "JTAG Controller Interface Summary," on page 14, changed On-Chip Termination column value for JTAG_MOD from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Section 3.7, “USB-OTG IOMUX Pin Configuration,” removed the third sentence from the first paragraph and added a note after Table 9. • In Section 4.3.4, “Ultra-High Voltage I/O (UHVIO) DC Parameters,” added clarification about UHVIO I/O cell HVE bit functionality after Table 21. • In Section 4.6.9, “DDR2 SDRAM Specific Parameters:” —Updated Table 58, "DDR2 SDRAM Timing Parameter Table," on page 69 —Added a note after Table 58 —Updated Figure 36, "DDR2 SDRAM Write Cycle Timing Diagram," on page 71 —Updated Table 60, "DDR2 SDRAM Write Cycle Parameter Table," on page 71 —Added a note after Table 60 —Updated Figure 37, "DDR2 SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram," on page 73 —Updated Table 63, "DDR2 SDRAM Read Cycle Parameter Table," on page 73 —Added a note after Table 63 • In Section 4.7.8.2, “Electrical Characteristics,” changed signal name in the second sentence of the first paragraph from “SENSB_MCLK” to “SENSB_PIX_CLK.” • In Table 128, "13 x 13 mm Signal Assignments, Power Rails, and I/O," on page 157, changed Configuraton after Reset column value for contacts, DI1_D0_CS, DI1_D1_CS, DI1_PIN11, and DI1_PIN12, from “Low” to “High.” • In Table 128, "13 x 13 mm Signal Assignments, Power Rails, and I/O," on page 157, changed Configuraton after Reset column value for contact, JTAG_MOD, from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Table 128, "13 x 13 mm Signal Assignments, Power Rails, and I/O," on page 157, changed Power Rail column value for contacts, UART1_CTS, UART1_RTS, UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD, UART3_RXD, and UART3_TXD, from “NVVCC_PER12” to “NVCC_PER12.” • In Table 131, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 177, changed Configuraton after Reset column value for contacts, DI1_D0_CS, DI1_D1_CS, DI1_PIN11, and DI1_PIN12, from “Low” to “High.” • In Table 131, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 177, changed Configuraton after Reset column value for contact, JTAG_MOD, from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Table 131, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 177, changed Power Rail column value for contacts, UART1_CTS, UART1_RTS, UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD, UART3_RXD, and UART3_TXD, from “NVVCC_PER12” to “NVCC_PER12.” • In Table 132, "Fuse Override Contacts," on page 189: —Added a footnote for contact, DISP1_DAT6 —Removed information about contact, EIM_A23, because the signal configuration it corresponds to, BT_HPN_EN, is not in use. • Corrected cross-references throughout the document.

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	05/2010	• Updated CaseTemperature Range column in Table 1, "Ordering Information," on page 3. • Changed the VREFOUT column in Table 3, "Special Signal Considerations," on page 12. • Added Section 3, “IOMUX Configuration for Boot Media”. • Updated Figure 2, "Power-Up Sequence," on page 24. • Updated the Minimum and Maximum columns in Table 13, "i.MX51 Operating Ranges," on page 19. • Added a note in Section 4.2.1, “Power-Up Sequence”. • Updated Section 4.2.1, “Power-Up Sequence.” • Changed the Input current (47 kΩ Pull-up) column in Table 21, "UHVIO DC Electrical Characteristics," on page 27 to Input current (75 kO Pull-up). • Added new table for parameters for DDR2 Pad output buffer Impedance. See Table 27, "DDR2 I/O Output Buffer Impedance HVE = 0," on page 32. • Added new section under Section 4.5, “I/O AC Parameters”. See Section 4.5.4, “AC Electrical Characteristics for DDR2”. • Updated Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. In the VIH (for square wave input) parameter, the minimum frequency was changed to NVCC_PER3 - 0.25V and the maximum frequency was changed to NVCC_PER3. • Added a note in Section 4.6.6, “NAND Flash Controller (NFC) Parameters” after Table 49. • Updated Asymmetric Mode Min, Symmetric Mode Min, and Max columns of Table 50. • Removed Conditions parameters of the Full scale output voltage row in Table 82. • Updated Section 4.7.11, “P-ATA Timing Parameters”. Replaced ATA/ATAPI-6 specification with ATA/ATAPI-5 specification. • In Table 102, "SSI Transmitter Timing with Internal Clock," on page 135, under the Synchronous Internal Clock Operation sections for the ID SS42, minimum frequency was changed from 10.0 to 30. • In Table 103, "SSI Receiver Timing with Internal Clock," on page 136, under the Internal Clock Operation section for ID SS20, minimum frequency was changed from 10.0 to 30. • In Table 104, "SSI Transmitter Timing with External Clock," on page 138, under the External Clock Operation section for ID SS38, maximum frequency was changed from 15.0 to 30. • Added a new section Section 4.7.16.1, “UART Electrical”, under Section 4.7.16, “UART”. • In Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148, for IDs SS28 and SS29, direction was changed from out to in. • In Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150, for IDs US40 and US41, direction was changed from out to in and the reference signal was changed to USB_VM1 and USB_VP1 respectively. • In Table 122, "USB Timing Specification for ULPI Parallel Mode," on page 151, added an extra row for ID17. • Updated Signal and Direction columns in Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150. • Updated Signal names in Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148.
Rev. 1	10/2009	Initial public release.