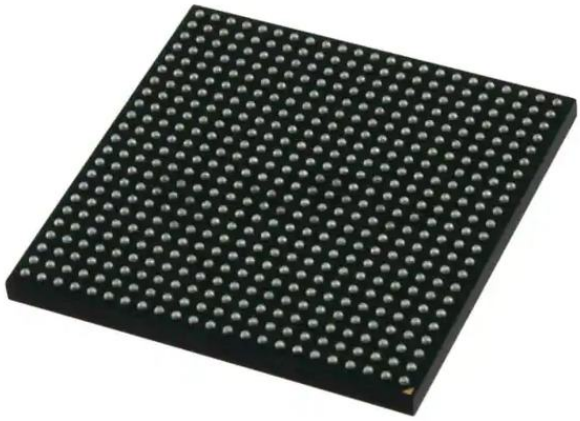

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 95°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx512cjm6cr2

1.2 Block Diagram

Figure 1 shows the functional modules of the processor.

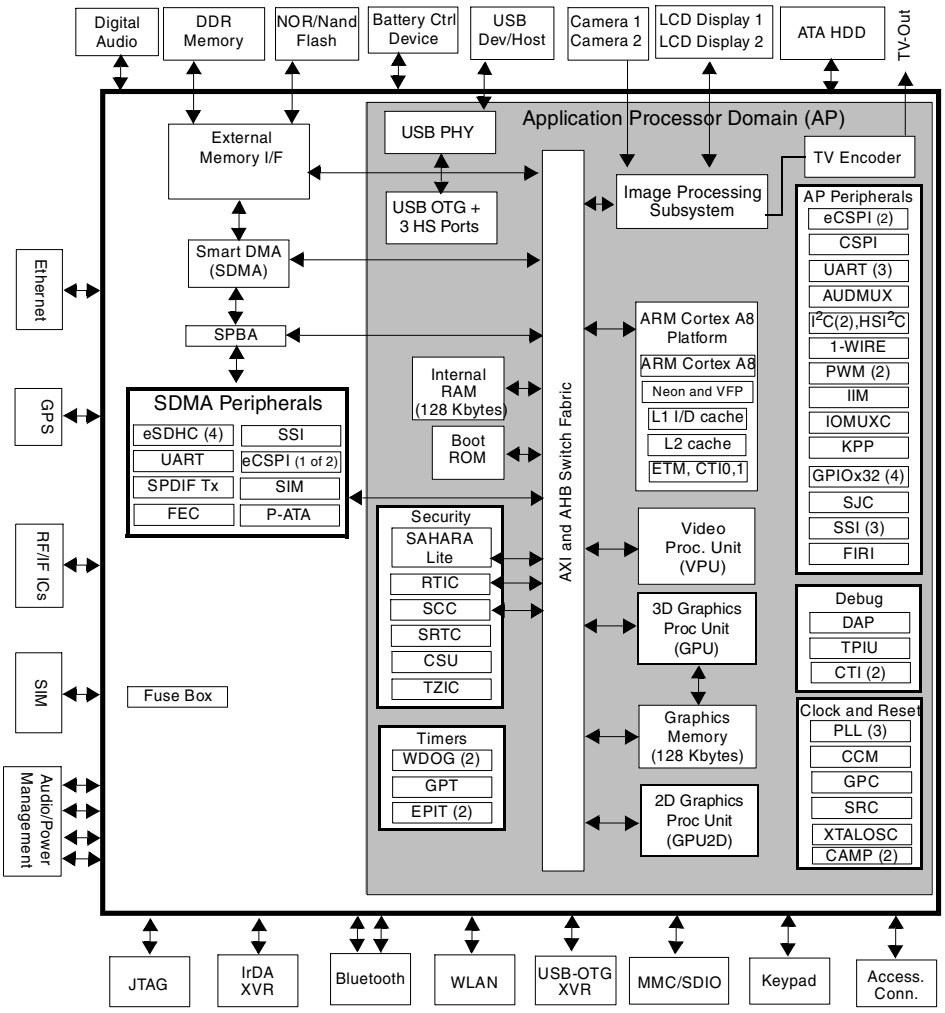

Figure 1. Functional Block Diagram

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	IPU enables connectivity to displays and image sensors, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces. • Legacy Interfaces • Analog TV interfaces (through a TV encoder bridge) The processing includes: • Support for camera control • Image enhancement: color adjustment and gamut mapping, gamma correction and contrast enhancement, sharpening and noise reduction • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Synchronization and control capabilities, allowing autonomous operation. • Hardware de-interlacing support
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
P-ATA (Muxed with eSDHC-4	Parallel ATA	Connectivity Peripherals	The P-ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA-5 (UDMA-4) compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. This is muxed with eSDHC-4 interfaces.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	Unified RAM, can be split between Secure RAM and Non-Secure RAM
ROM 36 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTIC	Real Time Integrity Checker	Security	Protecting read-only data from modification is one of the basic elements in trusted platforms. The Run-Time Integrity Checker v3 (RTICv3) module, is a data monitoring device responsible for ensuring that memory content is not corrupted during program execution. The RTICv3 mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The RTICv3's purpose is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement, and assist with boot authentication.
SAHARA Lite	SAHARA security accelerator Lite	Security	SAHARA (Symmetric/Asymmetric Hashing and Random Accelerator) is a security co-processor. It implements symmetric encryption algorithms, (AES, DES, 3DES, and RC4), public key algorithms, hashing algorithms (MD5, SHA-1, SHA-224, and SHA-256), and a hardware random number generator. It has a slave IP bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SCC	Security Controller	Security	The Security Controller is a security assurance hardware module designed to safely hold sensitive data such as encryption keys, digital right management (DRM) keys, passwords, and biometrics reference data. The SCC monitors the system's alert signal to determine if the data paths to and from it are secure—that is, cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCC also features a Key Encryption Module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex™-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API are available
SIM	Subscriber Identity Module Interface	Connectivity Peripherals	The SIM is an asynchronous interface with additional features for allowing communication with Smart Cards conforming to the ISO 7816 specification. The SIM is designed to facilitate communication to SIM cards or pre-paid phone cards.

2.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX51. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." Signal descriptions are defined in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CKIH1, CKIH2	Inputs feeding CAMPs (Clock Amplifiers) that have on-chip ac coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH1 or CKIH2 (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules driven by CKIH1 or CKIH2. See CCM chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details on the respective clock trees. After initialization, the CAMPs could be disabled (if not used) by CCM registers (CCR CAMPx_EN field). If disabled, the on-chip CAMP output is low; the input is irrelevant. If unused, the user should tie CKIH1/CKIH2 to GND for best practice.
CLK_SS	Clock Source Select is the input that selects the default reference clock source providing input to the DPLLs. To use a reference in the megahertz range per Table 8, tie CLK_SS to GND to select EXTAL/XTAL. To use a reference in the kilohertz range per Table 59, tie CLK_SS to NVCC_PER3 to select CKIL. After initialization, the reference clock source can be changed (initial setting is overwritten). **Note:** Because this input has a keeper circuit, Freescale recommends tying this input to directly to GND or NVCC_PER3. If a series resistor is used its value must be $\leq$ 4.7 kΩ.
COMP	The user should bypass this reference with an external 0.1 µF capacitor tied to GND. If TV OUT is not used, float the COMP contact and ensure the DACs are powered down. **Note:** Previous engineering samples required this reference to be bypassed to a positive supply.
FASTR_ANA and FASTR_DIG	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. Users should float this output.
GPIO_NAND	This is a general-purpose input/output (GPIO3_12) on the NVCC_NANDF_A power rail.
IOB, IOG, IOR, IOB_BACK, IOG_BACK, and IOR_BACK	These signals are analog TV outputs that should be tied to GND when not being used.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed.
NC	These signals are No Connect (NC) and should be floated by the user.

Table 34. I^2C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	10/74	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	7/14	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	17	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	30	—	67	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	15	—	34	ns

Table 35. Low Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Medium drive)	tdit	—	—	—	22	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	11	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time greater than 25 ns

Table 36. High Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	3/3 6/5	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	5/5 9/9	ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time > 25 ns

4.6.2 WDOG Reset Timing Parameters

Figure 13 shows the WDOG reset timing and Table 46 lists the timing parameters.

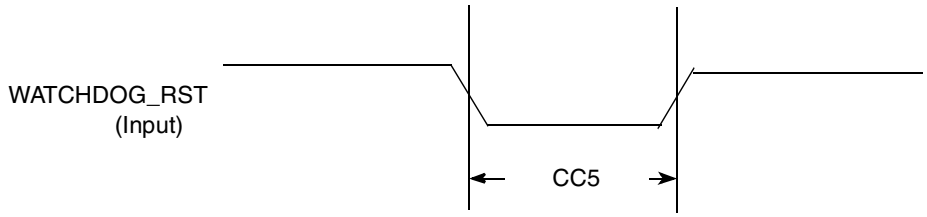

Figure 13. WATCHDOG_RST Timing Diagram

Table 46. WATCHDOG_RST Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WATCHDOG_RESET Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.6.4 Clock Amplifier Parameters (CKIH1, CKIH2)

The input to Clock Amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required. Table 47 shows the CAMP electrical parameters.

Table 47. CAMP Electrical Parameters (CKIH1, CKIH2)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	NVCC_PER3 - 0.25	—	NVCC_PER3	V
Sinusoidal input amplitude	0.4	—	VDD	Vp-p
Output duty cycle	45	50	55	%

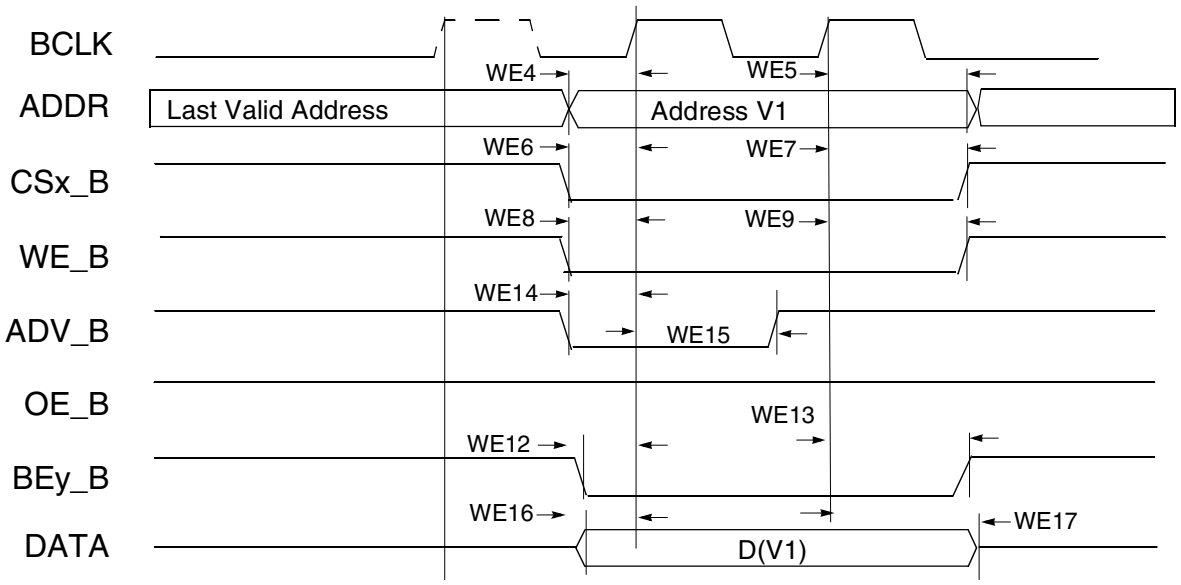

Figure 23. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

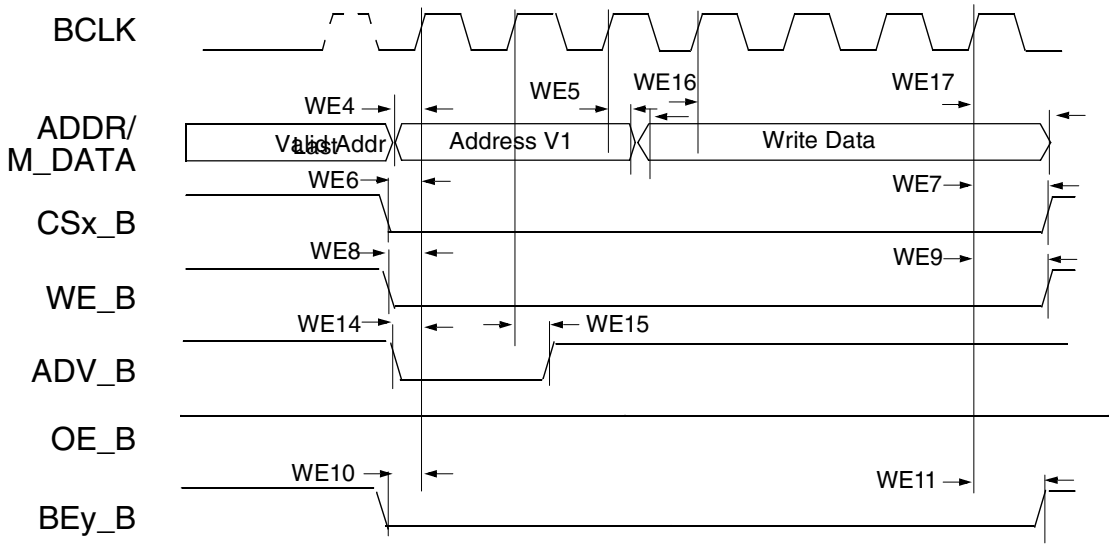

Figure 24. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

Figure 37 shows the timing diagram for DDR2 SDRM read cycle. The timing parameters for this diagram appear in Table 63.

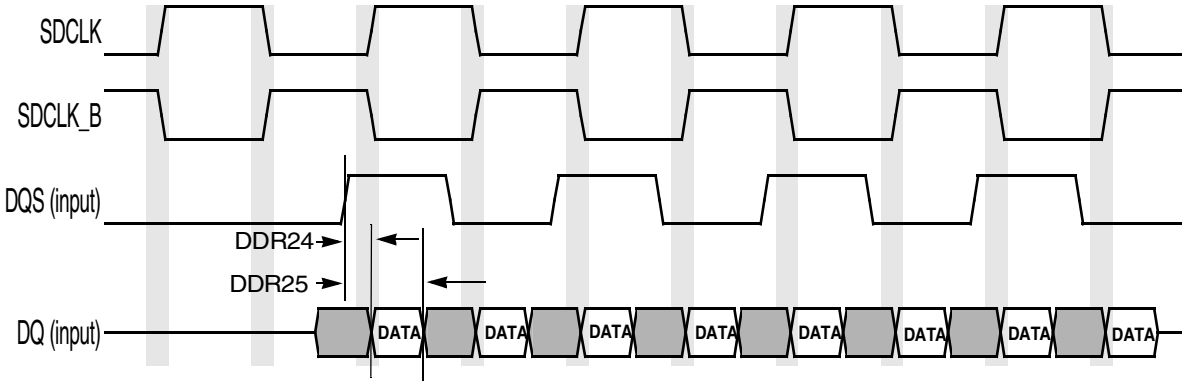

Figure 37. DDR2 SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 63. DDR2 SDRAM Read Cycle Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR24[1]	DQS—DQ Skew (defines the Data valid window during read cycles related to DQS).	t_{DQSQ}	—	0.5	ns
DDR25[2]	DQ HOLD time from DQS	t_{QH}	1.8	—	ns

1 The actual timing may vary depending on read calibration settings. What is actually important for the controller is DDR25-DDR24 which results in the minimum required DQ valid window width: 1.8ns-0.5ns = 1.3ns of minimum width.

2 The actual timing may vary depending on read calibration settings. What is actually important for the controller is DDR25-DDR24 which results in the minimum required DQ valid window width: 1.8ns-0.5ns = 1.3ns of minimum width.

NOTE

It is recommended to perform read calibration process in order to achieve the best performance.

Table 79. Video Signal Cross-Reference (continued)

i.MX51	LCD								Comment[1]
Port Name (x=1,2)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24-bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—	—
DIx_DISP_CLK	PixCLK							—	—
DIx_PIN1	—							VSYNC_IN	May be required for anti-tearing
DIx_PIN2	HSYNC							—	—
DIx_PIN3	VSYNC							—	VSYNC out
DIx_PIN4	—							—	Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							—	
DIx_PIN6	—							—	
DIx_PIN7	—							—	
DIx_PIN8	—							—	
DIx_D0_CS	—							CS0	—
DIx_D1_CS	—							CS1	Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							WR	—
DIx_PIN12	—							RD	—
DIx_PIN13	—							RS1	Register select signal
DIx_PIN14	—							RS2	Optional RS2
DIx_PIN15	DRDY/DV							DRDY	Data validation/blank, data enable
DIx_PIN16	—							—	Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							—	

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

[3] Display interface clock up time

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.7.8.6 Interface to a TV Encoder

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The timing of the interface is described in Figure 57.

NOTE

- The frequency of the clock DISP_CLK is 27 MHz (within 10%)
- The HSYNC, VSYNC signals are active low.
- The DRDY signal is shown as active high.
- The transition to the next row is marked by the negative edge of the HSYNC signal. It remains low for a single clock cycle
- The transition to the next field/frame is marked by the negative edge of the VSYNC signal. It remains low for at least one clock cycles

  — At a transition to an odd field (of the next frame), the negative edges of VSYNC and HSYNC coincide.

  — At a transition is to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the HSYNC signal being high.

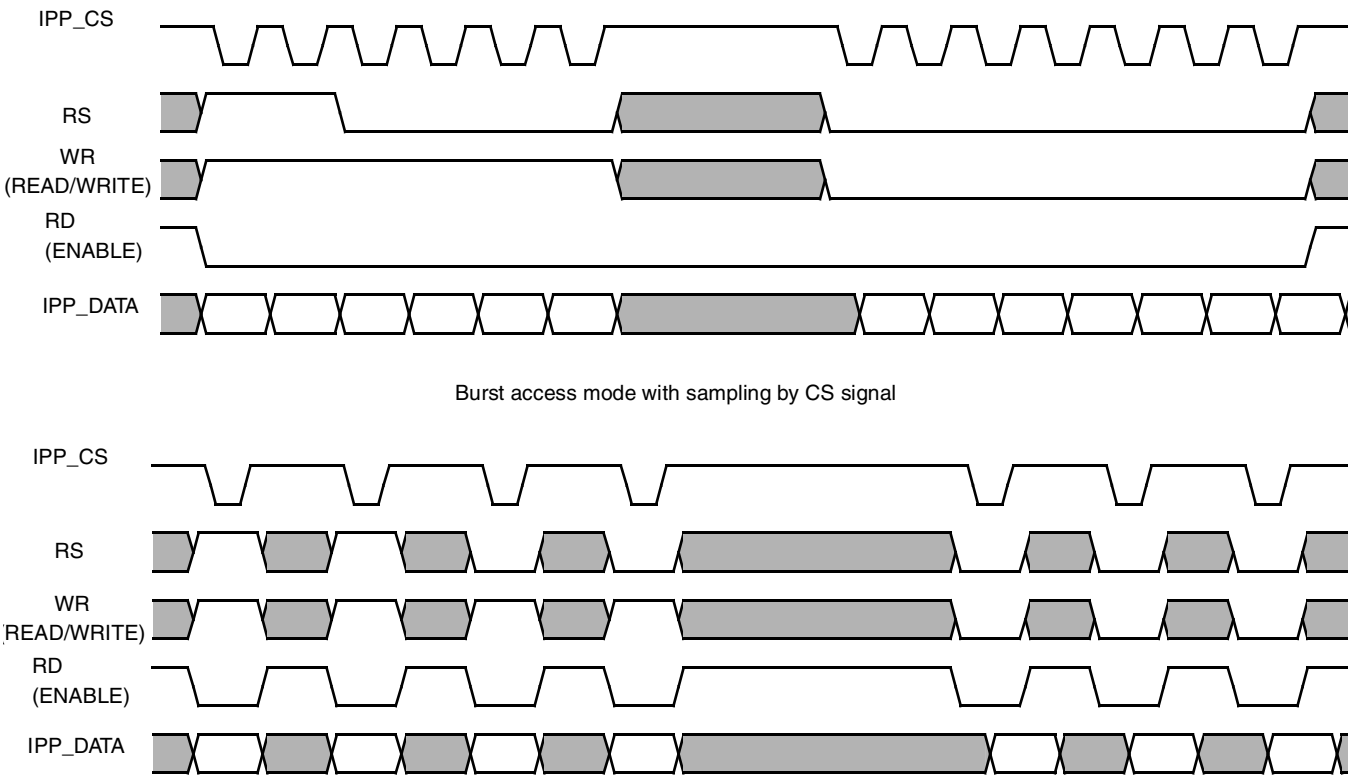

Figure 60. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

Table 90 and Figure 73 define the AC characteristics of all the P-ATA interface signals on all data transfer modes.

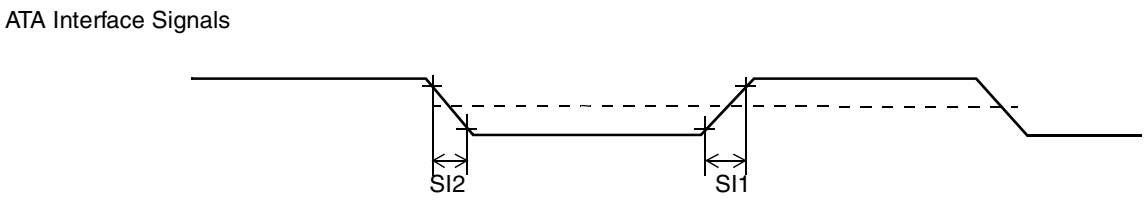

Figure 73. P-ATA Interface Signals Timing Diagram

Table 90. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface.[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface (see note)	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user needs to use level shifters for 5.0 V compatibility on the ATA interface. The i.MX51 P-ATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-4) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX51 P-ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 109 lists the transmit timing characteristics.

Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 109. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1]$-T_{ref\_clk}$[2]	$1/F_{baud\_rate}+T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)\times(1F_{baud\_rate})-T_{ref\_clk}$	$(3/16)\times(1F_{baud\_rate})+T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.
[2] Tref_clk: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART IrDA Mode Receiver

Figure 99 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 110 lists the receive timing characteristics.

Figure 99. UART IrDA Mode Receive Timing Diagram

Table 110. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2]$-$ $1/(16\times F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16\times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 us	$(5/16)\times(1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16\times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16\times F_{baud\_rate})$.

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_A4	U1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A5	U2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A6	T1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A7	T2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A8	T3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A9	P1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CAS	N4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS0	P3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS1	R3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D0	AC4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D1	AC3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D10	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D11	AA1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D12	AB2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D13	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D14	AC2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D15	AC1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D16	F2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D17	F3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D18	G3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D19	F4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D2	AB3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D20	H3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D21	G4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D22	J3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D23	H4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D24	J4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D25	J1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D26	J2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D27	H1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D28	H2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D29	G1	NVCC_EMI_DRAM	DDR2	Output	High

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_D3	AB4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D30	G2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D31	F1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D4	AA3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D5	AA4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D6	Y3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D7	Y4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D8	Y1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D9	Y2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM0	V1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM1	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM2	M4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM3	N2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_RAS	N3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE0	N1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE1	L1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCLK	M1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDCLK_B	M2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0	W3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0_B	W4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1	W2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1_B	W1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2	K3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2_B	K4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3	K2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3_B	K1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDWE	M3	NVCC_EMI_DRAM	DDR2	Output	High
EIM_A16[1]	Y12	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A17[1]	AE6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[1]	Y13	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[1]	AE7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[1]	Y6	NVCC_EMI	GPIO	Input	100 kΩ pull-up

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	H6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	D6	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	F6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	G6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	E3	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	A15	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AC18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	AE18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AC19	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	AB18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	Y24	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	AA25	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A18	NVCC_PER15	UHVIO	Output	—
SD1_CMD	C17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	B18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	D17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	D18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	C18	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	A19	NVCC_PER17	UHVIO	Output	—
SD2_CMD	F16	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	F18	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	A21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	F17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down
STR	D14	NVCC_PER12	—	—	—

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
TEST_MODE	AB25	NVCC_PER3	GPIO	Input	100 kΩ pull-down
UART1_CTS	B13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RTS	C13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RXD	D13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_TXD	A12	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_RXD	A13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_TXD	C14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART3_RXD	B14	NVCC_PER12	GPIO	Input	Keeper
UART3_TXD	A14	NVCC_PER12	GPIO	Input	Keeper
USBH1_CLK	C11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA0	B11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA1	A10	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA2	A9	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA3	C10	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA4	B9	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA5	F14	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA6	C12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA7	B12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DIR	B10	NVCC_PER11	GPIO	Input	Keeper
USBH1_NXT	D12	NVCC_PER11	GPIO	Input	Keeper
USBH1_STP	A11	NVCC_PER11	GPIO	Input	Keeper
XTAL[2]	AE23	NVCC_OSC	Analog	Output	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 See Table 3 on page 12 for more information.

3 During power-on reset this port acts as input for fuse override signal. See Table 132 on page 189 for more information.

4 During power-on reset this port acts as output for diagnostic signal. See Table 132 on page 189 for more information.

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper

Table 134. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_SDCKE0	DRAM_A7	DRAM_RAS	EIM_SDBA0	DRAM_A13	DRAM_D0	DRAM_D3	1
2	DRAM_A1	DRAM_A5	DRAM_A8	DRAM_A10	DRAM_A12	DRAM_A14	DRAM_D2	2
3	DRAM_A2	DRAM_CS1	DRAM_A6	DRAM_A9	EIM_SDBA1	DRAM_SDCLK	DRAM_D1	3
4	EIM_BCLK	DRAM_CS0	DRAM_A4	DRAM_CAS	DRAM_A11	DRAM_SDCLK_B	DRAM_D4	4
5	EIM_CS5	EIM_DTACK	DRAM_SDCKE1	DRAM_A3	DRAM_SDWE	GND	VREF	5
6	EIM_CS4	EIM_CS1	EIM_CS0	VDD_ANA_PLL_A	VDD_DIG_PLL_A	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	EIM_OE	EIM_CS2	EIM_D31	NVCC_EMI	GND_ANA_PLL_A	GND_DIG_PLL_A	VDD_FUSE	7
8	EIM_A19	EIM_D29	EIM_D27	EIM_D23	NVCC_EMI	VCC	GND	8
9	EIM_A16	EIM_D25	EIM_D21	EIM_EB3	NVCC_EMI	VCC	GND	9
10	EIM_D24	EIM_D19	EIM_D17	EIM_EB2	NVCC_EMI	VCC	GND	10
11	EIM_D18	EIM_DA15	EIM_DA13	EIM_DA11	NVCC_EMI	VCC	GND	11
12	EIM_DA12	EIM_DA9	EIM_EB1	EIM_EB0	NVCC_EMI	VCC	GND	12
13	EIM_DA6	EIM_DA5	EIM_DA7	EIM_DA1	NVCC_PER14	VDDA	GND	13
14	EIM_DA2	JTAG_TDI	JTAG_TRSTB	JTAG_MOD	NVCC_SRTC_POW	NVCC_I2C	GND	14
15	JTAG_TDO	PMIC_STBY_REQ	I2C1_CLK	JTAG_TCK	VREFOUT	NGND_TV_BACK	GND	15
16	PMIC_INT_REQ	CKIL	PMIC_ON_REQ	TVDAC_DHVDD	NVCC_TV_BACK	GND	GND	16
17	PMIC_RDY	COMP	NVCC_OSC	NGND_OSC	GND_ANA_PLL_B	VCC	VCC	17
18	AHVDDRGB	AHVDDRGB	VDD_DIG_PLL_B	GND_DIG_PLL_B	NVCC_PER3	NVCC_IPU2	NVCC_IPU9	18
19	AHVSSRGB	AHVSSRGB	VDD_ANA_PLL_B	CKIH1	DISPB2_SER_DIN	DISP2_DAT13	DISP2_DAT11	19
20	CKIH2	FASTR_DIG	FASTR_ANA	TEST_MODE	POR_B	DI1_PIN13	DISP2_DAT9	20
21	CLK_SS	RESET_IN_B	DISPB2_SER_RS	DISPB2_SER_DIO	DI1_D0_CS	DISP2_DAT15	DISP2_DAT0	21
22	DI1_PIN12	DI1_PIN11	DISP2_DAT10	DISP2_DAT4	DISP1_DAT2	DISP1_DAT4	CSI1_D10	22
23	DISP2_DAT14	DISP2_DAT12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	DISP1_DAT5	CSI1_D11	23
	AA	Y	W	V	U	T	R	