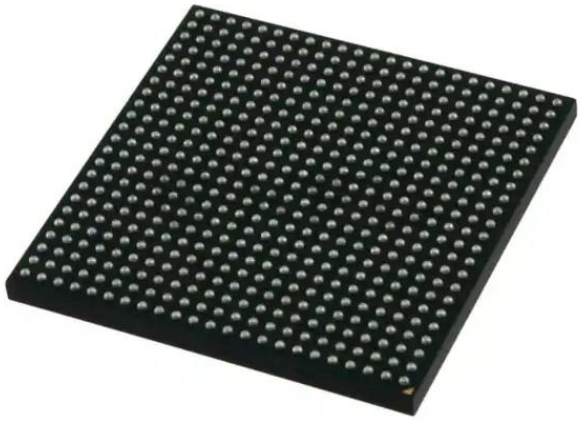

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx512djm8c

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

4.1.2 USB PHY Current Consumption

Table 17 shows the USB PHY current consumption.

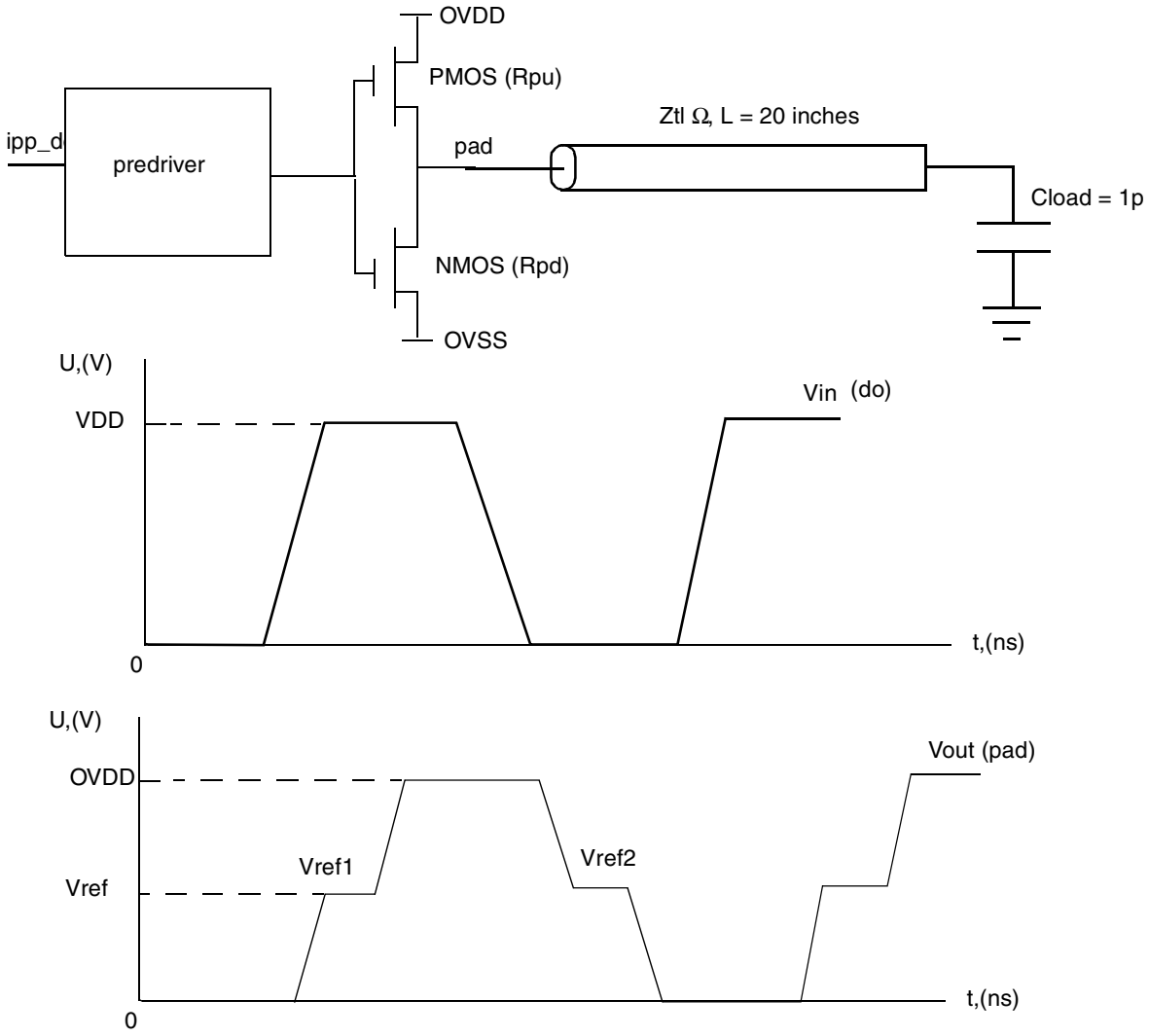
Table 17. USB PHY Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply VDDA33 (3.3 V)	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply NVCC_USBPHY (2.5 V)	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	6	7	mA
		TX	6	7	
	High Speed	RX	6	7	
		TX	6	7	
VDDA33 + NVCC_USBPHY + VCC	Suspend		50	100	µA

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX51 processor (worst-case scenario)



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 3. Impedance Matching Load for Measurement

Table 34. I^2C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	10/74	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	7/14	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	17	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	30	—	67	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	15	—	34	ns

Table 35. Low Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Medium drive)	tdit	—	—	—	22	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	11	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time greater than 25 ns

Table 36. High Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	3/3 6/5	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	5/5 9/9	ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time > 25 ns

4.5.4 AC Electrical Characteristics for DDR2

The load circuit for output pads, the output pad transition time waveform and the output pad propagation and transition time waveform are below.

Figure 10 shows the output pad transition time waveform.

Figure 10. Output Pad Transition Time Waveform

Figure 11 shows the output pad propagation and transition time waveform.

Figure 11. Output Pad Propagation and Transition Time Waveform

AC electrical characteristics in DDR2 mode for fast mode and for ovdd = 1.65 – 1.95 V, ipp_hve = 0 are placed in Table 37.

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.57/0.57 1.29/1.29	0.45/0.44 0.97/0.94	0.45/0.45 0.82/0.85	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	0.98/0.96 1.47/1.50	1.27/1.19 1.63/1.57	1.89/1.72 2.20/2.07	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	2.05/2.05 0.91/0.91	2.40/2.45 1.11/1.15	2.20/2.20 1.21/1.16	V/ns

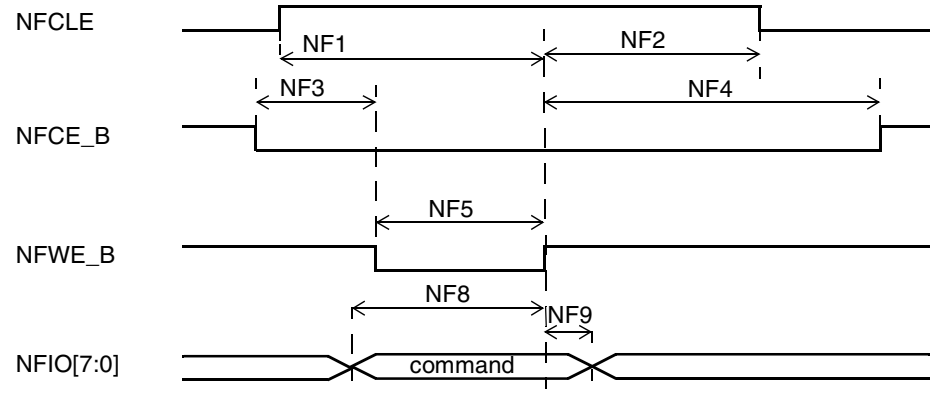


Figure 14. Command Latch Cycle Timing

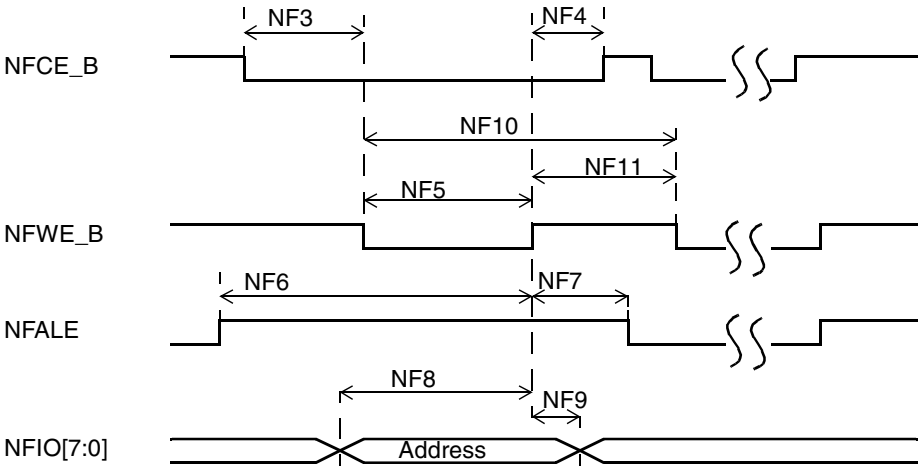


Figure 15. Address Latch Cycle Timing

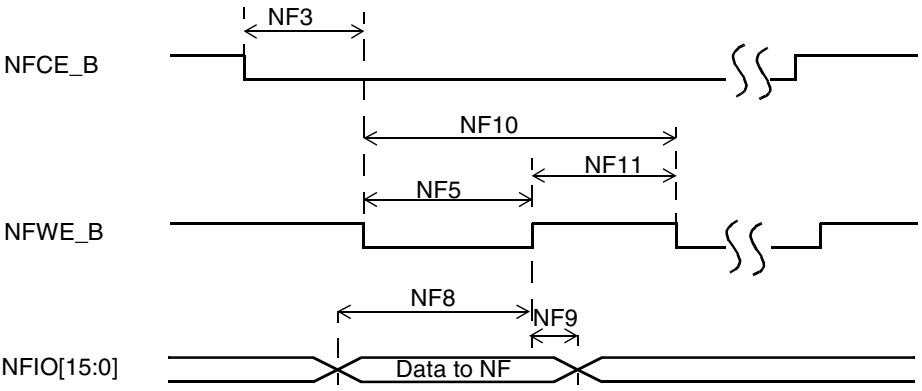


Figure 16. Write Data Latch Timing

4.6.8 SDRAM Controller Timing Parameters

4.6.8.1 Mobile DDR SDRAM Timing Parameters

Figure 32 shows the basic timing parameters for mobile DDR (mDDR) SDRAM. The timing parameters for this diagram is shown in Table 55.

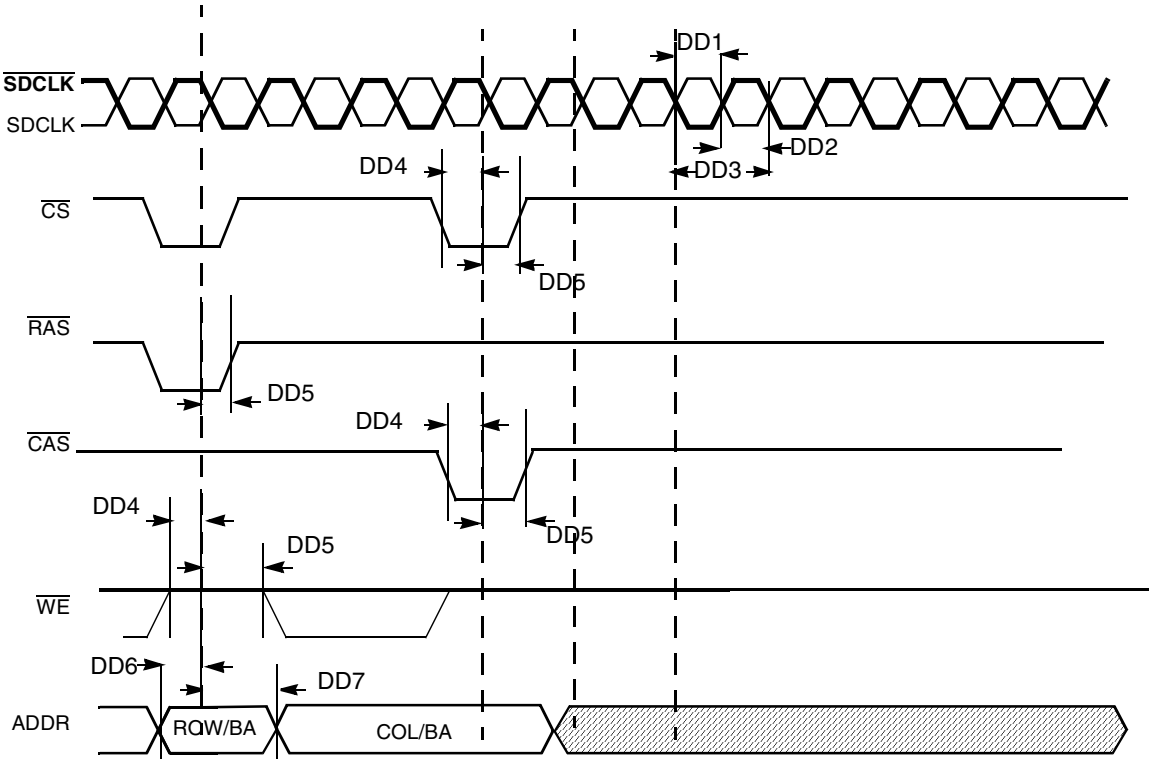


Figure 32. mDDR SDRAM Basic Timing Parameters

Table 55. mDDR SDRAM Timing Parameter Table

ID	Parameter	Symbol	200 MHz		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD1	SDRAM clock high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD2	SDRAM clock low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD3	SDRAM clock cycle time	t_{CK}	5	—	6	—	7.5	—	ns
DD4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns
DD6	Address output setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD7	Address output hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns

[1] This parameter is affected by pad timing. if the slew rate is < 1 V/ns, 0.2 ns should be added to the value. For cmos65 pads this is true for medium and low drive strengths.

Figure 33 shows the timing diagram for mDDR SDRAM write cycle. The timing parameters for this diagram is shown in Table 56.

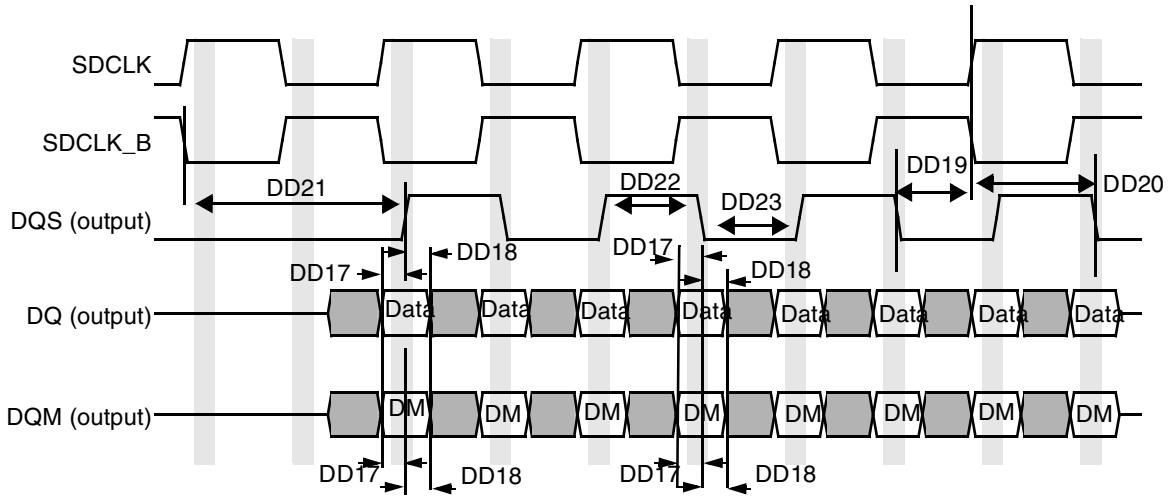


Figure 33. mDDR SDRAM Write cycle Timing Diagram

Table 56. mDDR SDRAM Write Cycle Parameter Table[1]

ID	Parameter	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD17	DQ and DQM setup time to DQS	t_{DS}[3]	0.48	—	0.6	—	0.8	—	ns
DD18	DQ and DQM hold time to DQS	t_{DH}[1]	0.48	—	0.6	—	0.8	—	ns
DD19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.2	—	0.2	—	0.2	—	tCK
DD20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.2	—	0.2	—	0.2	—	tCK
DD21	Write command to first DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DD22	DQS high level width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DD23	DQS low level width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	tCK

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

3 This parameter is affected by pad timing. If the slew rate is < 1 V/ns, 0.1 ns should be increased to this value.

Table 66. CSPI Slave Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	MOSI Hold Time	t_{Hmosi}	5	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	0	35	ns

4.7.2 eCSPI Timing Parameters

This section describes the timing parameters of the eCSPI. The eCSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

4.7.2.1 eCSPI Master Mode Timing

Figure 40 depicts the timing of eCSPI in Master mode and Table 67 lists the eCSPI Master Mode timing characteristics.

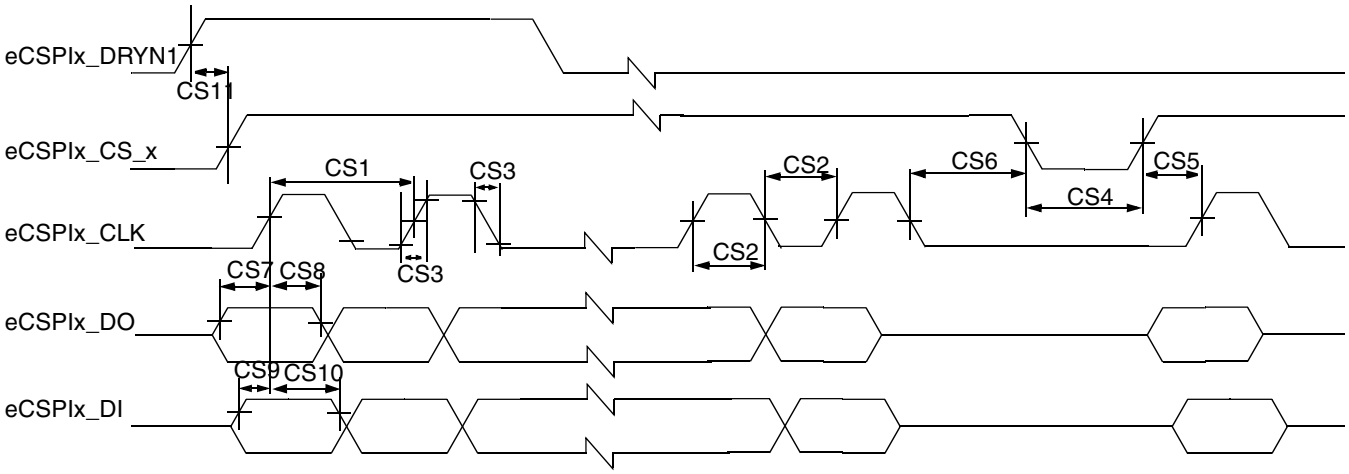


Figure 40. eCSPI Master Mode Timing Diagram

Table 67. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns

4.7.6.1 Standard and Fast Mode Timing Parameters

Figure 47 depicts the standard and fast mode timings of HS-I^{2}C module, and Table 75 lists the timing characteristics.

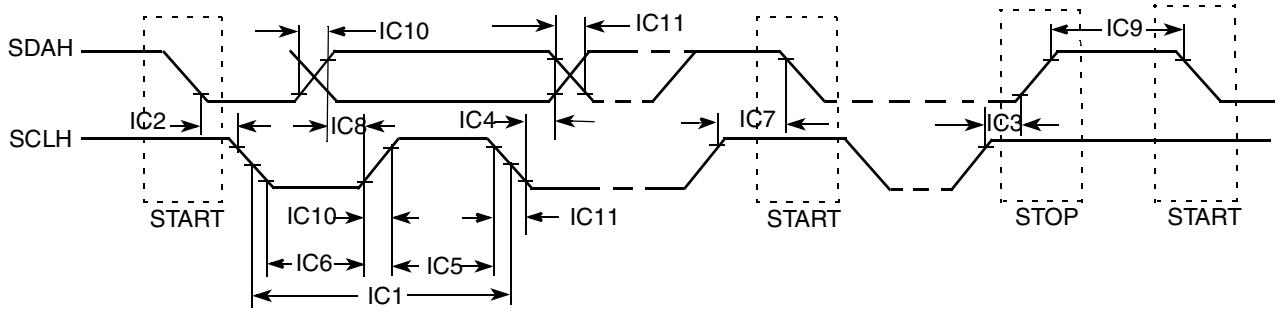


Figure 47. HS-I^{2}C Standard and Fast Mode Bus Timing

Table 75. HS-I^{2}C Timing Parameters—Standard and Fast Mode

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	SCLH cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of SCLH Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the SCLH Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both SDAH and SCLH signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both SDAH and SCLH signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	100	—	100	pF

1 A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC6) of the SCLH signal

3 A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement of Set-up time (ID No IC8) of 250 ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCLH signal.

If such a device does stretch the LOW period of the SCLH signal, it must output the next data bit to the SDAH line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLH line is released.

4 C_b = total capacitance of one bus line in pF.

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET— offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET— offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.75ns$$

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

[3] Display interface clock up time

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_UP}{DI\_CLK\_PERIOD}\right]\right)$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.7.8.6 Interface to a TV Encoder

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The timing of the interface is described in Figure 57.

NOTE

- The frequency of the clock DISP_CLK is 27 MHz (within 10%)
- The HSYNC, VSYNC signals are active low.
- The DRDY signal is shown as active high.
- The transition to the next row is marked by the negative edge of the HSYNC signal. It remains low for a single clock cycle
- The transition to the next field/frame is marked by the negative edge of the VSYNC signal. It remains low for at least one clock cycles

  — At a transition to an odd field (of the next frame), the negative edges of VSYNC and HSYNC coincide.

  — At a transition is to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the HSYNC signal being high.

[15]Display RS down time

$$Tdicdcs = (T_{DI\_CLK} \times ceil)\left[\frac{DISP\_CS\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]$$

DISP_CS_DOWN is predefined in REGISTER.

4.7.9 1-Wire Timing Parameters

Figure 68 depicts the RPP timing and Table 86 lists the RPP timing parameters.

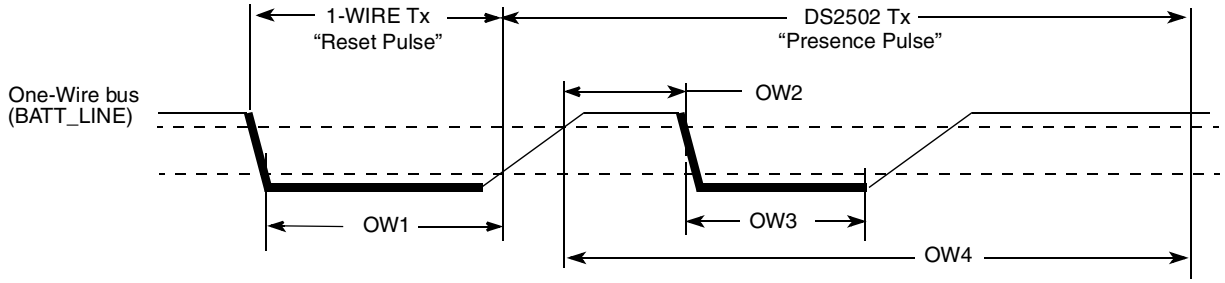


Figure 68. Reset and Presence Pulses (RPP) Timing Diagram

Table 86. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 69 depicts Write 0 Sequence timing, and Table 87 lists the timing parameters.

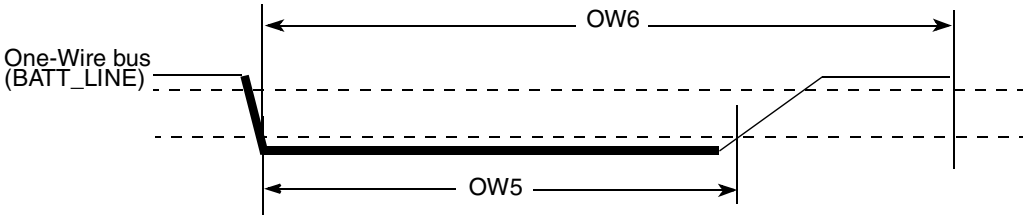


Figure 69. Write 0 Sequence Timing Diagram

Table 87. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Table 90 and Figure 73 define the AC characteristics of all the P-ATA interface signals on all data transfer modes.

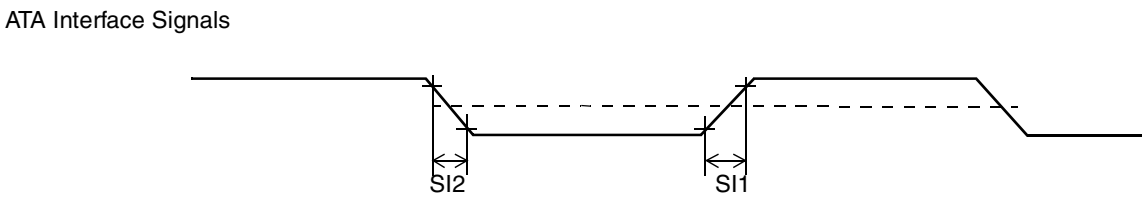


Figure 73. P-ATA Interface Signals Timing Diagram

Table 90. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface.[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface (see note)	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user needs to use level shifters for 5.0 V compatibility on the ATA interface. The i.MX51 P-ATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-4) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX51 P-ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Each of these steps is done in one CKIL period (usually 32 kHz). Power-down can be started because of a SIM Card removal detection or launched by the processor. Figure 87 and Table 98 shows the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

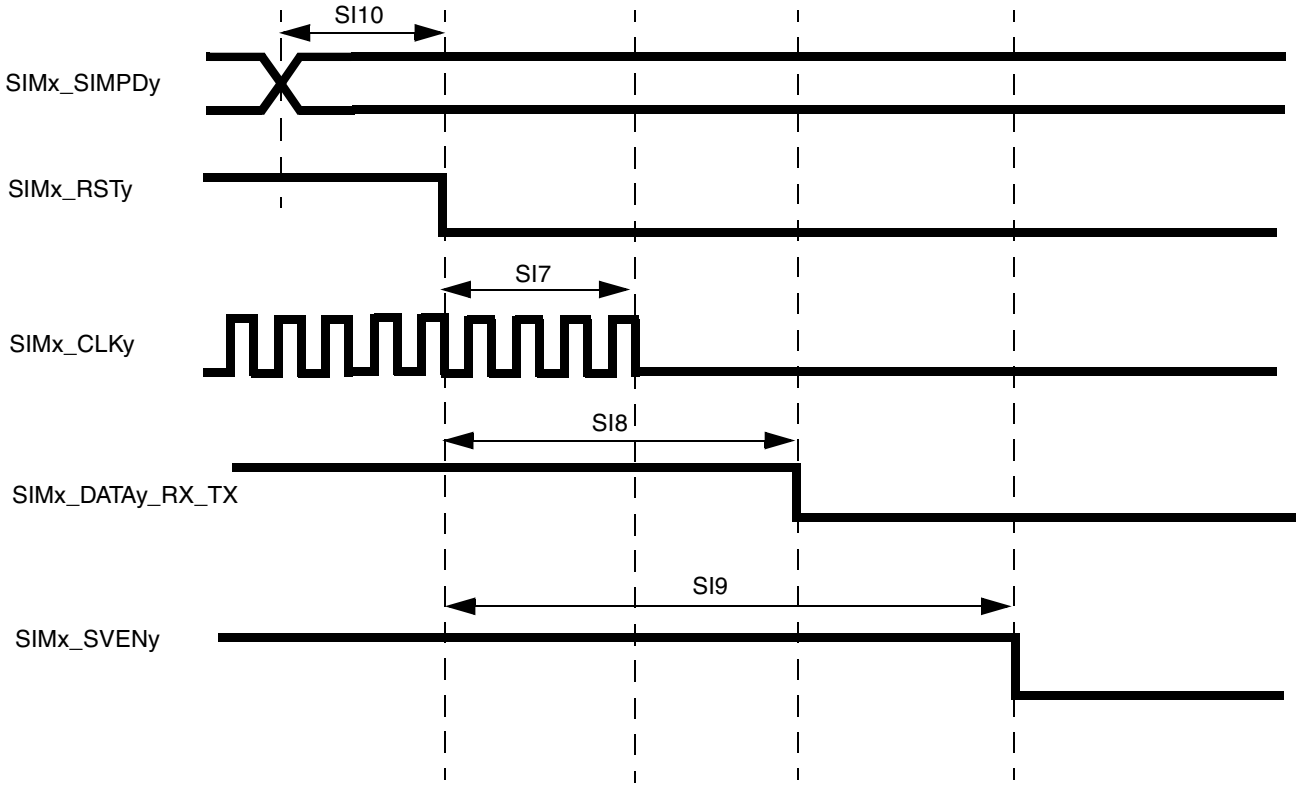


Figure 87. SmartCard Interface Power Down AC Timing

Table 98. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9×1/Fckil	1.1×1/Fckil	ns
SI8	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8×1/Fckil	2.2×1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7×1/Fckil	3.3×1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9×1/Fckil	1.1×1/Fckil	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16 UART

Table 106 shows the UART I/O configuration based on which mode is enabled.

Table 106. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.7.16.1 UART Electrical

This section describes the electrical information of the UART module.

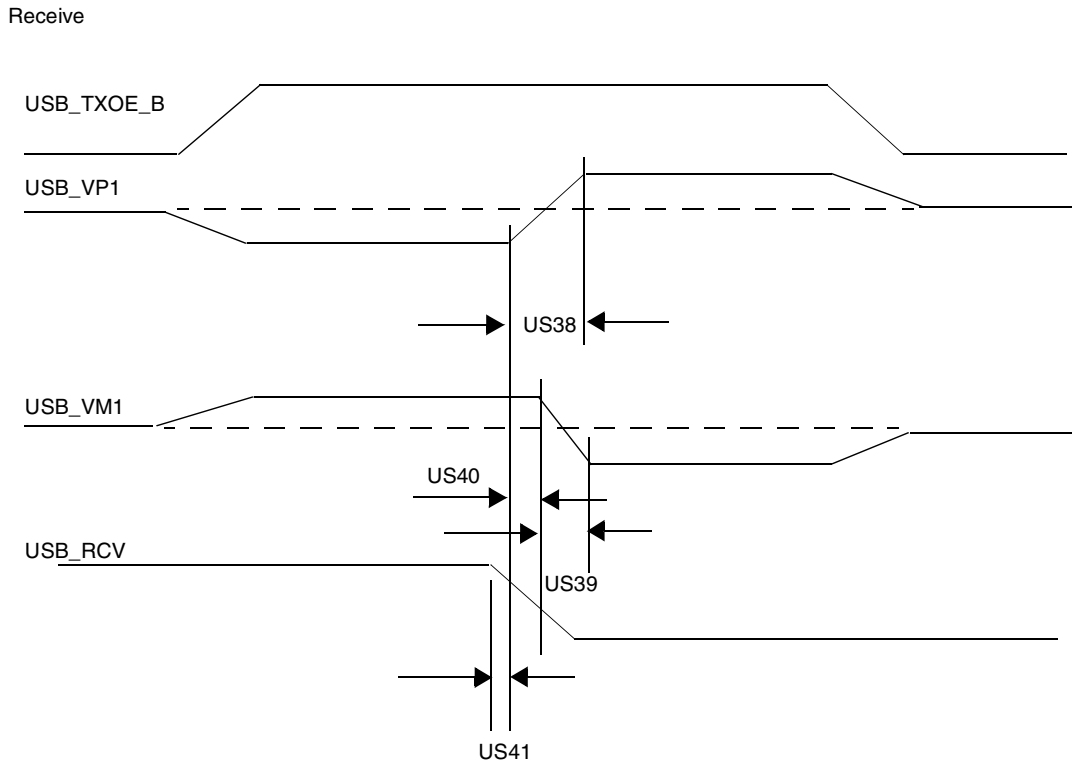


Figure 107. USB Receive Waveform in VP_VM Uni-directional Mode

Table 120 shows the USB port timing specification in VP_VM uni-directional mode.

Table 120. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Signal	Direction	Min	Max	Unit	Conditions / Reference Signal
US30	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP
US38	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US39	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US40	RX Skew	USB_VP1	In	–4.0	4.0	ns	USB_VM1
US41	RX Skew	USB_RCV	In	–6.0	2.0	ns	USB_VP1

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
CSI1_D19	N22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D8	A20	NVCC_PER8	GPIO	Input	Keeper
CSI1_D9	B20	NVCC_PER8	GPIO	Input	Keeper
CSI1_HSYNC	C19	NVCC_PER8	GPIO	Input	Keeper
CSI1_MCLK	F19	NVCC_PER8	GPIO	Input	Keeper
CSI1_PIXCLK	D19	NVCC_PER8	GPIO	Input	Keeper
CSI1_VSYNC	B19	NVCC_PER8	GPIO	Input	Keeper
CSI2_D12	F11	NVCC_PER9	GPIO	Input	Keeper
CSI2_D13	D8	NVCC_PER9	GPIO	Input	Keeper
CSI2_D14	M25	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D15	M24	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D16	M23	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D17	M22	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D18	A7	NVCC_PER9	GPIO	Input	Keeper
CSI2_D19	C7	NVCC_PER9	GPIO	Input	Keeper
CSI2_HSYNC	J20	NVCC_PER8	GPIO	Input	Keeper
CSI2_PIXCLK	D21	NVCC_PER8	GPIO	Input	Keeper
CSI2_VSYNC	C20	NVCC_PER8	GPIO	Input	Keeper
CSPI1_MISO	F12	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_MOSI	D9	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_RDY	A8	NVCC_PER10	GPIO	Input	Keeper
CSPI1_SCLK	D11	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS0	D10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS1	F13	NVCC_PER10	GPIO	Input	100 kΩ pull-up
DI_GP1	F20	NVCC_IPU6	GPIO	Input	Keeper
DI_GP2	K20	NVCC_IPU6	GPIO	Input	Keeper
DI_GP3	H23	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI_GP4	K23	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI1_D0_CS	W20	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	T18	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J22	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	V18	NVCC_IPU2	GPIO	Output	High

5.2.1.1 19 x 19 mm Package Drawing Notes

The following notes apply to Figure 110.

1 All dimensions in millimeters.

2 Dimensioning and tolerancing per ASME Y14.5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5 Parallelism measurement shall exclude any effect of mark on top surface of package.

5.2.2 19 x 19 mm Signal Assignments, Power Rails, and I/O

Table 130 shows the device connection list and Table 131 displays an alpha-sorted list of the signal assignments including associated power supplies.

5.2.2.1 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Table 130 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 130. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
AHVDDRGB	Y18, AA18
AHVSSRGB	Y19, AA19
GND	A1 , A23, G5, H9, J8, J9, J10, J12, J13, J14, K8, K9, K10, K11, K12, K13, K14, L8, L9, L10, L11,L12, L13, L14, M9, M10, M11, M12, M13, M14, M15, N8, N9, N10, N11, N12, N13, N14, N15, N16, P8, P9, P10, P11, P12, P13, P14, P15, R8, R9, R10, R11,R12, R13, R14, R15, R16, T5, T16, AC1, AC21, AC23
GND_ANA_PLL_A	U7
GND_ANA_PLL_B	U17
GND_DIG_PLL_A	T7
GND_DIG_PLL_B	V18
NGND_OSC	V17
NGND_TV_BACK	T15
NGND_USBPHY	L16
NVCC_EMI	U8, U9, U10, U11, U12, V7
NVCC_EMI_DRAM	H6, J6, K6, L6, M6, N6, P6, R6, T6
NVCC_HS10	M16
NVCC_HS4_1	M18
NVCC_HS4_2	N18
NVCC_HS6	M17
NVCC_I2C	T14

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_WAIT	AB4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EXTAL[2]	AB20	NVCC_OSC	Analog	Input	—
FASTR_ANA[2]	W20	NVCC_PER3	—	Input	—
FASTR_DIG[2]	Y20	NVCC_PER3	—	Input	—
GPANAIO[2]	J23	NVCC_USBPHY	Analog	Output	—
GPIO_NAND	D5	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
GPIO1_0	B21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_1	D20	NVCC_PER5	GPIO	Input	Keeper
GPIO1_2	A22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_3	D18	NVCC_PER5	GPIO	Input	Keeper
GPIO1_4	B22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_5	D19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_6	C19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_7	B23	NVCC_PER5	GPIO	Input	Keeper
GPIO1_8	C21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_9	C20	NVCC_PER5	GPIO	Input	Keeper
I2C1_CLK	W15	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
I2C1_DAT	AB16	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
ID	L19	NVCC_USBPHY	Analog	Input	Pull-up
IOB[2]	AC19	AHVDDRGB	Analog	Output	—
IOB_BACK[2]	AB19	—	Analog	Output	—
IOG[2]	AC18	AHVDDRGB	Analog	Output	—
IOG_BACK[2]	AB18	—	Analog	Output	—
IOR[2]	AC17	AHVDDRGB	Analog	Output	—
IOR_BACK[2]	AB17	—	Analog	Output	—
JTAG_DE_B	AB15	NVCC_PER14	GPIO	Input/Open-drain output	47 kΩ pull-up
JTAG_MOD	V14	NVCC_PER14	GPIO	Input	100 kΩ pull-up
JTAG_TCK	V15	NVCC_PER14	GPIO	Input	100 kΩ pull-down
JTAG_TDI	Y14	NVCC_PER14	GPIO	Input	47 kΩ pull-up
JTAG_TDO	AA15	NVCC_PER14	GPIO	3-state output	Keeper
JTAG_TMS	AC16	NVCC_PER14	GPIO	Input	47 kΩ pull-up