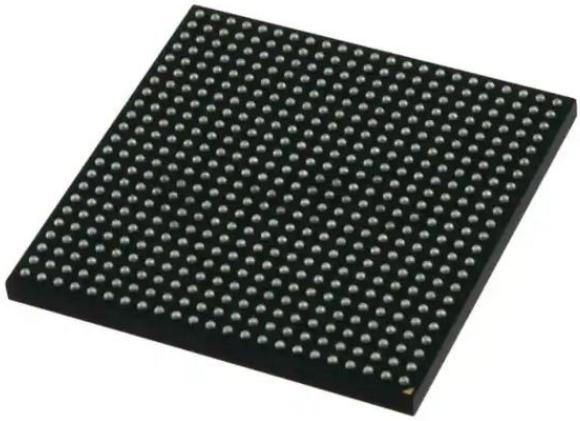

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx512djm8cr2

Table 2. i.MX51 Digital and Analog Modules (continued)

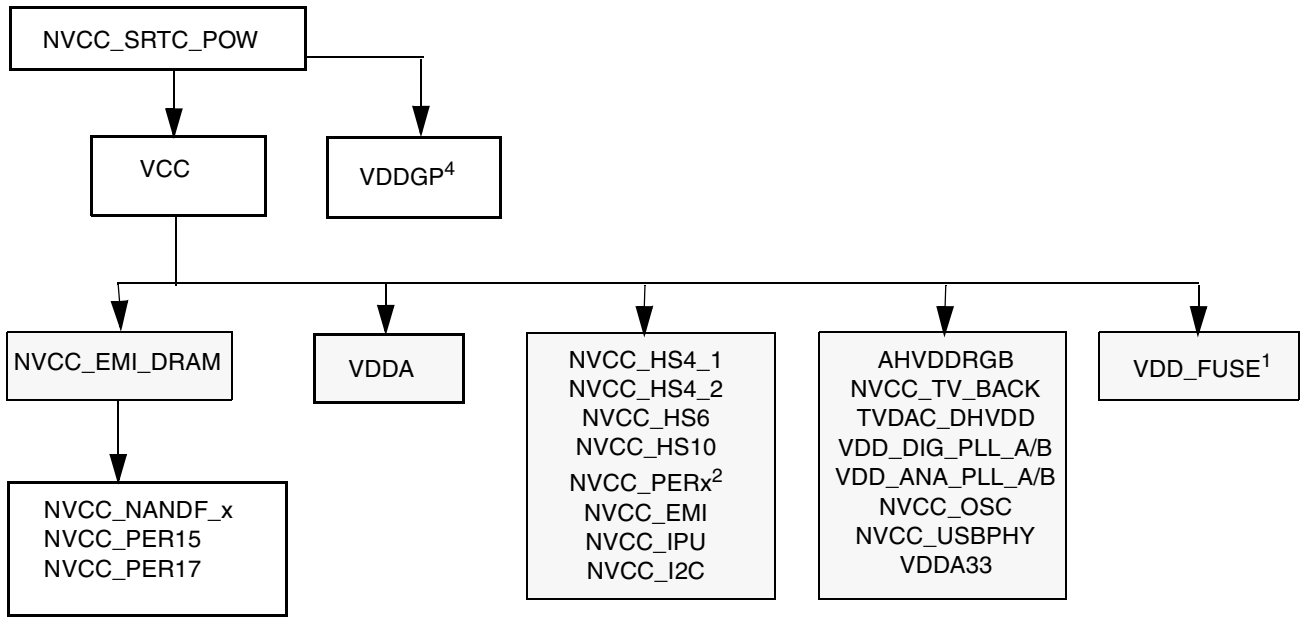
Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX51 processor incorporates a mechanism for regulating JTAG access. The i.MX51Secure JTAG Controller provides four different JTAG security modes that can be selected via e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Only the transmitter functionality is supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX51 processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two timeslots are being used simultaneously.
TVE	TV Encoder	Multimedia	The TVE is implemented in conjunction with the Image Processing Unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports the following analog video outputs: composite, S-video, and component video up to HD720p/1080i.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone Interrupt Controller (TZIC) collects interrupt requests from all i.MX51 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.



1. VDD_FUSE should only be powered when writing.
2. NVCC_PERx refers to NVCC_PER 3, 5, 8, 9, 10, 11, 12, 13, 14.
3. No power-up sequence dependencies exist between the supplies shown in the block diagram shaded in gray.
4. There is no requirement for VDDGP to be preceded by any other power supply other than NVCC_SRTC_POW.
5. If all of the UHVIO supplies (NVCC_NANDFx, NVCC_PER15 and NVCC_PER17) are less than 2.75 V then there is no requirement on the power up sequence order between NVCC_EMI_DRAM and the UHVIO supplies. However, if the voltage is 2.75 V and above, then NVCC_EMI_DRAM needs to power up before the UHVIO supplies as shown here.

Figure 2. Power-Up Sequence

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

For more information on power up, see i.MX51 Power-Up Sequence (AN4053).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO/HSGPIO)
- Double Data Rate 2 (DDR2)
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- High-Speed I^2C and I^2C
- Enhanced Secure Digital Host Controller (eSDHC)

4.3.7 USB Port Electrical DC Characteristics

Table 23 and Table 24 list the electrical DC characteristics.

Table 23. USBOTG Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	VDD x 0.7	VDD	V	—
Input low Voltage	VIL	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	0	VDD × 0.3	V	—
Output High Voltage	VOH	USB_VPOUT USB_VMOUT USB_TXENB	VDD – 0.43	—	V	7 mA Drv at IOH = 5 mA
Output Low Voltage	VOL	USB_VPOUT USB_VMOUT USB_TXENB	—	0.43	V	7 mA Drv at IOH = 5 mA

Table 24. USB Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	VDD x 0.7	VDD	V	—
Input Low Voltage	VIL	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	0	VDD x 0.3	V	—
Output High Voltage	VOH	USB_DAT_VP USB_SE0_VM USB_TXOE_B	VDD –0.43	—	V	7 mA Drv at Iout = 5 mA
Output Low Voltage	VOL	USB_DAT_VP USB_SE0_VM USB_TXOE_B	—	0.43	V	7 mA Drv at Iout = 5 mA

Table 29. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Low drive)	tdit	—	—	—	7	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.2 Fast I/O AC Parameters

Table 30 shows the fast I/O AC parameters.

Table 30. Fast I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.429/1.275 2.770/2.526	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.793/1.607 3.565/3.29	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.542/2.257 5.252/4.918	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.641/4.456 10.699/10.0	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.69/0.78 0.36/0.39	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.62 0.28/0.30	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	70	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	53	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.3 I^2C AC Parameters

NOTE

See the errata for HS-I^2C in the i.MX51 Chip Errata document. The two standard I^2C modules have no errata

4.6.5 DPLL Electrical Parameters

Table 48 shows the DPLL electrical parameters.

Table 48. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output Duty Cycle	—	48.5	50	51.5	%
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 47.

2 The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user.Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15.Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider.According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 Tdck is the time period of the output clock, dpdck_2.

4.6.6 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among different signals of NFC at the module level in the different operational modes.

Timing parameters in Figure 14, Figure 15, Figure 16, Figure 17, Figure 19, and Table 50 show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B. Timing parameters in Figure 14, Figure 15, Figure 16, Figure 18, Figure 19, and Table 50 show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16 - 40 pF) and there is max drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock ("enfc_clk" at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider. Table 49 demonstrates few examples for clock frequency settings.

Table 49. NFC Clock Settings Examples

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T—Clock Period (ns)[1]
133 (max value)	5 (reset value)	26.6	38
133	4	33.25	31
133	3	44.33	23

[1] Rounded up to whole nanoseconds.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low the actual data bus capturing might occur after the specified trhoh (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (T = 39 ns) guarantees proper operation for devices having trhoh > 15 ns. It is also recommended to set the NFC_FREQ_SEL Fuse accordingly to initiate the boot with 33.33 MHz clock.

Lower frequency operation can be supported for most available devices in the market, relying on data lines Bus-Keeper logic. This depends on device behavior on the data bus in the time interval between data output valid to data output high-Z state. In NAND device parameters this period is marked between trhoh and trhz (RE_B high to output high-Z). In most devices, the data transition from valid value to high-Z occurs without going through other states. Setting the data bus pads to Bus-Keeper mode in the IOMUX registers, keeps the data bus valid internally after the specified hold time, allowing proper capturing with slower clock.

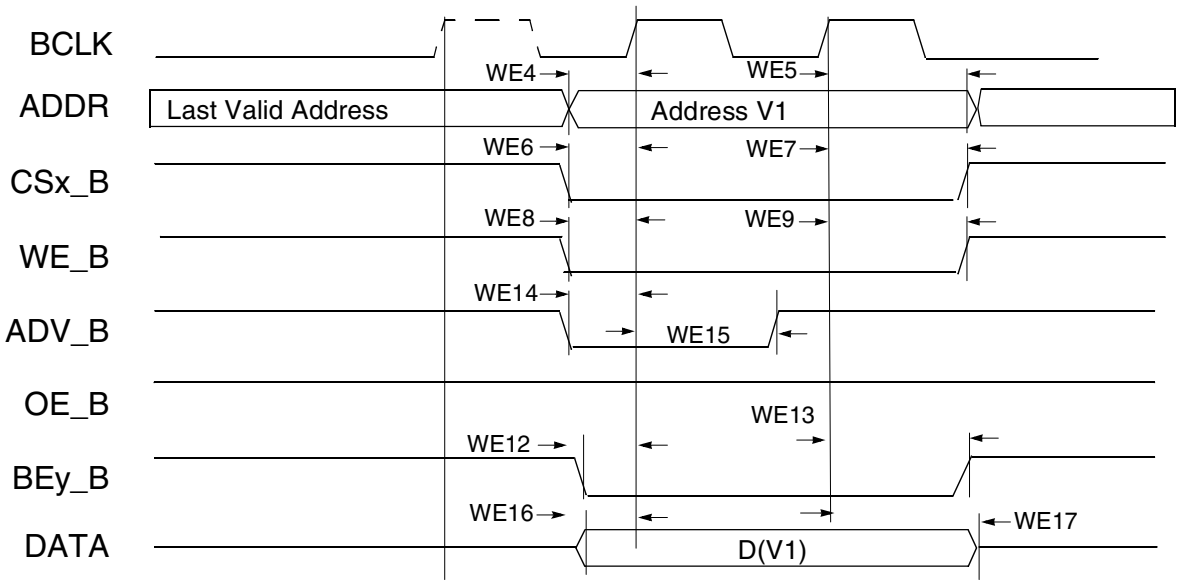


Figure 23. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

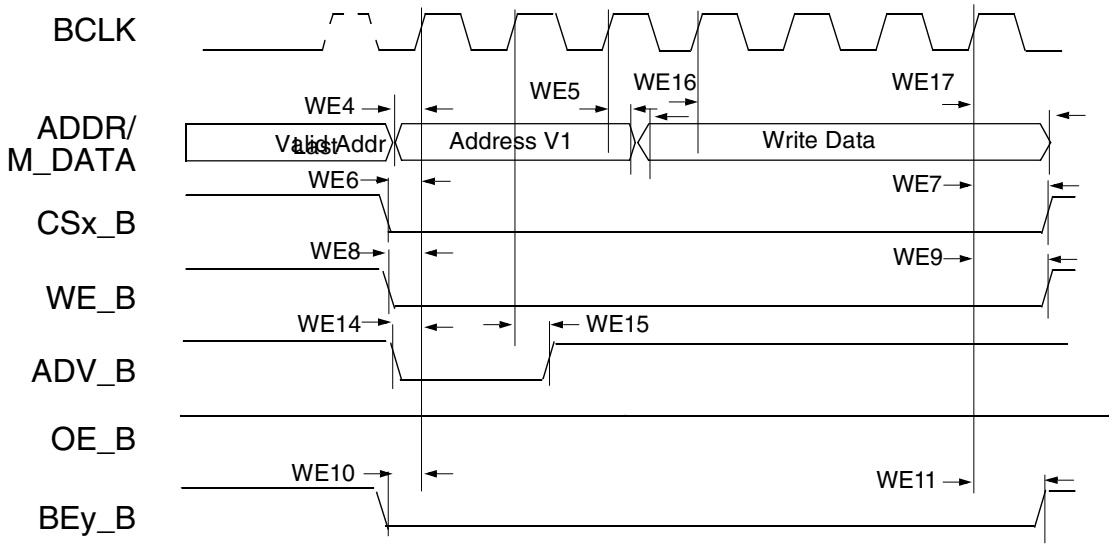


Figure 24. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

4.6.8 SDRAM Controller Timing Parameters

4.6.8.1 Mobile DDR SDRAM Timing Parameters

Figure 32 shows the basic timing parameters for mobile DDR (mDDR) SDRAM. The timing parameters for this diagram is shown in Table 55.

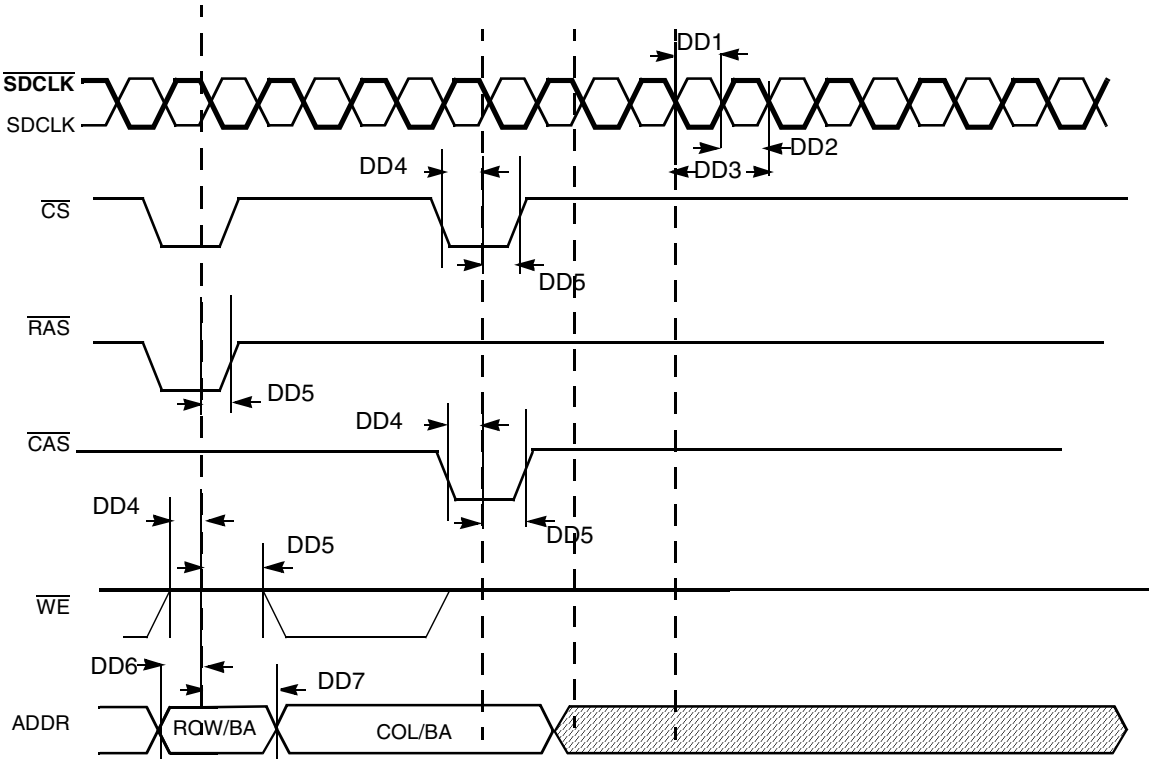


Figure 32. mDDR SDRAM Basic Timing Parameters

Table 55. mDDR SDRAM Timing Parameter Table

ID	Parameter	Symbol	200 MHz		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD1	SDRAM clock high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD2	SDRAM clock low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD3	SDRAM clock cycle time	t_{CK}	5	—	6	—	7.5	—	ns
DD4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns
DD6	Address output setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD7	Address output hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns

[1] This parameter is affected by pad timing. if the slew rate is < 1 V/ns, 0.2 ns should be added to the value. For cmos65 pads this is true for medium and low drive strengths.

4.7.4.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 72 lists MII asynchronous inputs signal timing information. Figure 45 shows MII asynchronous input timings listed in Table 72.

Table 72. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

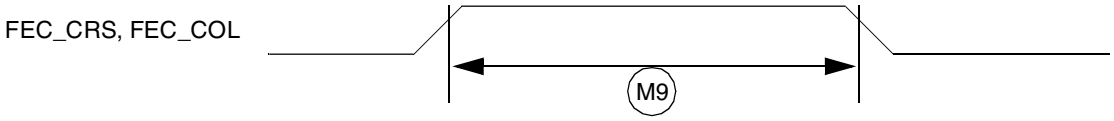


Figure 45. MII Async Inputs Timing Diagram

4.7.4.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 73 lists MII serial management channel timings. Figure 46 shows MII serial management channel timings listed in Table 73. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 73. MII Transmit Signal Timing

ID	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

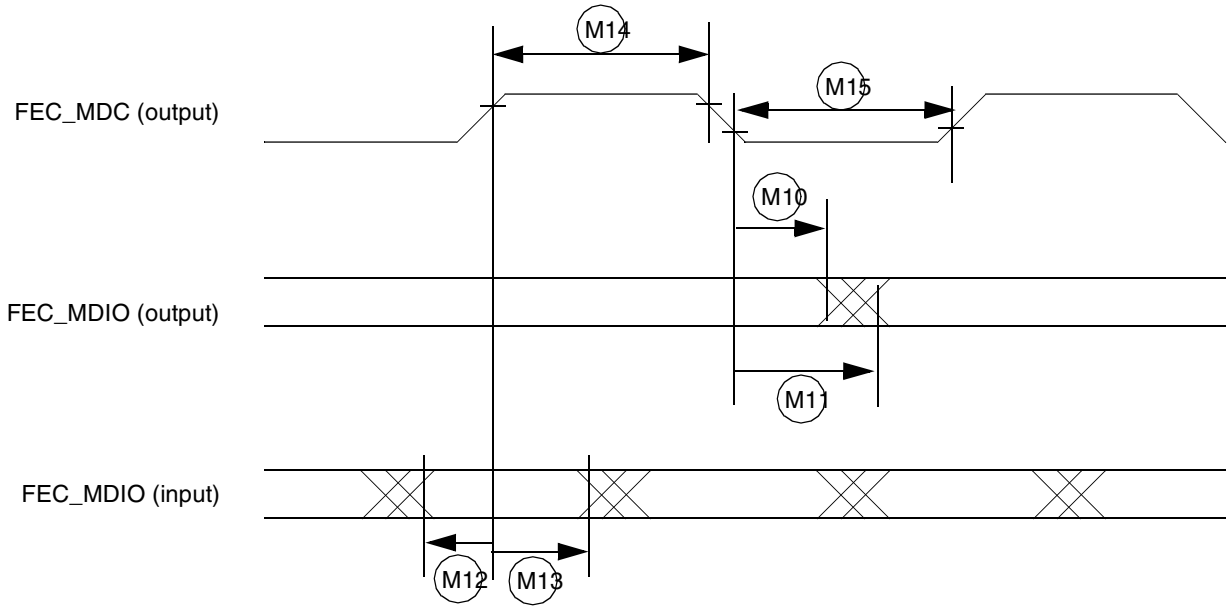


Figure 46. MII Serial Management Channel Timing Diagram

4.7.5 Frequency Pre-Multiplier (FPM) Electrical Parameters (CKIL)

The FPM is a DPLL that converts a signal operating in the kilohertz region into a clock signal operating in the megahertz region. The output of the FPM provides the reference frequency for the on-chip DPLLs. Parameters of the FPM are listed in Table 74.

Table 74. FPM Specifications

Parameter	Min	Typ	Max	Unit
Reference clock frequency range—CKIL	32	32.768	256	kHz
FPM output clock frequency range	8	—	33	MHz
FPM multiplication factor (test condition is changed by a factor of 2)	128	—	1024	—
Lock-in time[1]	—	—	312.5	µs
Cycle-to-cycle frequency jitter (peak to peak)	—	8	20	ns

[1] pIrf = 1 cycle assumed missed + x cycles for reset deassert + y cycles for calibration and lock x[ts] = {2,3,5,9}; y[ts] = {7,8,10,14}; where ts is the chosen time scale of the reference clock. In this case reference clock = 32 kHz which makes ts = 0, therefore total time required for achieving lock is 10(1+2+7) cycles or 312.5 µs.

4.7.6 High-Speed I^{2}C (HS-I^{2}C) Timing Parameters

This section describes the timing parameters of the HS-I^{2}C module. This module can operate in the following modes: Standard, Fast and High speed.

NOTE

See the errata for the HS-I^{2}C module in the i.MX51 Chip Errata. There are two standard I^{2}C modules that have no errata.

4.7.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C Module. Figure 49 depicts the timing of I²C module, and Table 77 lists the I²C Module timing characteristics.

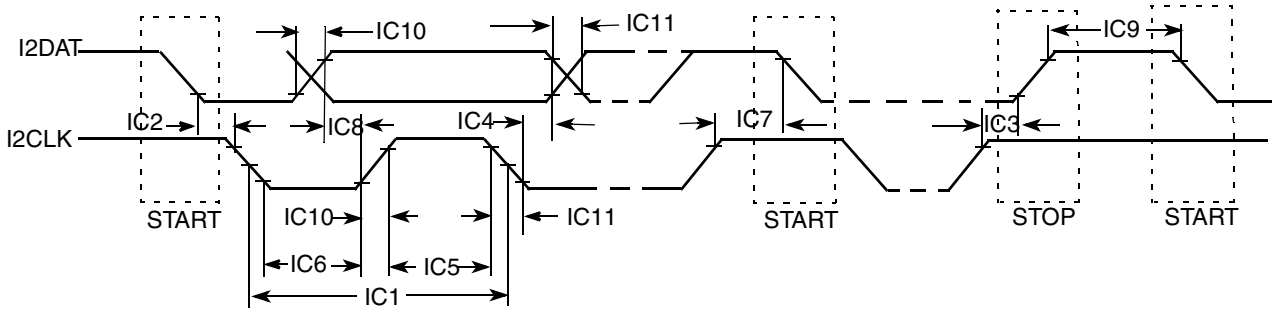


Figure 49. I²C Bus Timing

Table 77. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: display processing, image conversions, and other related functions.
- Synchronization and control capabilities such as avoidance of tearing artifacts.

4.7.8.1 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.1.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.1.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 50.

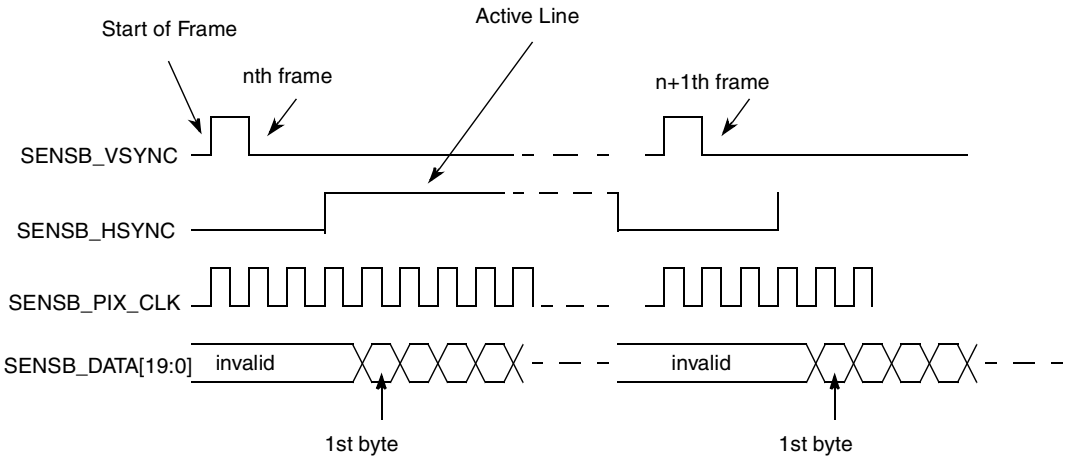


Figure 50. Gated Clock Mode Timing Diagram

joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

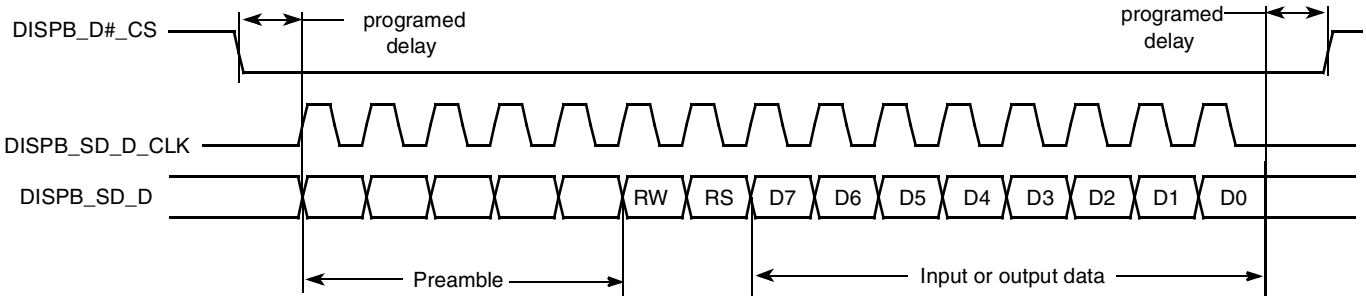


Figure 64. 3-Wire Serial Interface Timing Diagram

Figure 65 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

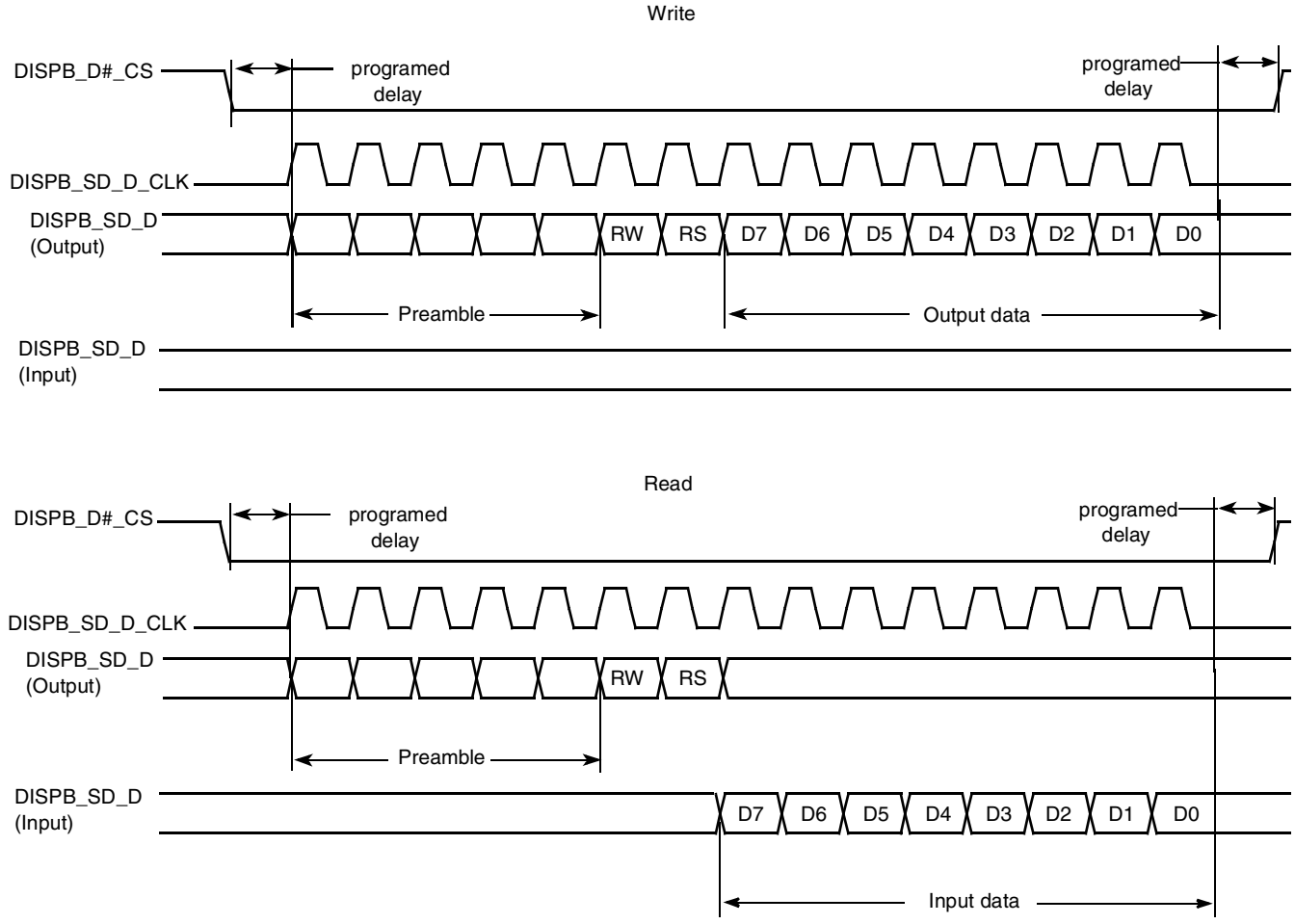


Figure 65. 4-Wire Serial Interface Timing Diagram

Figure 72 depicts the timing of the PWM, and Table 89 lists the PWM timing parameters.

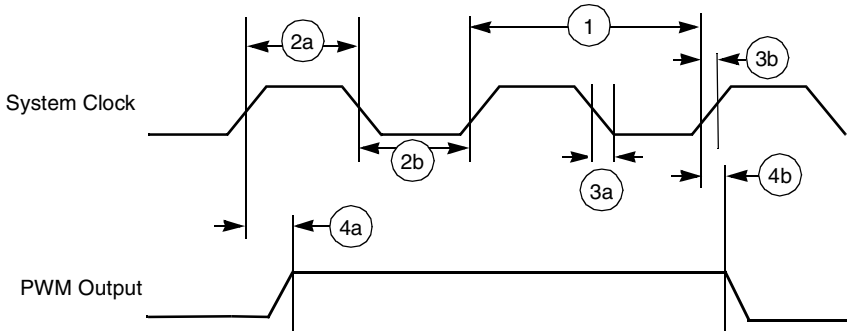


Figure 72. PWM Timing

Table 89. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.11 P-ATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-5 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 66 Mbyte/s. Parallel ATA module interface consist of a total of 29 pins, Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-5 specification and these requirements are configurable by the ATA module registers.

Table 91 shows ATA timing parameters.

Table 91. P-ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	Peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4	 15 ns 10 ns 7 ns 5 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4	 5.0 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver
tbuf	Max buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

4.7.13 SCAN JTAG Controller (SJC) Timing Parameters

Figure 88 depicts the SJC test clock input timing. Figure 89 depicts the SJC boundary scan timing. Figure 91 depicts the TRST timing with respect to TCK. Figure 90 depicts the SJC test access port. Signal parameters are listed in Table 99.

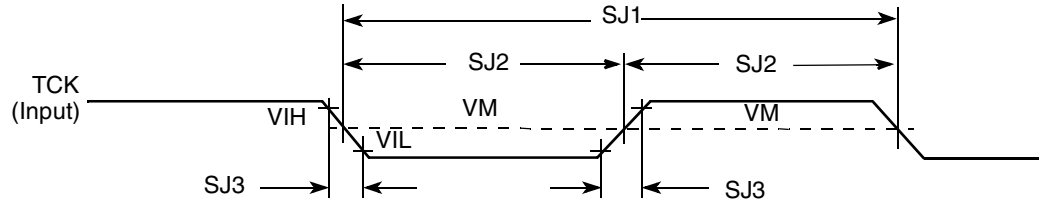


Figure 88. Test Clock Input Timing Diagram

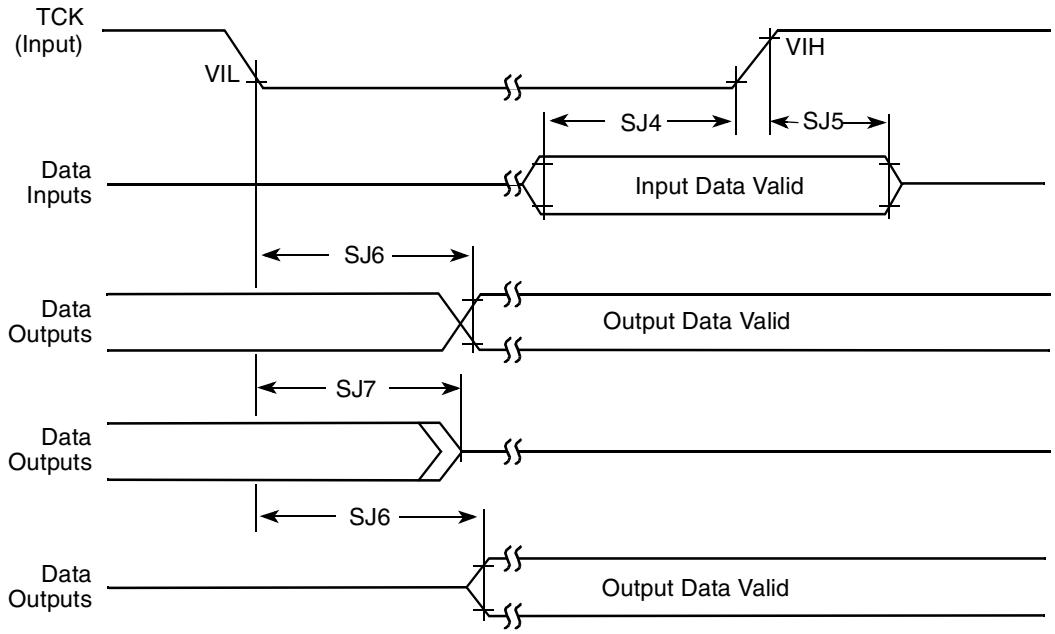


Figure 89. Boundary Scan (JTAG) Timing Diagram

Table 114. Definitions of USB Receive Waveform in DAT_SE0 Bi-Directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions/ Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 USB DAT_SE0 Unidirectional Mode

Table 115 shows the signal definitions in DAT_SE0 unidirectional mode

Table 115. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential RX data when USB_TXOE_B is high

Figure 102 and Figure 103 shows the USB transmit/receive waveform in DAT_SE0 uni-directional mode respectively.

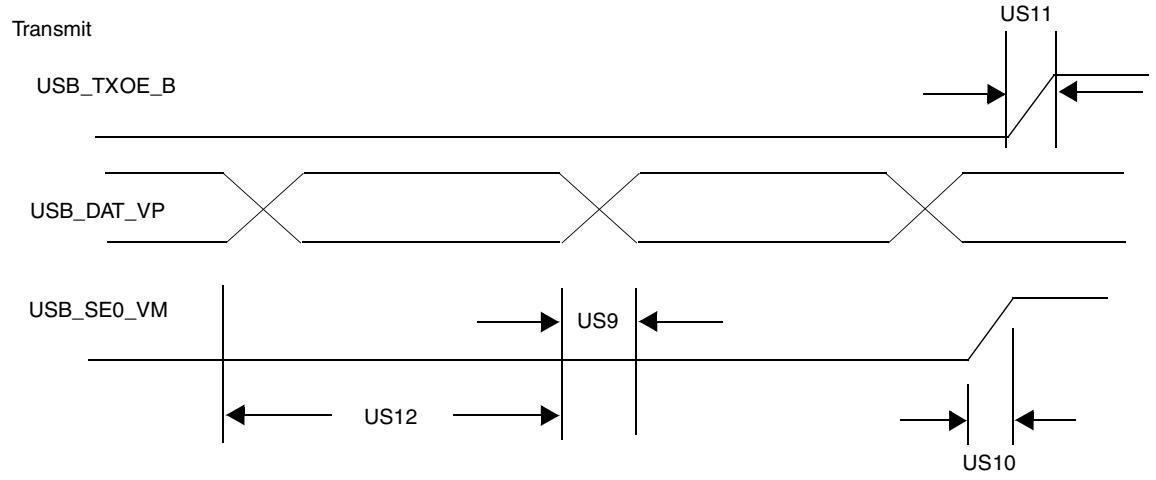


Figure 102. USB Transmit Waveform in DAT_SE0 Uni-directional Mode

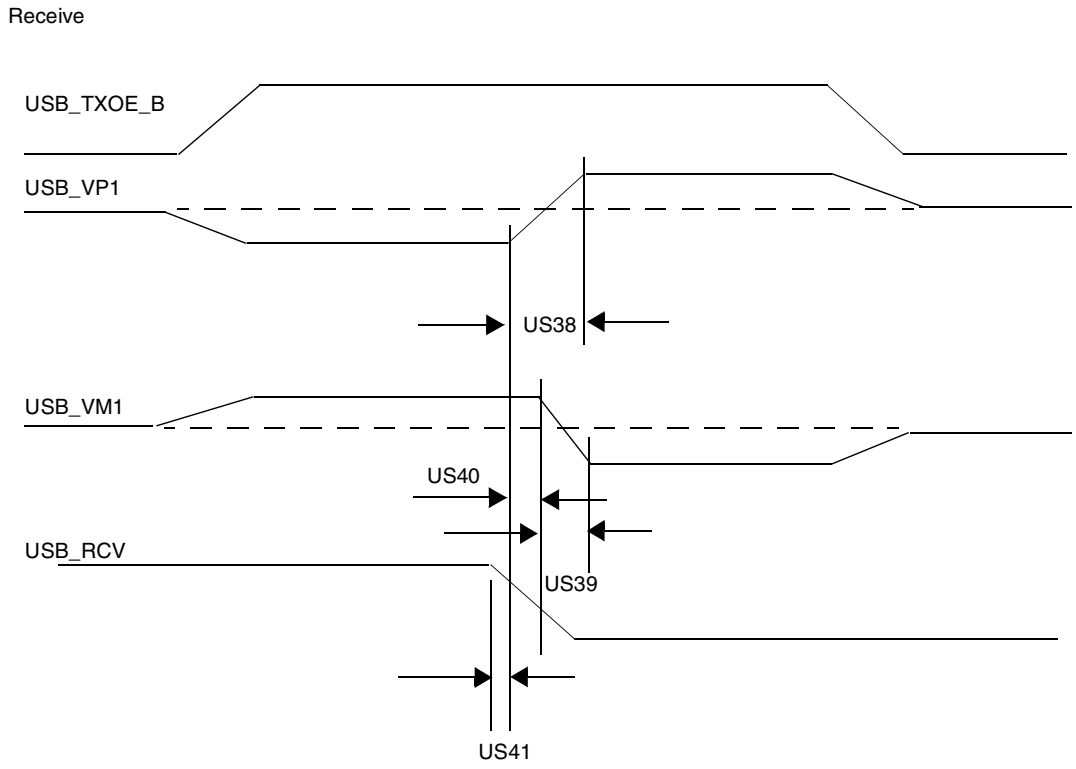


Figure 107. USB Receive Waveform in VP_VM Uni-directional Mode

Table 120 shows the USB port timing specification in VP_VM uni-directional mode.

Table 120. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Signal	Direction	Min	Max	Unit	Conditions / Reference Signal
US30	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP
US38	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US39	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US40	RX Skew	USB_VP1	In	–4.0	4.0	ns	USB_VM1
US41	RX Skew	USB_RCV	In	–6.0	2.0	ns	USB_VP1

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_WAIT	AB4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EXTAL[2]	AB20	NVCC_OSC	Analog	Input	—
FASTR_ANA[2]	W20	NVCC_PER3	—	Input	—
FASTR_DIG[2]	Y20	NVCC_PER3	—	Input	—
GPANAIO[2]	J23	NVCC_USBPHY	Analog	Output	—
GPIO_NAND	D5	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
GPIO1_0	B21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_1	D20	NVCC_PER5	GPIO	Input	Keeper
GPIO1_2	A22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_3	D18	NVCC_PER5	GPIO	Input	Keeper
GPIO1_4	B22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_5	D19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_6	C19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_7	B23	NVCC_PER5	GPIO	Input	Keeper
GPIO1_8	C21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_9	C20	NVCC_PER5	GPIO	Input	Keeper
I2C1_CLK	W15	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
I2C1_DAT	AB16	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
ID	L19	NVCC_USBPHY	Analog	Input	Pull-up
IOB[2]	AC19	AHVDDRGB	Analog	Output	—
IOB_BACK[2]	AB19	—	Analog	Output	—
IOG[2]	AC18	AHVDDRGB	Analog	Output	—
IOG_BACK[2]	AB18	—	Analog	Output	—
IOR[2]	AC17	AHVDDRGB	Analog	Output	—
IOR_BACK[2]	AB17	—	Analog	Output	—
JTAG_DE_B	AB15	NVCC_PER14	GPIO	Input/Open-drain output	47 kΩ pull-up
JTAG_MOD	V14	NVCC_PER14	GPIO	Input	100 kΩ pull-up
JTAG_TCK	V15	NVCC_PER14	GPIO	Input	100 kΩ pull-down
JTAG_TDI	Y14	NVCC_PER14	GPIO	Input	47 kΩ pull-up
JTAG_TDO	AA15	NVCC_PER14	GPIO	3-state output	Keeper
JTAG_TMS	AC16	NVCC_PER14	GPIO	Input	47 kΩ pull-up