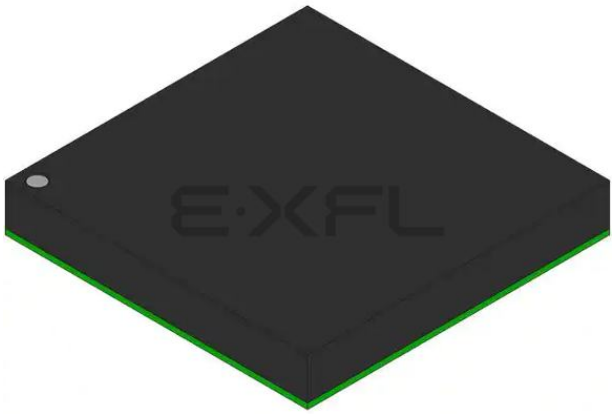

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 95°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx513cjm6c

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	IPU enables connectivity to displays and image sensors, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces. • Legacy Interfaces • Analog TV interfaces (through a TV encoder bridge) The processing includes: • Support for camera control • Image enhancement: color adjustment and gamut mapping, gamma correction and contrast enhancement, sharpening and noise reduction • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Synchronization and control capabilities, allowing autonomous operation. • Hardware de-interlacing support
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
P-ATA (Muxed with eSDHC-4	Parallel ATA	Connectivity Peripherals	The P-ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA-5 (UDMA-4) compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. This is muxed with eSDHC-4 interfaces.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	Unified RAM, can be split between Secure RAM and Non-Secure RAM
ROM 36 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes

Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xD products (Consumer)	ARM core supply voltage $0 \leq f_{ARM} \leq 167$ MHz	0.8	0.85	1.15	V
	ARM core supply voltage $167 < f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VDDGP MCIMX51xC products (Industrial)	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.10	V
	ARM core supply voltage Stop mode	0.90	0.95	1.05	V
VCC MCIMX51xD products (Consumer)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage Low Performance Mode (LPM) The clock frequencies are derived from AXI and AHB buses at 44 MHz and a DDR clock rate of DDR Clock/3. DDR2 does not support frequencies below 125 MHz per JEDEC.	1.00	1.05	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VCC MCIMX51xC products (Industrial)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.90	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output. The association is shown in Table 128 and Table 131.

4.3.1 GPIO/HSGPIO DC Parameters

The parameters in Table 18 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 18. GPIO/HSGPIO DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = -1 mA	OVDD –0.15	—	OVDD + 0.3	V
Low-level output voltage	Vol	Iout = 1mA	—	—	0.15	V
High-level output current	Ioh	Vout = 0.8×OVDD Low drive Medium drive High drive Max drive	 –1.9 –3.7 –5.2 –6.6	—	—	mA
Low-level output current	Iol	Vout = 0.2×OVDD Low drive Medium drive High drive Max drive	 1.9 3.7 5.2 6.6	—	—	mA
High-Level DC input voltage[1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3×OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 OVDD = 2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+[1, 2]	VT+	—	0.5OVDD	—	—	V
Schmitt trigger VT-[1, 2]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	—	—	See Note [3]	—
Input current (22 kΩ Pull-up)	Iin	Vin = 0	—	—	161	µA
Input current (47 kΩ Pull-up)	Iin	Vin = 0	—	—	76	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0	—	—	36	µA
Input current (100 kΩ Pull-down)	Iin	Vin = OVDD	—	—	36	µA
Keeper Circuit Resistance	—	OVDD = 1.875V OVDD = 2.775V	— —	22 17	— —	kΩ

1 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3 I/O leakage currents are listed in Table 25.

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt[1]	di/dt	—	390	201	99	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Slow mode and for ovdd=1.65 – 1.95 V, ipp_hve = 0 are placed in Table 38:

Table 38. AC Electrical Characteristics of DDR2 IO Pads for Slow Mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.75/0.76 1.39/1.40	0.70/0.74 1.18/1.21	1.06/1.00 1.49/1.47	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.50/1.55 2.05/2.16	1.90/1.95 2.36/2.48	3.23/3.10 3.82/3.75	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	1.56/1.54 0.84/0.84	1.54/1.46 0.92/0.89	0.93/0.99 0.66/0.67	V/ns
Output Pad di/dt[1]	di/dt	—	82	40	19	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 44.

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.42 3.01/2.96	1.20/1.27 2.38/2.40	1.43/1.49 2.37/2.44	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.05/2.04 4.50/4.42	1.67/1.71 3.48/3.52	1.82/1.87 3.16/3.28	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.06/3.98 8.94/8.86	3.15/3.17 6.92/6.93	2.92/ 3.02 5.69/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.07/2.23 3.21/3.48	2.46/2.62 3.35/3.63	3.92/3.93 4.84/4.97	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.53/2.74 4.26/4.58	2.83/3.04 4.12/4.49	4.32/4.35 5.55/5.76	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.93/4.23 7.38/7.91	3.89/4.21 6.43/7.01	5.37/5.51 7.45/7.94	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.45	0.69/0.66 0.42/0.41	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.65/0.63 0.31/0.31	0.54/0.53 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.29 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns

Table 50. NFC—Timing Characteristics (continued)

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF21	WE high to RE low	tWHR	14T-5.45	14T-5.45	—
NF22	WE high to busy	tWB	—	—	6T

1 t_{DSR} is calculated by the following formula:
Asymmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} + {}^1/_2T - Tdl^2$
Symmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} - Tdl^2$
$t_{REpd} + t_{Dpd}$ = 11.2 ns (including clock skew)
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
t_{DSR} can be used to determine t_{REA} max parameter with the following formula: $t_{REA} = 1.5T - t_{DSR}$.

2 Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{aclk}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{aclk} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

3 NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4 NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^2 - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.7 External Interface Module (WEIM)

The following sections provide information on the WEIM.

4.6.7.1 WEIM Signal Cross Reference

Table 51 is a guide to help the user identify signals in the WEIM Chapter of the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) that are the same as those mentioned in this data sheet.

Table 51. WEIM Signal Cross Reference

Reference Manual WEIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUX Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 53.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

Figure 34 shows the timing diagram for mDDR SDRAM DQ versus DQS and SDCLK read cycle. The timing parameters for this diagram is shown in Table 57.

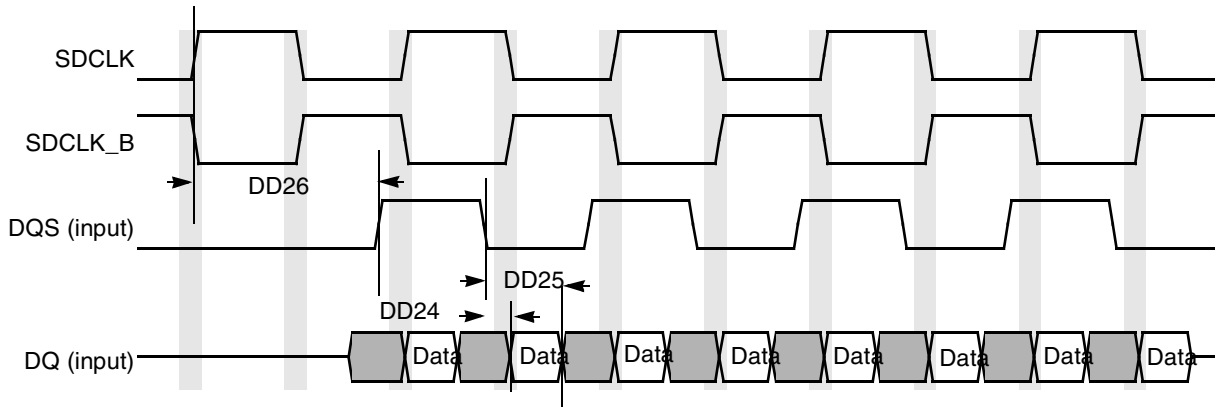


Figure 34. mDDR SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 57. mDDR SDRAM Read Cycle Parameter Table[1]

ID	PARAMETER	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.4	—	0.75	—	0.85	ns
DD25	DQS DQ in HOLD time from DQS	t_{QH}	1.75	—	2.05	—	2.6	—	ns
DD26	DQS output access time from SDCLK posedge	t_{DQSCK}	2	5	2	5.5	2	6.5	ns

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock)

4.7.6.1 Standard and Fast Mode Timing Parameters

Figure 47 depicts the standard and fast mode timings of HS-I^{2}C module, and Table 75 lists the timing characteristics.

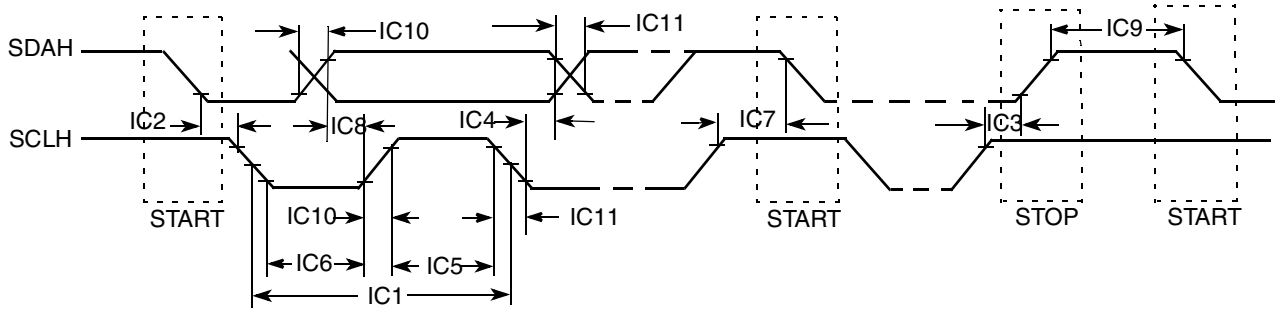


Figure 47. HS-I^{2}C Standard and Fast Mode Bus Timing

Table 75. HS-I^{2}C Timing Parameters—Standard and Fast Mode

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	SCLH cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of SCLH Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the SCLH Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both SDAH and SCLH signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both SDAH and SCLH signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	100	—	100	pF

1 A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC6) of the SCLH signal

3 A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement of Set-up time (ID No IC8) of 250 ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCLH signal.

If such a device does stretch the LOW period of the SCLH signal, it must output the next data bit to the SDAH line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLH line is released.

4 C_b = total capacitance of one bus line in pF.

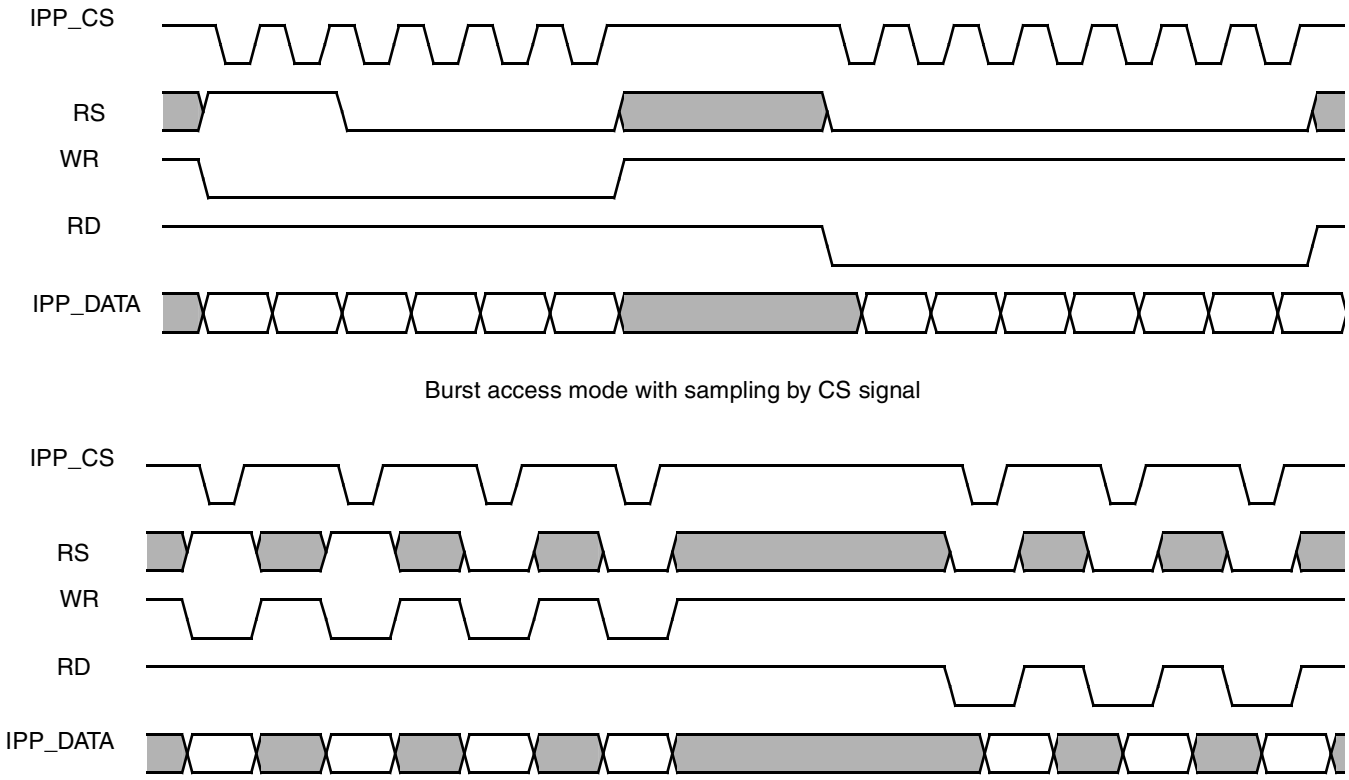


Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

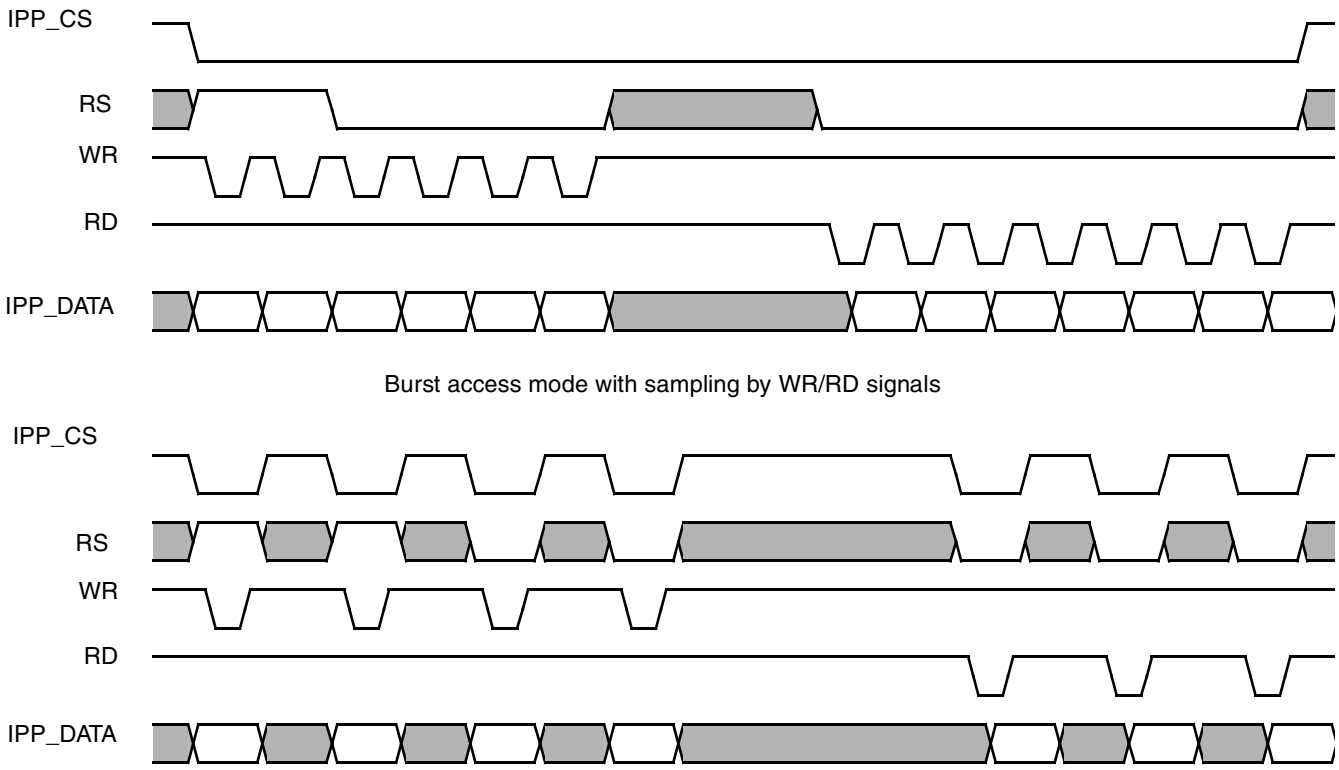


Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

[9]Display control up for read

$$Tdicur = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[10]Display control down for read

$$Tdicdrw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[11]Display control up for write

$$Tdicuw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[12]This parameter is a requirement to the display connected to the IPU

[13]Data read point

$$Tdrp = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_READ\_EN}{DI\_CLK\_PERIOD}\right]$$

Note: DISP#_READ_EN—operand of DC's MICROCDE READ command to sample incoming data

[14]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

4.7.8.8 Standard Serial Interfaces

The IPU supports the following types of asynchronous serial interfaces:

1. 3-wire (with bidirectional data line).
2. 4-wire (with separate data input and output lines).
3. 5-wire type 1 (with sampling RS by the serial clock).
4. 5-wire type 2 (with sampling RS by the chip select signal).

The IPU has four independent outputs and one input. The port can be configured to provide 3, 4, or 5-wire interfaces.

Figure 64 depicts the timing diagram of the 3-wire serial interface. The timing diagrams correspond to active-low IPP#_CS signal and the straight polarity of the IPP_CLK signal.

For this interface, a bidirectional data line is used outside the chip. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide

Figure 70 depicts Write 1 Sequence timing, Figure 71 depicts the Read Sequence timing, and Table 88 lists the timing parameters.

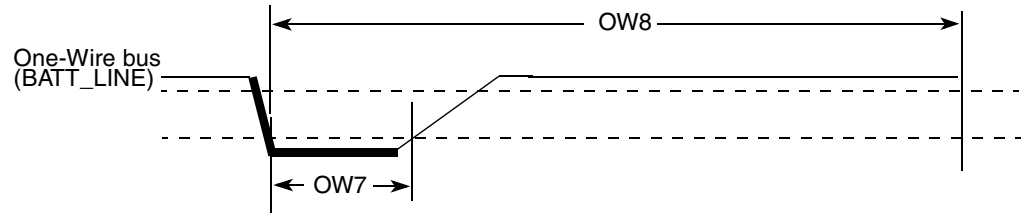


Figure 70. Write 1 Sequence Timing Diagram

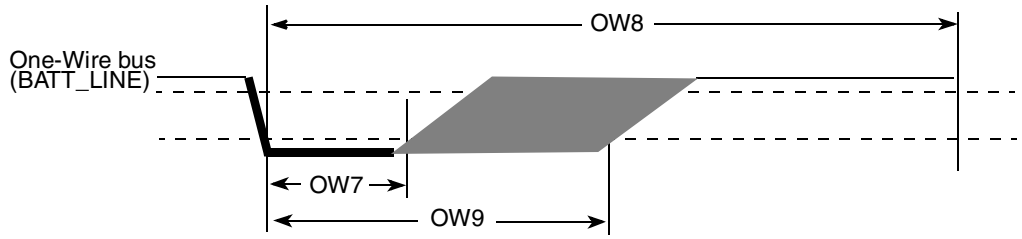


Figure 71. Read Sequence Timing Diagram

Table 88. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write /Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.7.10 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM.The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 75 shows timing for PIO write and Table 93 lists the timing parameters for PIO write.

Figure 75. Multi-word DMA (MDMA) Timing

Table 93. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 75	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)× T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

4.7.11.3 UDMA Output Timing

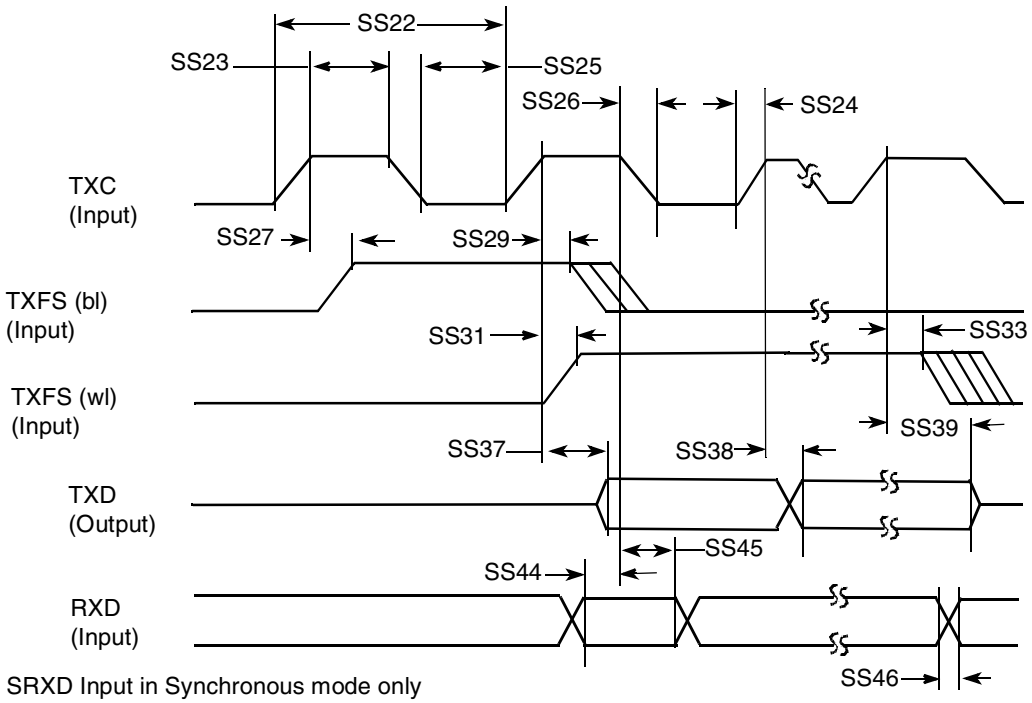
Figure 81 shows timing when the UDMA out transfer starts, Figure 82 shows timing when the UDMA out host terminates transfer, Figure 83 shows timing when the UDMA out device terminates transfer, and Table 96 lists the timing parameters for UDMA out burst.

Figure 81. UDMA Out Transfer Starts Timing Diagram

Figure 82. UDMA Out Host Terminates Transfer Timing Diagram

4.7.15.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter external clock timing and Table 104 lists the timing parameters for the SSI transmitter external clock.



Note: SRXD Input in Synchronous mode only

Figure 94. SSI Transmitter External Clock Timing Diagram

Table 104. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	30	ns

Table 125. USB PHY System Clocking Parameters (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Jitter (peak-peak)	<1.2 MHz	0	—	50	ps
Jitter (peak-peak)	>1.2 MHz	0	—	100	ps
Duty-cycle	—	40	—	60	%

4.7.19.4 USB PHY Voltage Thresholds

Table 126 lists the USB PHY voltage thresholds.

Table 126. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid	—	0.8	1.4	2.0	V
B-Device Session Valid	—	0.8	1.4	4.0	V
B-Device Session End	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V

[1] For VBUS maximum rating, see Table 11 on page 18

5 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 13 x 13 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power/reference ID (by ball grid location) for the 13 × 13 mm, 0.5 mm pitch package.

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_D0_CS	U21	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	AB23	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J18	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	Y22	NVCC_IPU2	GPIO	Output	High
DI1_PIN12	AA22	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	T20	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	H20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	G23	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	G22	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J21	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	J20	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	K18	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	H23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	N20	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	N21	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[3]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[3]	E21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[3]	F20	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[3]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[3]	G19	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[3]	E23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[3]	F21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[3]	G20	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[3]	H18	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	U22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[3]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[3]	H19	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[3]	F22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[3]	G21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	U23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	T22	NVCC_HS6	HSGPIO	Input	Keeper

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	05/2010	• Updated CaseTemperature Range column in Table 1, "Ordering Information," on page 3. • Changed the VREFOUT column in Table 3, "Special Signal Considerations," on page 12. • Added Section 3, “IOMUX Configuration for Boot Media”. • Updated Figure 2, "Power-Up Sequence," on page 24. • Updated the Minimum and Maximum columns in Table 13, "i.MX51 Operating Ranges," on page 19. • Added a note in Section 4.2.1, “Power-Up Sequence”. • Updated Section 4.2.1, “Power-Up Sequence.” • Changed the Input current (47 kΩ Pull-up) column in Table 21, "UHVIO DC Electrical Characteristics," on page 27 to Input current (75 kO Pull-up). • Added new table for parameters for DDR2 Pad output buffer Impedance. See Table 27, "DDR2 I/O Output Buffer Impedance HVE = 0," on page 32. • Added new section under Section 4.5, “I/O AC Parameters”. See Section 4.5.4, “AC Electrical Characteristics for DDR2”. • Updated Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. In the VIH (for square wave input) parameter, the minimum frequency was changed to NVCC_PER3 - 0.25V and the maximum frequency was changed to NVCC_PER3. • Added a note in Section 4.6.6, “NAND Flash Controller (NFC) Parameters” after Table 49. • Updated Asymmetric Mode Min, Symmetric Mode Min, and Max columns of Table 50. • Removed Conditions parameters of the Full scale output voltage row in Table 82. • Updated Section 4.7.11, “P-ATA Timing Parameters”. Replaced ATA/ATAPI-6 specification with ATA/ATAPI-5 specification. • In Table 102, "SSI Transmitter Timing with Internal Clock," on page 135, under the Synchronous Internal Clock Operation sections for the ID SS42, minimum frequency was changed from 10.0 to 30. • In Table 103, "SSI Receiver Timing with Internal Clock," on page 136, under the Internal Clock Operation section for ID SS20, minimum frequency was changed from 10.0 to 30. • In Table 104, "SSI Transmitter Timing with External Clock," on page 138, under the External Clock Operation section for ID SS38, maximum frequency was changed from 15.0 to 30. • Added a new section Section 4.7.16.1, “UART Electrical”, under Section 4.7.16, “UART”. • In Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148, for IDs SS28 and SS29, direction was changed from out to in. • In Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150, for IDs US40 and US41, direction was changed from out to in and the reference signal was changed to USB_VM1 and USB_VP1 respectively. • In Table 122, "USB Timing Specification for ULPI Parallel Mode," on page 151, added an extra row for ID17. • Updated Signal and Direction columns in Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150. • Updated Signal names in Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148.
Rev. 1	10/2009	Initial public release.