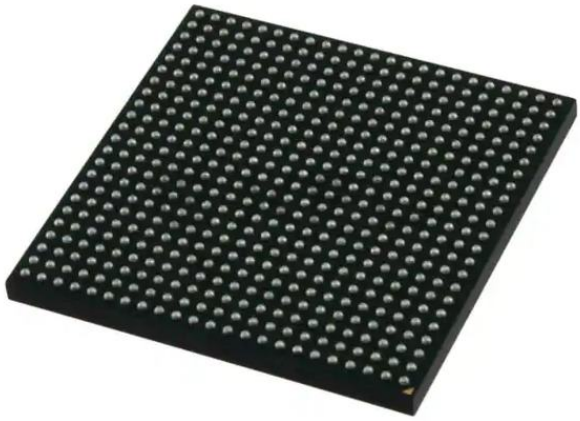

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 95°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx513cjm6cr2

Features include the following:

- **Smart Speed Technology**—The heart of the i.MX51 processors is a level of power management throughout the device that enables the rich suite of multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Smart Speed Technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than typical industry expectations.
- **Applications Processor**—The i.MX51 processors boost the capabilities of high-tier portable applications by providing for the ever-increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) allows the device run at much lower voltage and frequency with sufficient MIPS for tasks such as audio decode resulting in significant power reduction.
- **Multimedia Powerhouse**—The multimedia performance of the i.MX51 processors is boosted by a multi-level cache system and further enhanced by a Multi-Standard Hardware Video Codec, autonomous Image Processing Unit, SD and HD720p Triple Video (TV) Encoder with triple video DAC, Neon (including Advanced SIMD, 32-bit Single-Precision floating point support and Vector Floating Point co-processor), and a programmable smart DMA (SDMA) controller.
- **Powerful Graphics Acceleration**—Graphics is the key to mobile game navigation, web browsing, and other applications. The i.MX51 processors provide two independent, integrated Graphics Processing Units: OpenGL ES 2.0 3D graphics accelerator (27 Mtri/s, 166 Mpix/s) and OpenVG 1.1 2D graphics accelerator (166 Mpix/s).
- **Interface Flexibility**—The i.MX51 processor interface supports connection to all popular types of external memories: DDR2, Mobile DDR, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC), and OneNAND. Designers seeking to provide products that deliver a rich multimedia experience find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, High-Speed USB On-The-Go with PHY, and three High-Speed USB hosts, multiple expansion card ports (High-Speed MMC/SDIO Host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, I^2S serial audio, and SIM card, among others).
- **Increased Security**—Because the need for advanced security for mobile devices continues to increase, the i.MX51 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the MX51 security features contact your Freescale representative.

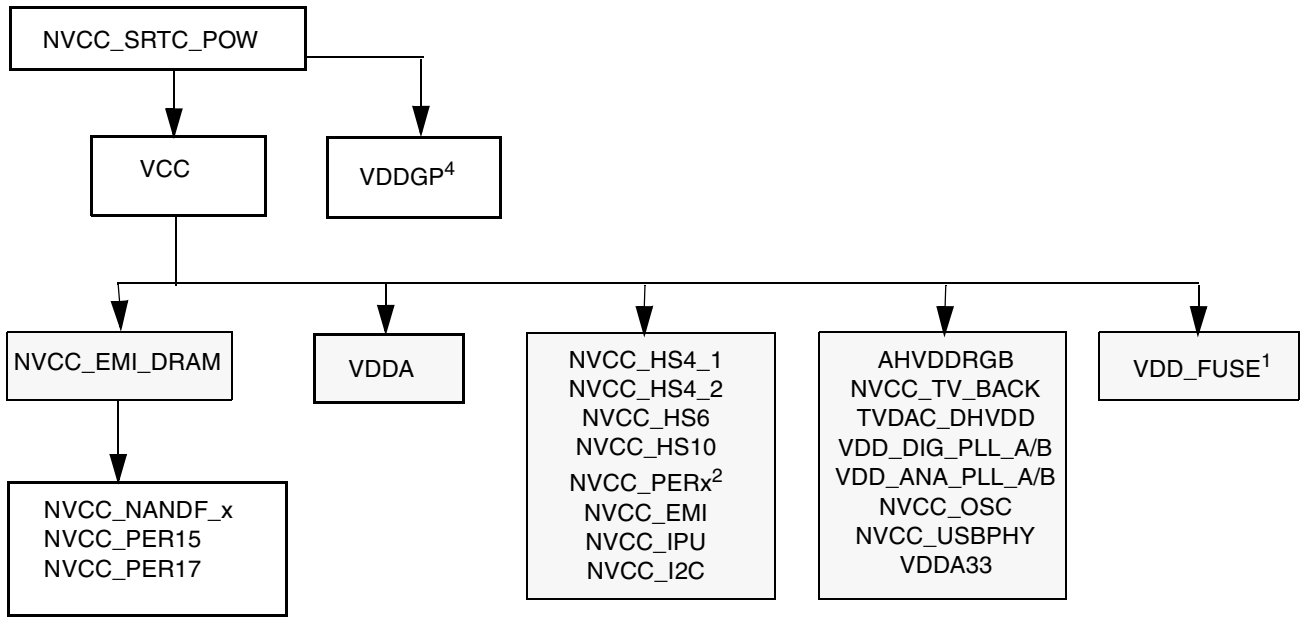
Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xD products (Consumer)	ARM core supply voltage $0 \leq f_{ARM} \leq 167$ MHz	0.8	0.85	1.15	V
	ARM core supply voltage $167 < f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VDDGP MCIMX51xC products (Industrial)	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.10	V
	ARM core supply voltage Stop mode	0.90	0.95	1.05	V
VCC MCIMX51xD products (Consumer)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage Low Performance Mode (LPM) The clock frequencies are derived from AXI and AHB buses at 44 MHz and a DDR clock rate of DDR Clock/3. DDR2 does not support frequencies below 125 MHz per JEDEC.	1.00	1.05	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VCC MCIMX51xC products (Industrial)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.90	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.



1. VDD_FUSE should only be powered when writing.
2. NVCC_PERx refers to NVCC_PER 3, 5, 8, 9, 10, 11, 12, 13, 14.
3. No power-up sequence dependencies exist between the supplies shown in the block diagram shaded in gray.
4. There is no requirement for VDDGP to be preceded by any other power supply other than NVCC_SRTC_POW.
5. If all of the UHVIO supplies (NVCC_NANDFx, NVCC_PER15 and NVCC_PER17) are less than 2.75 V then there is no requirement on the power up sequence order between NVCC_EMI_DRAM and the UHVIO supplies. However, if the voltage is 2.75 V and above, then NVCC_EMI_DRAM needs to power up before the UHVIO supplies as shown here.

Figure 2. Power-Up Sequence

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

For more information on power up, see i.MX51 Power-Up Sequence (AN4053).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO/HSGPIO)
- Double Data Rate 2 (DDR2)
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- High-Speed I^2C and I^2C
- Enhanced Secure Digital Host Controller (eSDHC)

Figure 6 depicts the load circuit for output pads for standard- and fast-mode. Figure 7 depicts the output pad transition time definition. Figure 8 depicts load circuit with external pull-up current source for HS-mode. Figure 9 depicts HS-mode timing definition.

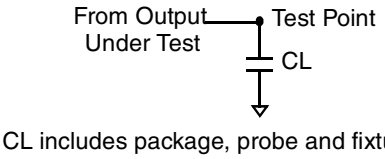


Figure 6. Load Circuit for Standard and Fast-Mode

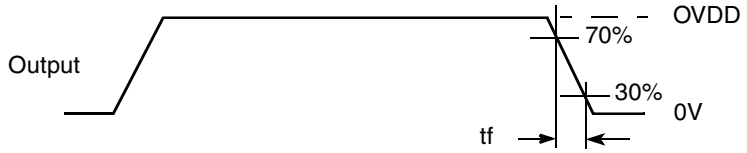
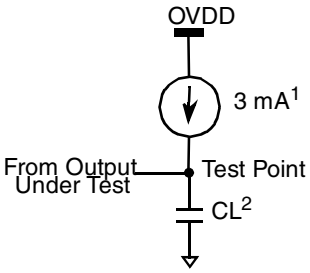


Figure 7. Definition of Timing for Standard and Fast-Mode



Notes:
[1]Load current when output is between 0.3×OVDD and 0.7×OVDD
[2]CL includes package, probe, and fixture capacitance.

Figure 8. Load Circuit for HS-Mode with External Pull-Up Current Source

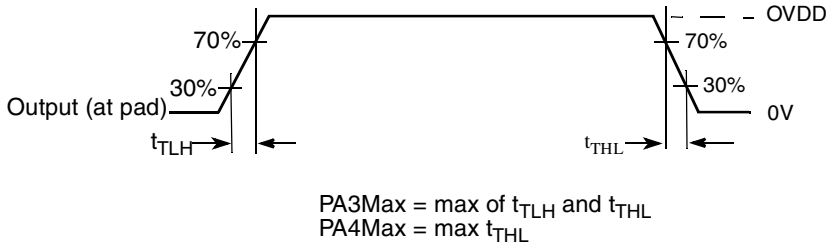


Figure 9. Definition of Timing for HS-Mode

Table 34. I^2C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	10/74	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	7/14	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	17	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	30	—	67	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	15	—	34	ns

Table 35. Low Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Medium drive)	tdit	—	—	—	22	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	11	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time greater than 25 ns

Table 36. High Voltage I^2C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	3/3 6/5	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	5/5 9/9	ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time > 25 ns

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

4.6 Module Timing

This section contains the timing and electrical parameters for the modules in the i.MX51 processor.

4.6.1 Reset Timings Parameters

Figure 12 shows the reset timing and Table 45 lists the timing parameters.

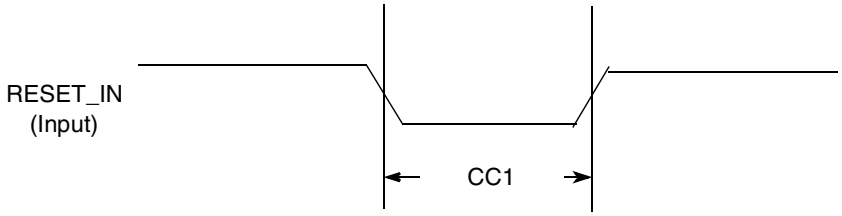


Figure 12. Reset Timing Diagram

Table 45. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN to be qualified as valid (input slope = 5 ns)	50	—	ns

Table 50. NFC—Timing Characteristics (continued)

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF21	WE high to RE low	tWHR	14T-5.45	14T-5.45	—
NF22	WE high to busy	tWB	—	—	6T

1 t_{DSR} is calculated by the following formula:
Asymmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} + {}^1/_2T - Tdl^2$
Symmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} - Tdl^2$
$t_{REpd} + t_{Dpd}$ = 11.2 ns (including clock skew)
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
t_{DSR} can be used to determine t_{REA} max parameter with the following formula: $t_{REA} = 1.5T - t_{DSR}$.

2 Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{aclk}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{aclk} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

3 NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4 NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^2 - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.7 External Interface Module (WEIM)

The following sections provide information on the WEIM.

4.6.7.1 WEIM Signal Cross Reference

Table 51 is a guide to help the user identify signals in the WEIM Chapter of the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) that are the same as those mentioned in this data sheet.

Table 51. WEIM Signal Cross Reference

Reference Manual WEIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUX Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA

Table 58. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}[1]	1.7	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

[1] These values are for command/address slew rates of 1 V/ns and SDCLK / SDCLK_B differential slew rate of 2 V/ns. For different values use the settings shown in Table 59.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 59. Derating Values for DDR2-400 (SDCLK = 200 MHz)

Command / Address Slew Rate (V/ns)	SDCLK Differential Slew Rates[1,2]						Unit
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	+0	+0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 61. Derating values for DDR2 Differential DQS[1,2]

Table 62. Derating values for DDR2 Single Ended DQS[3,4]

1. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
2. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).
3. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
4. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: display processing, image conversions, and other related functions.
- Synchronization and control capabilities such as avoidance of tearing artifacts.

4.7.8.1 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.1.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.1.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 50.

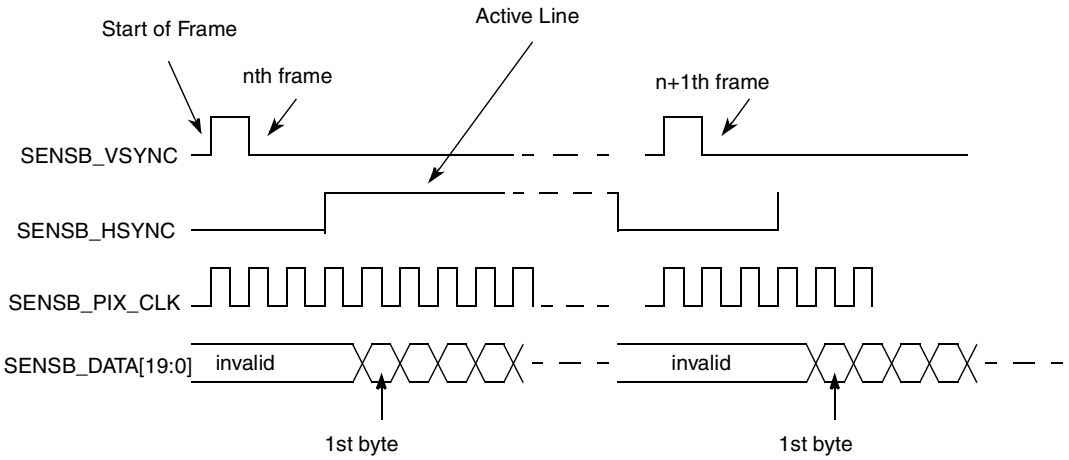


Figure 50. Gated Clock Mode Timing Diagram

Figure 62 shows timing of the parallel interface with IPP_WAIT control.

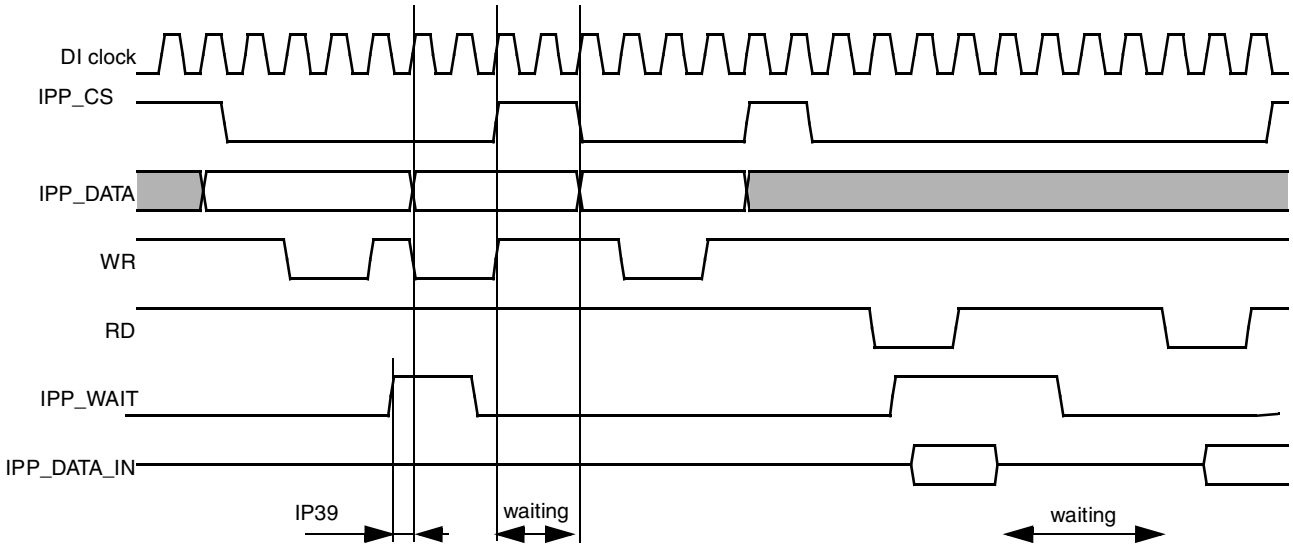


Figure 62. Parallel Interface Timing Diagram—Read Wait States

Figure 72 depicts the timing of the PWM, and Table 89 lists the PWM timing parameters.

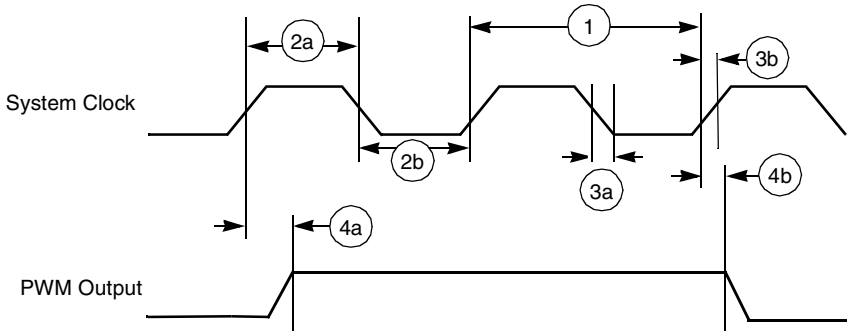


Figure 72. PWM Timing

Table 89. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.11 P-ATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-5 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 66 Mbyte/s. Parallel ATA module interface consist of a total of 29 pins, Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-5 specification and these requirements are configurable by the ATA module registers.

4.7.11.1 PIO Mode Read Timing

Figure 74 shows timing for PIO read and Table 92 lists the timing parameters for PIO read.

Figure 74. PIO Read Timing Diagram

Table 92. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 74	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)×T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

4.7.18 USB Parallel Interface Timing

Electrical and timing specifications of Parallel Interface are presented in the subsequent sections. Table 121 shows the signal definitions in parallel mode. Figure 108 shows the USB transmit/receive waveform in parallel mode. Table 122 shows the USB timing specification for ULPI parallel mode.

Table 121. Signal Definitions—Parallel Interface (Normal ULPI)

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to Clock.
USB_Data[7:0]	I/O	Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the Data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

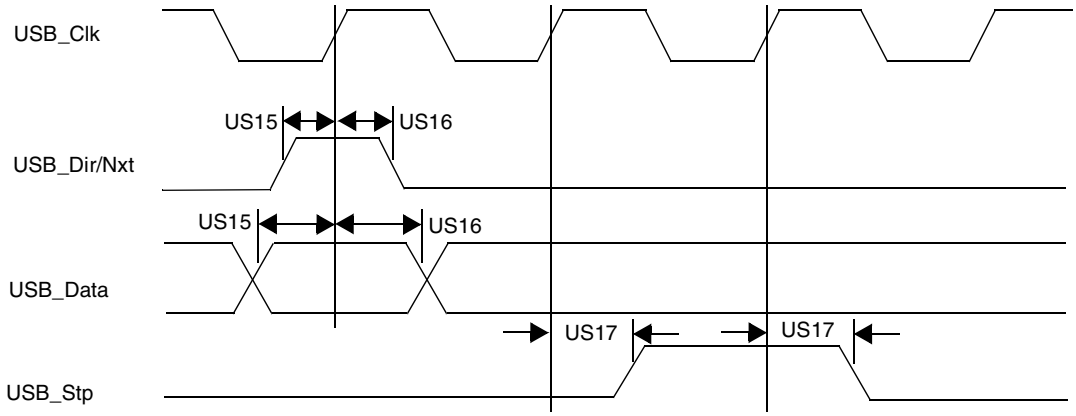


Figure 108. USB Transmit/Receive Waveform in Parallel Mode

Table 122. USB Timing Specification for ULPI Parallel Mode

ID	Parameter	Min	Max	Unit	Conditions/ Reference Signal
US15	Setup Time (Dir, Nxt in, Data in)	6	—	ns	10 pF
US16	Hold Time (Dir, Nxt in, Data in)	0	—	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H3 routed to DISP2 I/O[1] and H1	—	9	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H2	—	11	ns	10 pF

[1] H3 routed to NANDF I/O is recommended for Full and Low-Speed use only.

5.1.1 BGA—Case 2058 13 x 13 mm, 0.5 mm Pitch

Figure 109 shows the top view, bottom view, and side view of the 13 ×13 mm package.

Figure 109. Package: Case 2058—0.5 mm Pitch

5.1.1.1 13 x 13 mm Package Drawing Notes

The following notes apply to Figure 109.

1 All dimensions in millimeters.

2 Dimensioning and tolerancing per ASME Y14.5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5 Parallelism measurement shall exclude any effect of mark on top surface of package.

5.1.2 13 x 13 mm, 0.5 Pitch Ball Assignment Lists

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name. Table 128 displays an alpha-sorted list of the signal assignments. Table 129 provides a listing of the no-connect contacts.

5.1.2.1 13 x 13 mm Ball Contact Assignments

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
AHVDDRGB	V15, V16
AHVSSRGB	V13, V14
GND	A1, A24, A25, B1, B25, E7, E13, E16, E19, G5, J13, J14, K5, K13, K14, K15, L13, L14, L15, L21, M12, M13, M14, M15, N5, N6, N8, N9, N10, N11, P8, P9, P11, P21, R8, R9, R10, R11, R12, T8, T9, T10, T11, T12, T13, U5, U9, U10, U11, U12, U13, U21, W5, AA7, AA10, AA13, AA16, AA19, AD1, AD2, AD25, AE1, AE24, AE25
GND_ANA_PLL_A	AE3
GND_ANA_PLL_B	AC25
GND_DIG_PLL_A	AE2
GND_DIG_PLL_B	AD24
NGND_OSC	AC23
NGND_TV_BACK	AB22
NGND_USBPHY	L23
NVCC_EMI	U8, V8
NVCC_EMI_DRAM	L5, M5, R5, T5, Y5, AA5
NVCC_HS10	M20
NVCC_HS4_1	L20
NVCC_HS4_2	P20
NVCC_HS6	N20
NVCC_I2C	V11
NVCC_IPU2	V20
NVCC_IPU4	N16
NVCC_IPU5	K16
NVCC_IPU6	M16

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	H6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	D6	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	F6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	G6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	E3	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	A15	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AC18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	AE18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AC19	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	AB18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	Y24	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	AA25	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A18	NVCC_PER15	UHVIO	Output	—
SD1_CMD	C17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	B18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	D17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	D18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	C18	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	A19	NVCC_PER17	UHVIO	Output	—
SD2_CMD	F16	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	F18	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	A21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	F17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down
STR	D14	NVCC_PER12	—	—	—

Table 129. 13 x 13 mm No Connect Assignments (continued)

Ball Status	Ball Assignments
NC	H17
NC	H19
NC	H21
NC	J5
NC	J7
NC	J17
NC	J19
NC	J21
NC	K7
NC	K17
NC	K19
NC	K21
NC	L7
NC	L17
NC	L19
NC	M7
NC	M17
NC	M19
NC	M21
NC	N7
NC	N17
NC	N19
NC	N21
NC	P5
NC	P7
NC	P17
NC	P19
NC	R7
NC	R17
NC	R19
NC	R21
NC	T7
NC	T17

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper