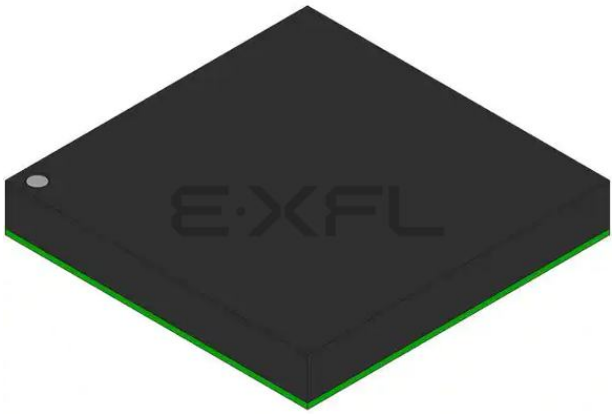

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx513djm8c

Table 29. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Low drive)	tdit	—	—	—	7	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.2 Fast I/O AC Parameters

Table 30 shows the fast I/O AC parameters.

Table 30. Fast I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.429/1.275 2.770/2.526	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.793/1.607 3.565/3.29	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.542/2.257 5.252/4.918	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.641/4.456 10.699/10.0	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.69/0.78 0.36/0.39	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.62 0.28/0.30	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	70	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	53	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.3 I^2C AC Parameters

NOTE

See the errata for HS-I^2C in the i.MX51 Chip Errata document. The two standard I^2C modules have no errata

Figure 6 depicts the load circuit for output pads for standard- and fast-mode. Figure 7 depicts the output pad transition time definition. Figure 8 depicts load circuit with external pull-up current source for HS-mode. Figure 9 depicts HS-mode timing definition.

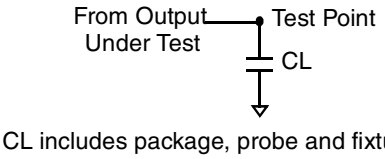


Figure 6. Load Circuit for Standard and Fast-Mode

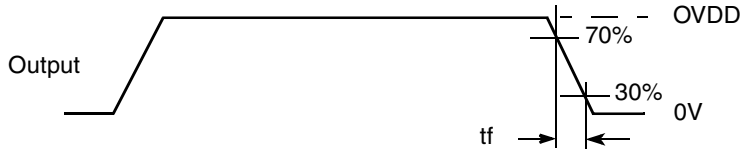
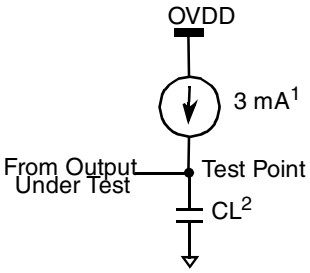


Figure 7. Definition of Timing for Standard and Fast-Mode



Notes:
[1]Load current when output is between 0.3×OVDD and 0.7×OVDD
[2]CL includes package, probe, and fixture capacitance.

Figure 8. Load Circuit for HS-Mode with External Pull-Up Current Source

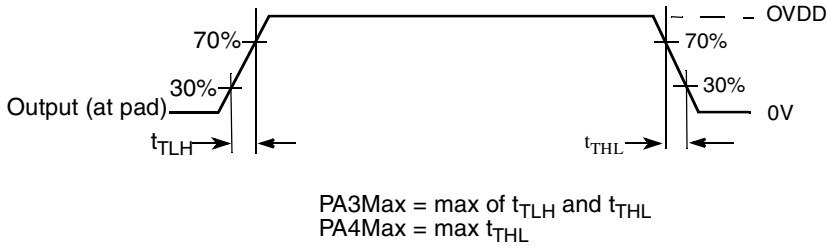


Figure 9. Definition of Timing for HS-Mode

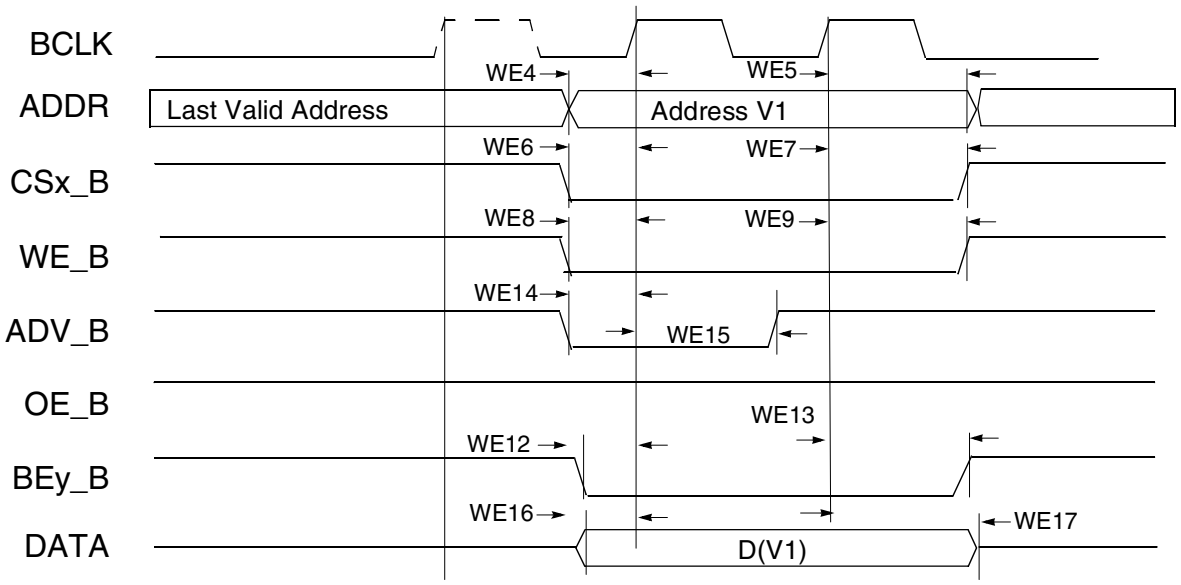


Figure 23. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

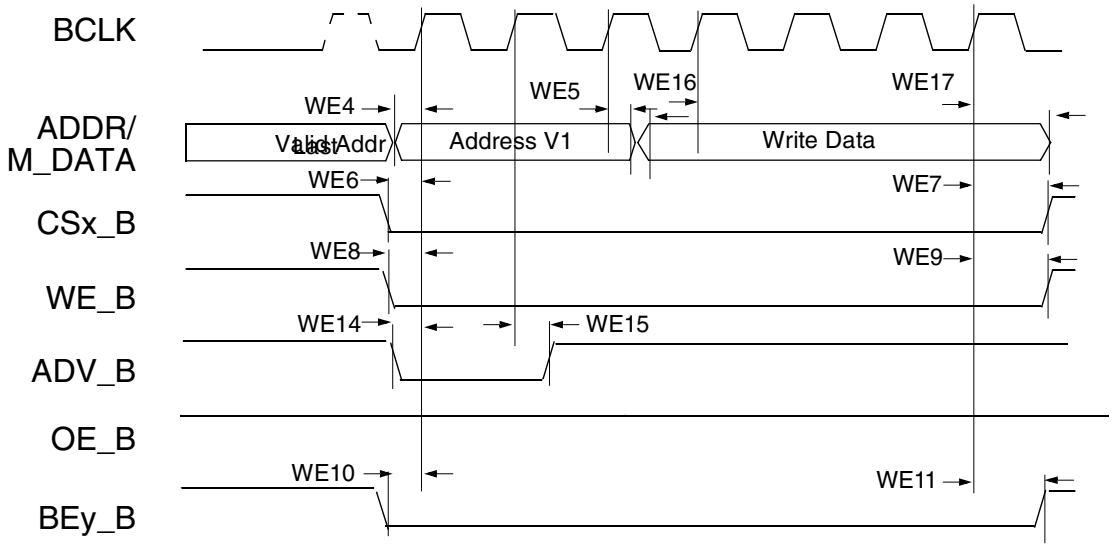


Figure 24. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 53.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

Table 58. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}[1]	1.7	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

[1] These values are for command/address slew rates of 1 V/ns and SDCLK / SDCLK_B differential slew rate of 2 V/ns. For different values use the settings shown in Table 59.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 59. Derating Values for DDR2-400 (SDCLK = 200 MHz)

Command / Address Slew Rate (V/ns)	SDCLK Differential Slew Rates[1,2]						Unit
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	+0	+0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 61. Derating values for DDR2 Differential DQS[1,2]

Table 62. Derating values for DDR2 Single Ended DQS[3,4]

1. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
2. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).
3. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
4. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

Table 85. Asynchronous Serial Interface Timing Characteristics (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]-Tdicur-1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5	—	Tdicpr-Tdicdr-1.5	ns
IP60	Write data setup time	Tds	Tdicdw-1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns
IP69	Clock offset[11]	Toclk	Toclk-1.5	Toclk	Toclk+1.5	ns
IP70	RS up time[12]	Tdicurs	Tdicurs–1.5	Tdicurs	Tdicurs+1.5	ns
IP71	RS down time[13]	Tdicdrs	Tdicdrs -1.5	Tdicdrs	Tdicdrs+1.5	ns
IP72	CS up time[14]	Tdicucs	Tdicucs –1.5	Tdicucs	Tdicucs+1.5	ns
IP73	CS down time[15]	Tdicdcs	Tdicdcs –1.5	Tdicdcs	Tdicdcs+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display interface clock period value for read

$$Tdicpr = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{DI\_CLK\_PERIOD}\right]$$

[3]Display interface clock period value for write

$$Tdicpw = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{DI\_CLK\_PERIOD}\right]$$

Table 90 and Figure 73 define the AC characteristics of all the P-ATA interface signals on all data transfer modes.

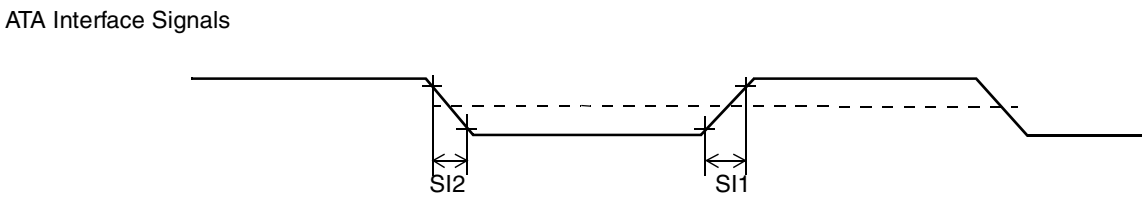


Figure 73. P-ATA Interface Signals Timing Diagram

Table 90. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface.[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface (see note)	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user needs to use level shifters for 5.0 V compatibility on the ATA interface. The i.MX51 P-ATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-4) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX51 P-ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

4.7.13 SCAN JTAG Controller (SJC) Timing Parameters

Figure 88 depicts the SJC test clock input timing. Figure 89 depicts the SJC boundary scan timing. Figure 91 depicts the TRST timing with respect to TCK. Figure 90 depicts the SJC test access port. Signal parameters are listed in Table 99.

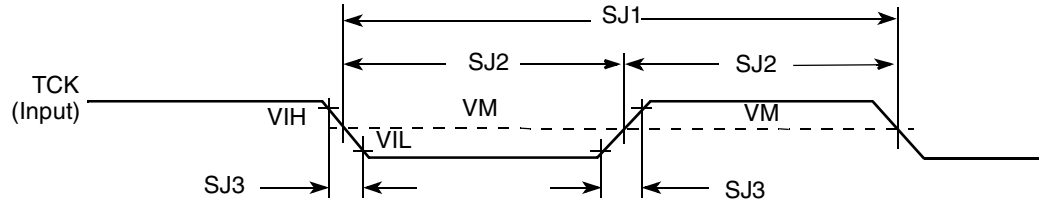


Figure 88. Test Clock Input Timing Diagram

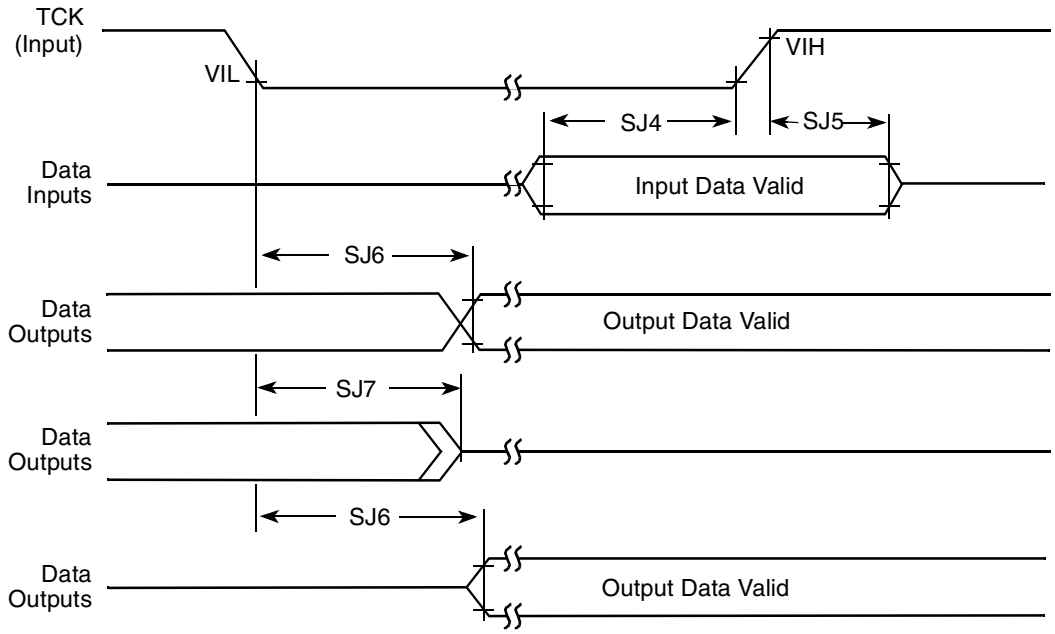


Figure 89. Boundary Scan (JTAG) Timing Diagram

4.7.15.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver internal clock timing and Table 103 lists the timing parameters for the SSI receiver internal clock.

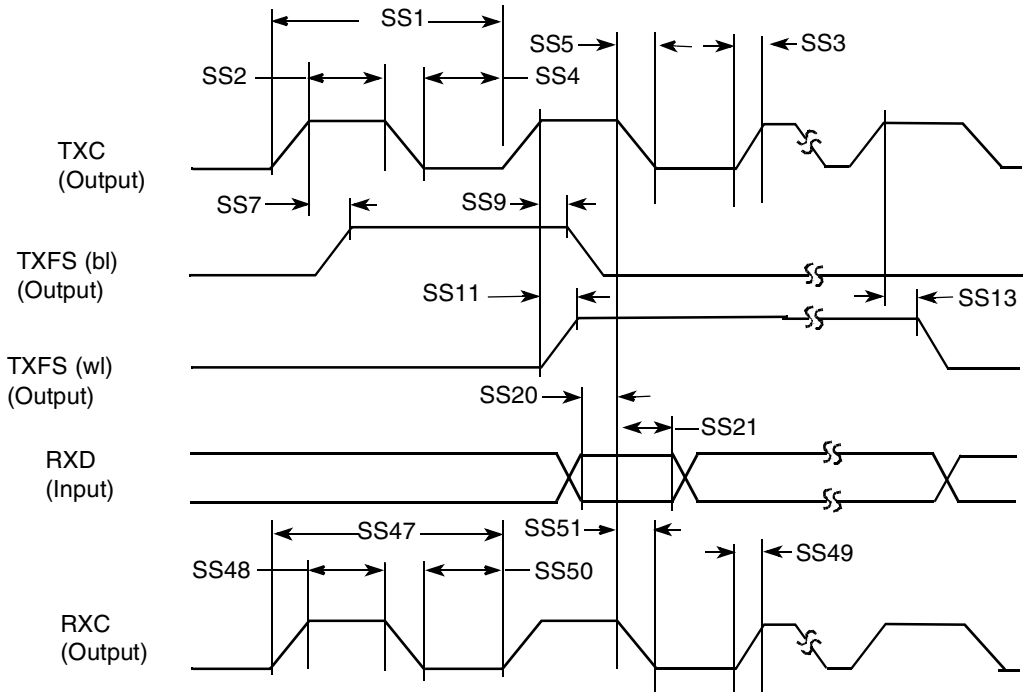


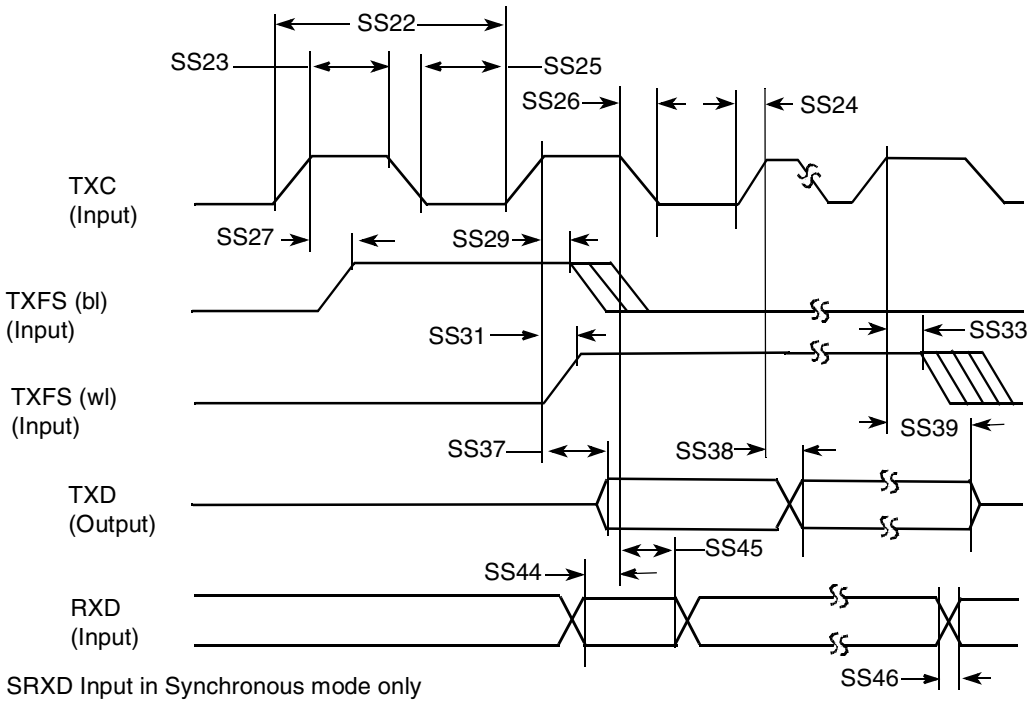
Figure 93. SSI Receiver Internal Clock Timing Diagram

Table 103. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	30	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns

4.7.15.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter external clock timing and Table 104 lists the timing parameters for the SSI transmitter external clock.



Note: SRXD Input in Synchronous mode only

Figure 94. SSI Transmitter External Clock Timing Diagram

Table 104. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	30	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16 UART

Table 106 shows the UART I/O configuration based on which mode is enabled.

Table 106. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.7.16.1 UART Electrical

This section describes the electrical information of the UART module.

Table 114. Definitions of USB Receive Waveform in DAT_SE0 Bi-Directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions/ Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 USB DAT_SE0 Unidirectional Mode

Table 115 shows the signal definitions in DAT_SE0 unidirectional mode

Table 115. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential RX data when USB_TXOE_B is high

Figure 102 and Figure 103 shows the USB transmit/receive waveform in DAT_SE0 uni-directional mode respectively.

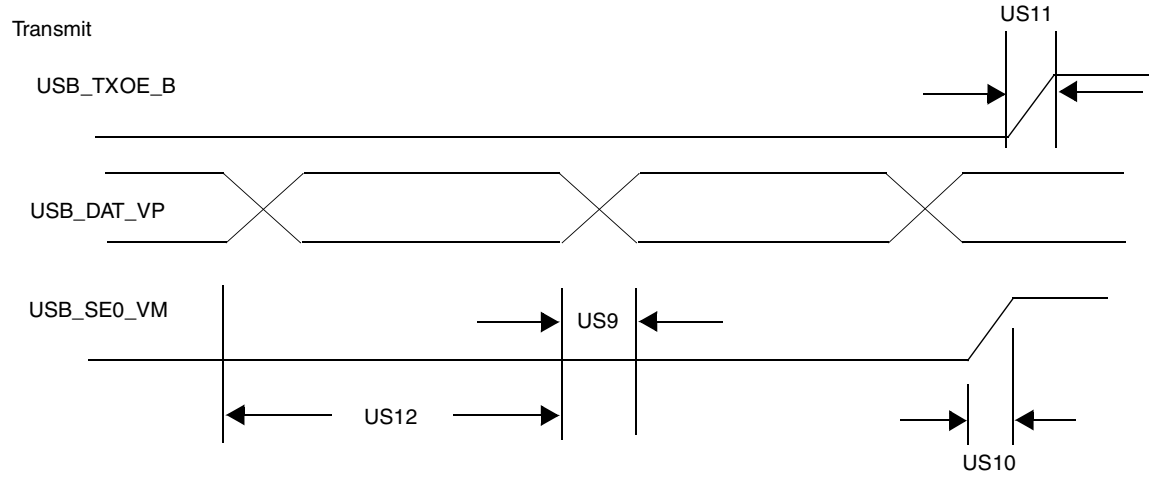


Figure 102. USB Transmit Waveform in DAT_SE0 Uni-directional Mode

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_IPU7	H22
NVCC_IPU8	V22
NVCC_IPU9	L16
NVCC_NANDF_A	J8
NVCC_NANDF_B	H8
NVCC_NANDF_C	H9
NVCC_OSC	AD22
NVCC_PER10	H12
NVCC_PER11	H11
NVCC_PER12	H15
NVCC_PER13	H14
NVCC_PER14	V9
NVCC_PER15	H16
NVCC_PER17	J16
NVCC_PER3	V10
NVCC_PER5	D20
NVCC_PER8	J15
NVCC_PER9	H10
NVCC_SRTC_POW	V12
NVCC_TV_BACK	AC22
NVCC_USBPHY	P16
RREFEXT	K18
SGND	P10
SVCC	N13
SVDDGP	M11
TVDAC_DHVDD	AB21
VBUS	L22
VCC	N12, N14, N15, P12, P13, P14, P15, R13, R14, R15, T14, T15, T16, U14, U15, U16
VDD_ANA_PLL_A	AD4
VDD_ANA_PLL_B	AC24
VDD_DIG_PLL_A	AD3
VDD_DIG_PLL_B	AB23
VDD_FUSE	P6

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
KEY_COL2	D16	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_COL3[4]	A16	NVCC_PER13	GPIO	Output	High
KEY_COL4[4]	B17	NVCC_PER13	GPIO	Output	Low
KEY_COL5[4]	A17	NVCC_PER13	GPIO	Output	Low
KEY_ROW0	B15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW1	C15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW2	F15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW3	D15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
NANDF_ALE	E1	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CLE	E2	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS0	D4	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS1	D1	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS2	D5	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS3	B2	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS4	B3	NVCC_NANDF_A	UHVIO	Output	Low
NANDF_CS5	C4	NVCC_NANDF_A	UHVIO	Output	Low
NANDF_CS6	A2	NVCC_NANDF_B	UHVIO	Output	Low
NANDF_CS7	F7	NVCC_NANDF_B	UHVIO	Output	Low
NANDF_D0	D7	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D1	F9	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D10	C5	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D11	B4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D12	A3	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D13	F10	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D14	E4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D15	J6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D2	C6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D3	B5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D4	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D5	F8	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	A6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	A5	NVCC_NANDF_B	UHVIO	Input	Keeper

Table 129. 13 x 13 mm No Connect Assignments (continued)

Ball Status	Ball Assignments
NC	T19
NC	T21
NC	U7
NC	U17
NC	U19
NC	V5
NC	V7
NC	V19
NC	V21
NC	W7
NC	W8
NC	W9
NC	W10
NC	W11
NC	W12
NC	W13
NC	W14
NC	W15
NC	W16
NC	W17
NC	W18
NC	W19
NC	W21
NC	Y21
NC	AA6
NC	AA8
NC	AA9
NC	AA11
NC	AA12
NC	AA14
NC	AA15
NC	AA17
NC	AA18

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_D0_CS	U21	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	AB23	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J18	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	Y22	NVCC_IPU2	GPIO	Output	High
DI1_PIN12	AA22	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	T20	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	H20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	G23	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	G22	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J21	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	J20	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	K18	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	H23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	N20	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	N21	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[3]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[3]	E21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[3]	F20	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[3]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[3]	G19	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[3]	E23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[3]	F21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[3]	G20	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[3]	H18	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	U22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[3]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[3]	H19	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[3]	F22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[3]	G21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	U23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	T22	NVCC_HS6	HSGPIO	Input	Keeper

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper

5.3 13 × 13 mm, 0.5 Pitch Ball Map

Table 133 shows the 13 x 13 mm, 0.5 pitch ball map.

Table 133. 13 × 13 mm, 0.5 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	GND	NANDF_CS6	NANDF_D12	NANDF_D8	NANDF_D7	NANDF_D6	CSI2_D18	CSPI1_RDY	USBH1_DATA2	USBH1_DATA1	USBH1_STP	UART1_TXD	UART2_RXD	UART3_TXD	OWIRE_LINE	KEY_COL3	KEY_COL5	SD1_CLK	SD2_CLK	CSI1_D8	SD2_DATA2	GPIO1_3	GPIO1_7	GND	GND	A
B	GND	NANDF_CS3	NANDF_CS4	NANDF_D11	NANDF_D3	NANDF_D4	AUD3_BB_TXD	AUD3_BB_RXD	USBH1_DATA4	USBH1_DIR	USBH1_DATA0	USBH1_DATA7	UART1_CTS	UART3_RXD	KEY_ROW0	KEY_COL0	KEY_COL4	SD1_DATA0	CSI1_VSYNC	CSI1_D9	SD2_DATA1	GPIO1_4	GPIO1_2	GPIO1_6	GND	B
C	NANDF_RB1	NANDF_RB3	GPIO_NAND	NANDF_CS5	NANDF_D10	NANDF_D2	CSI2_D19	AUD3_BB_FS	AUD3_BB_CK	USBH1_DATA3	USBH1_CLK	USBH1_DATA6	UART1_RTS	UART2_TXD	KEY_ROW1	KEY_COL1	SD1_CMD	SD1_DATA3	CSI1_HSYNC	NVCC_PER5	GPIO1_1	GPIO1_5	DISP1_DAT8	GPIO1_8	GPIO1_9	C
D	NANDF_CS1	NANDF_RB0	NANDF_RB2	NANDF_CS0	NANDF_CS2	NANDF_RDY_INT	NANDF_D0	CSI2_D13	CSPI1_MOSI	CSPI1_SS0	CSPI1_SCLK	USBH1_NXT	UART1_RXD	STR	KEY_ROW3	KEY_COL2	SD1_DATA1	SD1_DATA2	CSI1_PIXCLK	CSI2_PIXCLK	DISP1_DAT14	DISP1_DAT9	DISP1_DAT7	DISP1_DAT6	D
E	NANDF_ALE	NANDF_CLE	NANDF_WP_B	NANDF_D14	—	—	GND	—	—	VDDGP	—	—	GND	—	—	GND	—	—	GND	—	DISP1_DAT12	DISP1_DAT13	DISP1_DAT10	DISP1_DAT11	E
F	DRAM_D31	DRAM_D16	DRAM_D17	DRAM_D19	—	NANDF_RE_B	NANDF_CS7	NANDF_D5	NANDF_D1	NANDF_D13	CSI2_D12	CSPI1_MISO	CSPI1_SS1	USBH1_DATA5	KEY_ROW2	SD2_CMD	SD2_DATA3	SD2_DATA0	CSI1_MCLK	DI1_GP1	—	DISP1_DAT15	DISP1_DAT16	DISP1_DAT17	DISP1_DAT21	F
G	DRAM_D29	DRAM_D30	DRAM_D18	DRAM_D21	GND	NANDF_WE_B	—	—	—	—	—	—	—	—	—	—	—	—	—	DI1_PIN15	—	DISP1_DAT19	DISP1_DAT18	DISP1_DAT22	DISP1_DAT20	G
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 4	08/2010	• Updated Case Temperature Range column of Table 1, "Ordering Information," on page 3. • Updated Table 13, "i.MX51 Operating Ranges," on page 19 to include separate specification for case temperature for industrial parts. • Removed table footnote in Table 16, "i.MX51 Stop Mode Current and Power Consumption," on page 21. • Removed table footnote in Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. • Updated Table 52, "WEIM Interface Pinout in Various Configurations," on page 55.
Rev. 3	06/2010	• Updated Max column of Table 15, "Fuse Supply Current," on page 21. Deleted eFuse Read Current row from the same table. • Updated Symbol, Test Conditions, and Max columns of Table 18, "GPIO/HSGPIO DC Electrical Characteristics," on page 25. • Updated Max and Unit columns of Table 19, "DDR2 I/O DC Electrical Parameters," on page 26. • Updated Test Conditions, Max, and Unit columns of Table 20, "LVIO DC Electrical Characteristics," on page 26 • Updated Symbol, Test Conditions, Max, and Unit columns of Table 21, "UHVIO DC Electrical Characteristics," on page 27. • Updated Max and Unit columns of Table 22, "I2C Standard/Fast/High-Speed Mode Electrical Parameters for Low/Medium Drive Strength," on page 29. • Added a new table Table 25, "I/O Leakage Current," on page 31.