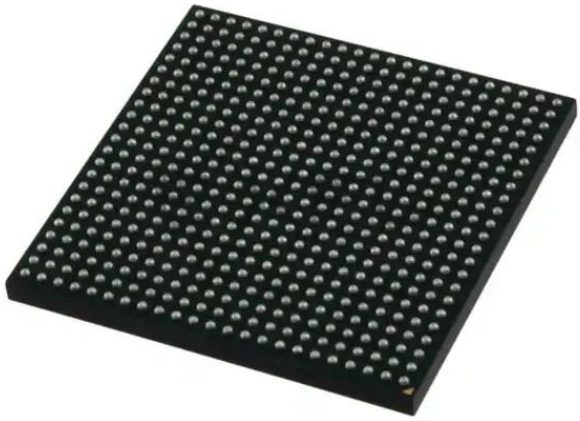

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx513djm8cr2

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_INT_REQ	When using the MC13892 power management IC, the PMIC_INT_REQ high-priority interrupt input on i.MX51 should be either floated or tied to NVCC_SRTC_POW with a 4.7 kΩ to 68 kΩ resistor. This avoids a continuous current drain on the real-time clock backup battery due to a 100 kΩ on-chip pull-up resistor. PMIC_INT_REQ is not used by the Freescale BSP (board support package) software. The BSP requires that the general-purpose INT output from the MC13892 be connected to the i.MX51 GPIO input GPIO1_8 configured to cause an interrupt that is not high-priority. The original intent was for PMIC_INT_REQ to be connected to a circuit that detects when the battery is almost depleted. In this case, the I/O must be configured as alternate mode 0 (ALT0 = power fail).
POR_B	This cold reset negative logic input resets all modules and logic in the IC. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Memory repair – Configuration of memory repair per fuse settings • Cold reset logic of WDOG – Some WDOG logic is only reset by POR_B. See WDOG chapter in *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details.
RREFEXT	Determines the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required.
SGND, SVCC, and SVDDGP	These sense lines provide the ability to sense actual on-chip voltage levels on their respective supplies. SGND monitors differentials of the on-chip ground versus an external power source. SVCC monitors on-chip VCC, and SVDDGP monitors VDDGP. Freescale recommends connection of the SVCC and SVDDGP signals to the feedback inputs of switching power-supplies or to test points.
STR	This signal is reserved for Freescale manufacturing use. The user should float this signal.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. AC electrical characteristics for slow and fast I/O are presented in the Table 29 and Table 30, respectively.

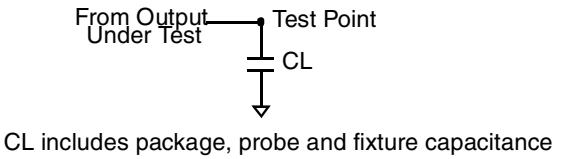

Figure 4. Load Circuit for Output

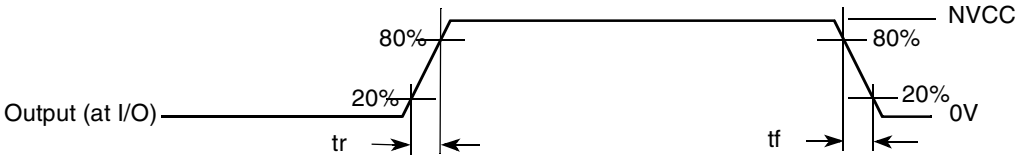

Figure 5. Output Transition Time Waveform

4.5.1 Slow I/O AC Parameters

Table 29 shows the slow I/O AC parameters.

Table 29. Slow I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.98/1.52 3.08/2.69	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.31/1.838 3.8/2.4	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.92/2.43 5.37/4.99	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.93/4.53 10.55/9.79	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	mA/ns

[1] Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5 = 000000.

[2] Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

[3] Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 40.

Table 40. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.43 3.03/2.92	1.20/1.27 2.39/2.38	1.43/1.49 2.35/2.46	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.04/2.04 4.51/4.49	1.68/1.74 3.47/3.50	1.82/1.91 3.16/3.30	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.08/3.93 9.06/8.93	3.16/3.19 6.92/6.93	2.90/3.01 5.74/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.00/2.17 3.15/3.42	2.33/2.50 3.24/3.52	3.70/3.70 4.63/4.75	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.47/2.68 4.2/4.53	2.72/2.92 4.01/4.37	4.10/4.16 5.33/5.55	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.87/4.18 7.32/7.86	3.78/4.10 6.35/6.90	5.13/5.30 7.25/7.73	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.49	0.69/0.66 0.42/0.40	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.70/0.62 0.31/0.31	0.54/0.52 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt		47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 44.

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.42 3.01/2.96	1.20/1.27 2.38/2.40	1.43/1.49 2.37/2.44	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.05/2.04 4.50/4.42	1.67/1.71 3.48/3.52	1.82/1.87 3.16/3.28	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.06/3.98 8.94/8.86	3.15/3.17 6.92/6.93	2.92/ 3.02 5.69/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.07/2.23 3.21/3.48	2.46/2.62 3.35/3.63	3.92/3.93 4.84/4.97	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.53/2.74 4.26/4.58	2.83/3.04 4.12/4.49	4.32/4.35 5.55/5.76	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.93/4.23 7.38/7.91	3.89/4.21 6.43/7.01	5.37/5.51 7.45/7.94	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.45	0.69/0.66 0.42/0.41	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.65/0.63 0.31/0.31	0.54/0.53 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.29 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16 - 40 pF) and there is max drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock ("enfc_clk" at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider. Table 49 demonstrates few examples for clock frequency settings.

Table 49. NFC Clock Settings Examples

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T—Clock Period (ns)[1]
133 (max value)	5 (reset value)	26.6	38
133	4	33.25	31
133	3	44.33	23

[1] Rounded up to whole nanoseconds.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low the actual data bus capturing might occur after the specified trhoh (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (T = 39 ns) guarantees proper operation for devices having trhoh > 15 ns. It is also recommended to set the NFC_FREQ_SEL Fuse accordingly to initiate the boot with 33.33 MHz clock.

Lower frequency operation can be supported for most available devices in the market, relying on data lines Bus-Keeper logic. This depends on device behavior on the data bus in the time interval between data output valid to data output high-Z state. In NAND device parameters this period is marked between trhoh and trhz (RE_B high to output high-Z). In most devices, the data transition from valid value to high-Z occurs without going through other states. Setting the data bus pads to Bus-Keeper mode in the IOMUX registers, keeps the data bus valid internally after the specified hold time, allowing proper capturing with slower clock.

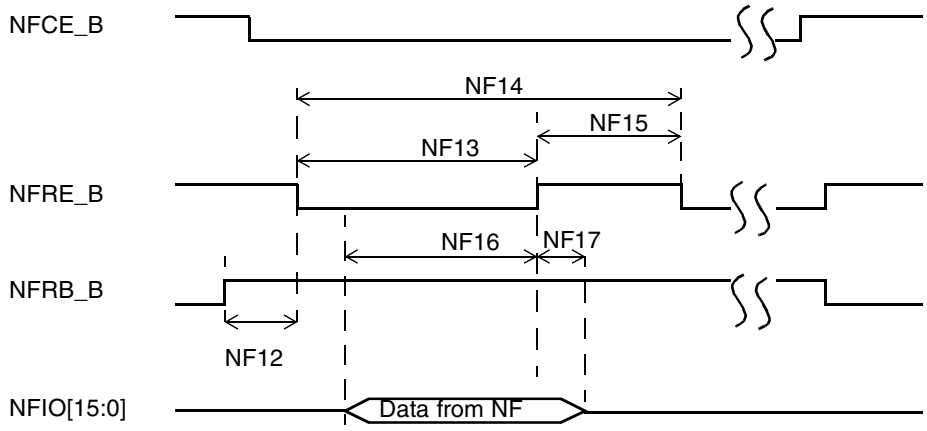

Figure 17. Read Data Latch Timing—Asymmetric Mode

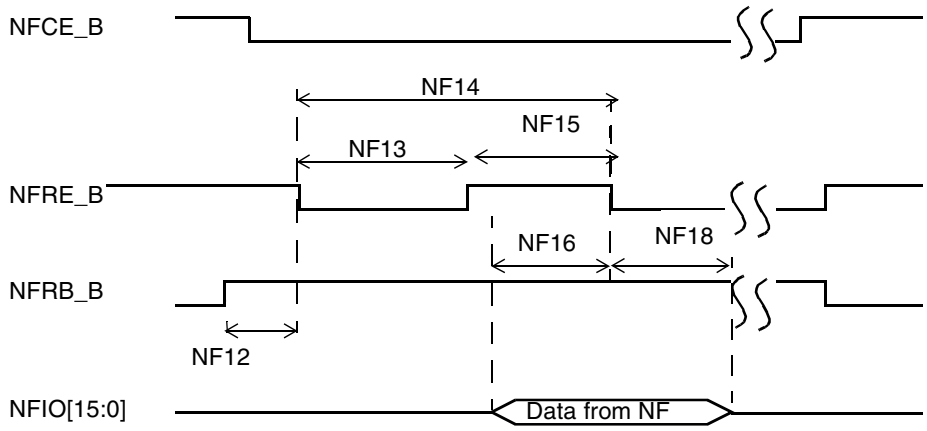

Figure 18. Read Data Latch Timing—Symmetric Mode

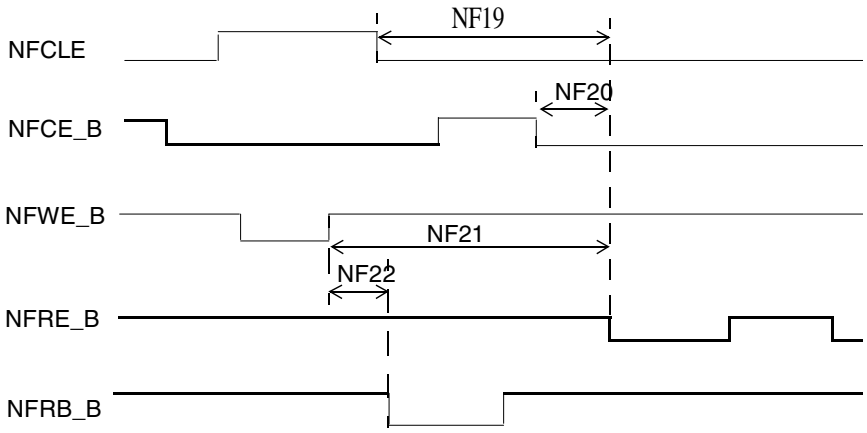

Figure 19. Other Timing Parameters

Table 50. NFC—Timing Characteristics

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF1	NFCLE setup Time	tCLS	2T-1	2T-1	—
NF2	NFCLE Hold Time	tCLH	T-4.45	T-4.45	—
NF3	NFCE_B Setup Time	tCS	2T-1	T-1	—
NF4	NFCE_B Hold Time	tCH	2T-5.55	0.5T-5.55	—
NF5	NFWE_B Pulse Width	tWP	T-2.5	0.5T-1.5	—
NF6	NFALE Setup Time	tALS	2T-2.7	2T-2.7	—
NF7	NFALE Hold Time	tALH	T-4.45	T-4.45	—
NF8	Data Setup Time	tDS	T-2.25	0.5T-2.25	—
NF9	Data Hold Time	tDH	T-6.55	0.5T-5.55	—
NF10	Write Cycle Time	tWC	2T	T	—
NF11	NFWE_B Hold Time	tWH	T-1.25	0.5T-1.25	—
NF12	Ready to NFRE_B Low	tRR	9T	9T	—
NF13	NFRE_B Pulse Width	tRP	1.5T-2.7	0.5T	—
NF14	READ Cycle Time	tRC	2T	T	—
NF15	NFRE_B High Hold Time	tREH	0.5T-1.5	0.5T-1.5	—
NF16[1]	Data Setup on READ	tDSR	11.2+0.5T-Tdl[2]	11.2-Tdl[2]	—
NF17[3]	Data Hold on READ	tDHR	0	—	$2T_{aclk}$+T
NF18[4]	Data Hold on READ	tDHR	—	Tdl[2]	$2T_{aclk}$+T
NF19	CLE to RE delay	tCLR	13T	13T	—
NF20	CE to RE delay	tCRE	T-3.45	1.5T-3.45	—

4.6.8 SDRAM Controller Timing Parameters

4.6.8.1 Mobile DDR SDRAM Timing Parameters

Figure 32 shows the basic timing parameters for mobile DDR (mDDR) SDRAM. The timing parameters for this diagram is shown in Table 55.

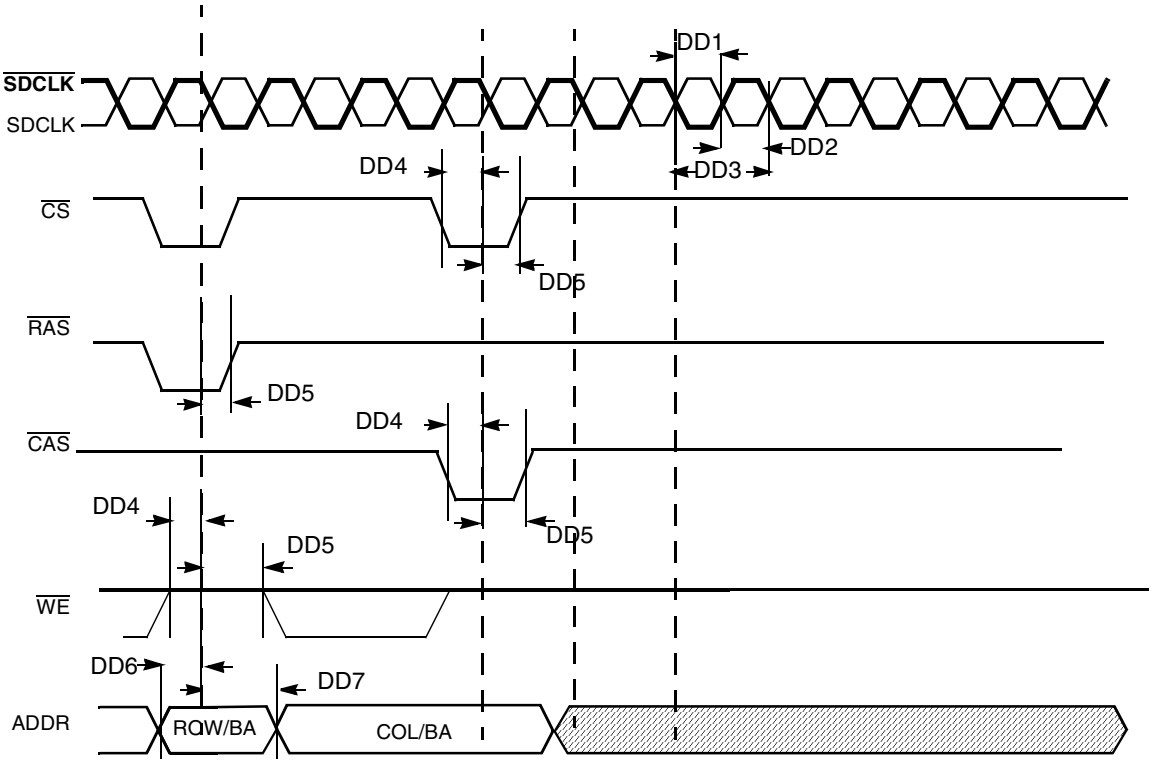

Figure 32. mDDR SDRAM Basic Timing Parameters

Table 55. mDDR SDRAM Timing Parameter Table

ID	Parameter	Symbol	200 MHz		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD1	SDRAM clock high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD2	SDRAM clock low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD3	SDRAM clock cycle time	t_{CK}	5	—	6	—	7.5	—	ns
DD4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns
DD6	Address output setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD7	Address output hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns

[1] This parameter is affected by pad timing. if the slew rate is < 1 V/ns, 0.2 ns should be added to the value. For cmos65 pads this is true for medium and low drive strengths.

Figure 34 shows the timing diagram for mDDR SDRAM DQ versus DQS and SDCLK read cycle. The timing parameters for this diagram is shown in Table 57.

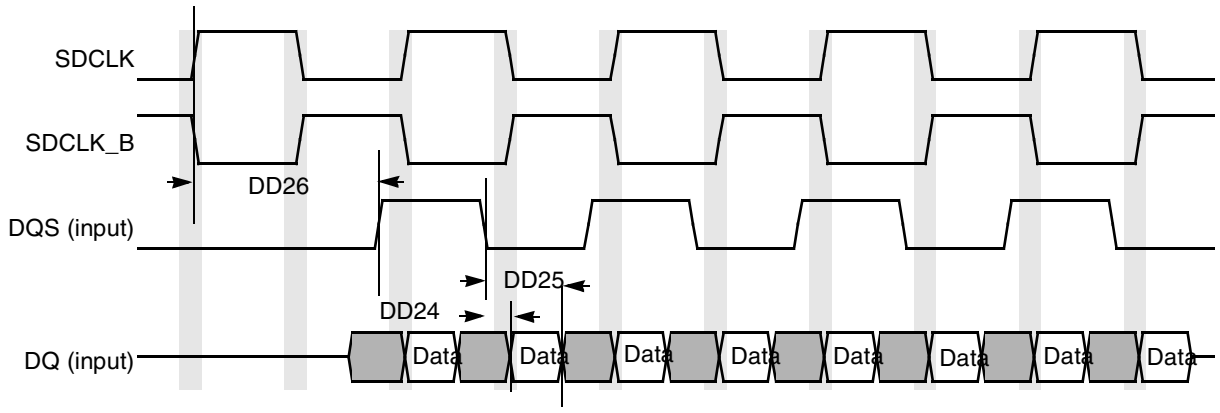

Figure 34. mDDR SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 57. mDDR SDRAM Read Cycle Parameter Table[1]

ID	PARAMETER	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.4	—	0.75	—	0.85	ns
DD25	DQS DQ in HOLD time from DQS	t_{QH}	1.75	—	2.05	—	2.6	—	ns
DD26	DQS output access time from SDCLK posedge	t_{DQSCK}	2	5	2	5.5	2	6.5	ns

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock)

4.6.9 DDR2 SDRAM Specific Parameters

Figure 35 shows the timing parameters for DDR2. The timing parameters for this diagram appear in Table 58.

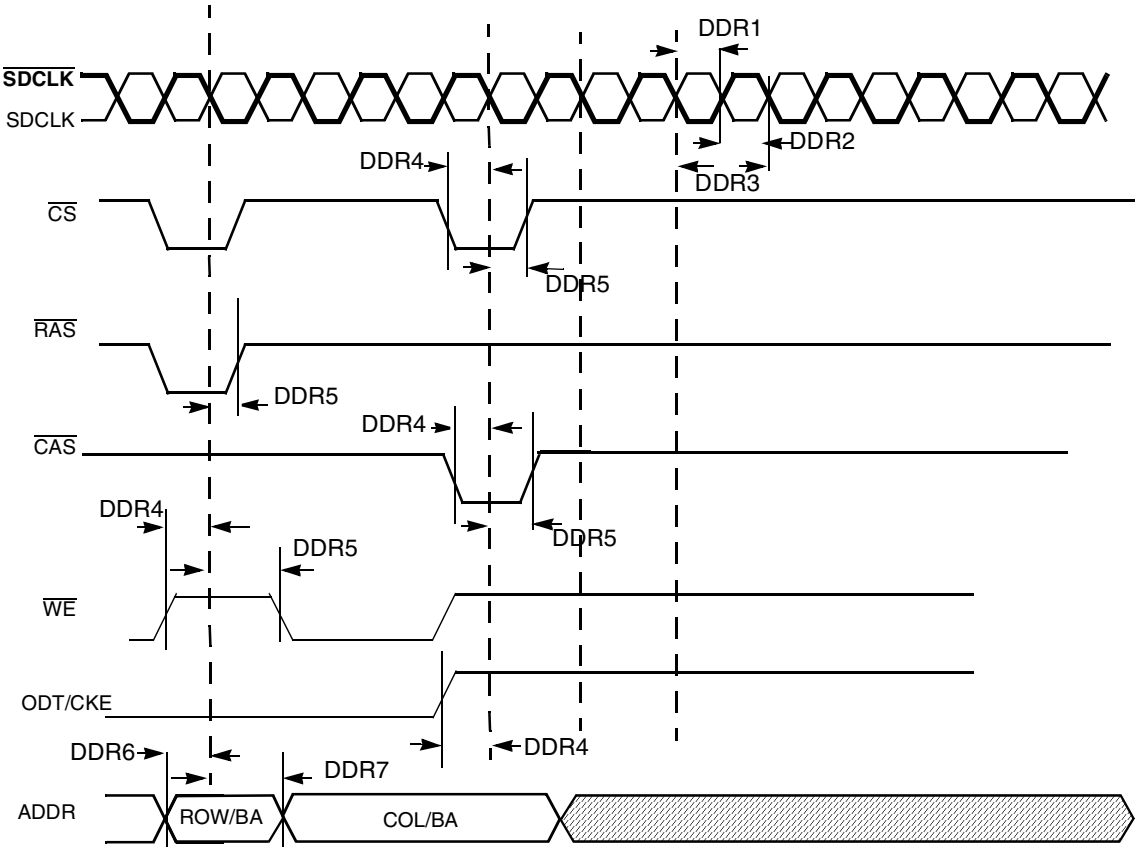

Figure 35. DDR2 SDRAM Basic Timing Parameters

Table 58. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	5	—	ns
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}[1]	1.5	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}[1]	1.7	—	ns

4.7.4.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 72 lists MII asynchronous inputs signal timing information. Figure 45 shows MII asynchronous input timings listed in Table 72.

Table 72. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

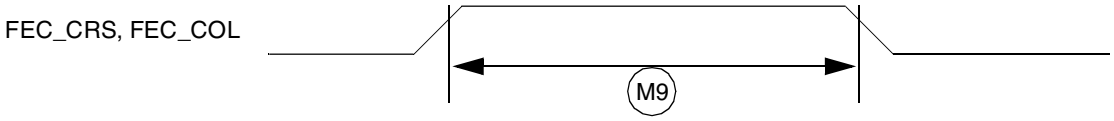

Figure 45. MII Async Inputs Timing Diagram

4.7.4.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 73 lists MII serial management channel timings. Figure 46 shows MII serial management channel timings listed in Table 73. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 73. MII Transmit Signal Timing

ID	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

4.7.6.1 Standard and Fast Mode Timing Parameters

Figure 47 depicts the standard and fast mode timings of HS-I^{2}C module, and Table 75 lists the timing characteristics.

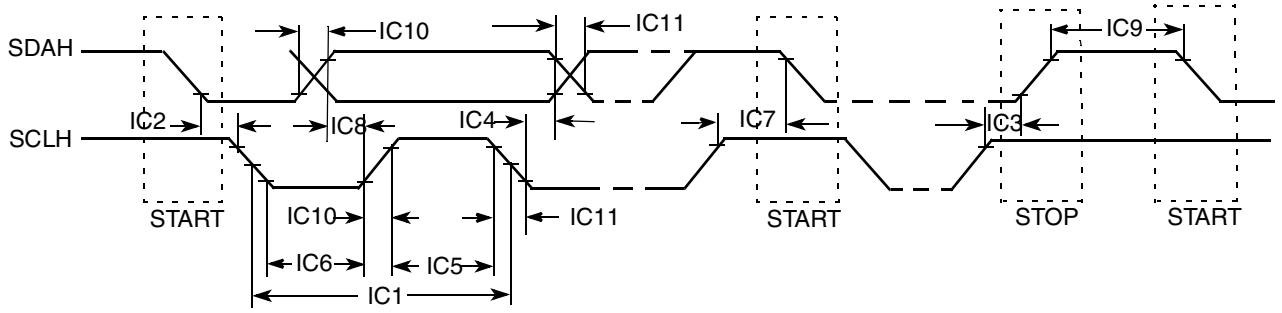

Figure 47. HS-I^{2}C Standard and Fast Mode Bus Timing

Table 75. HS-I^{2}C Timing Parameters—Standard and Fast Mode

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	SCLH cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of SCLH Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the SCLH Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both SDAH and SCLH signals	—	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both SDAH and SCLH signals	—	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	100	—	100	pF

1 A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC6) of the SCLH signal

3 A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement of Set-up time (ID No IC8) of 250 ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCLH signal.

If such a device does stretch the LOW period of the SCLH signal, it must output the next data bit to the SDAH line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLH line is released.

4 C_b = total capacitance of one bus line in pF.

joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

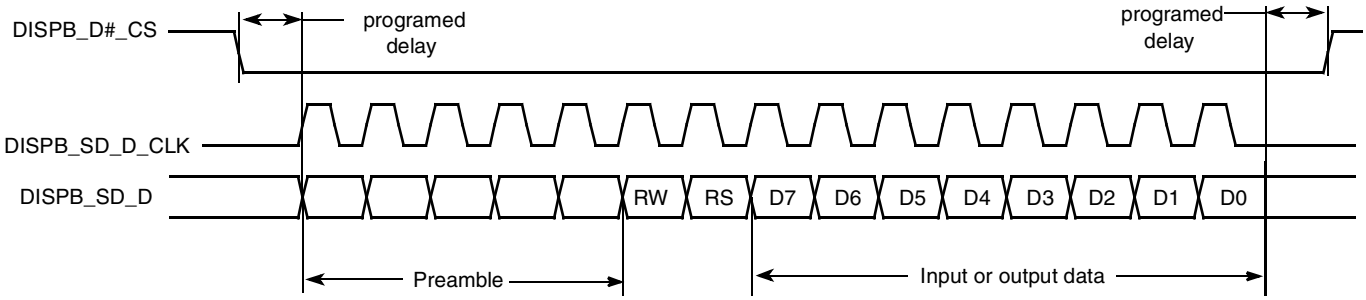

Figure 64. 3-Wire Serial Interface Timing Diagram

Figure 65 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

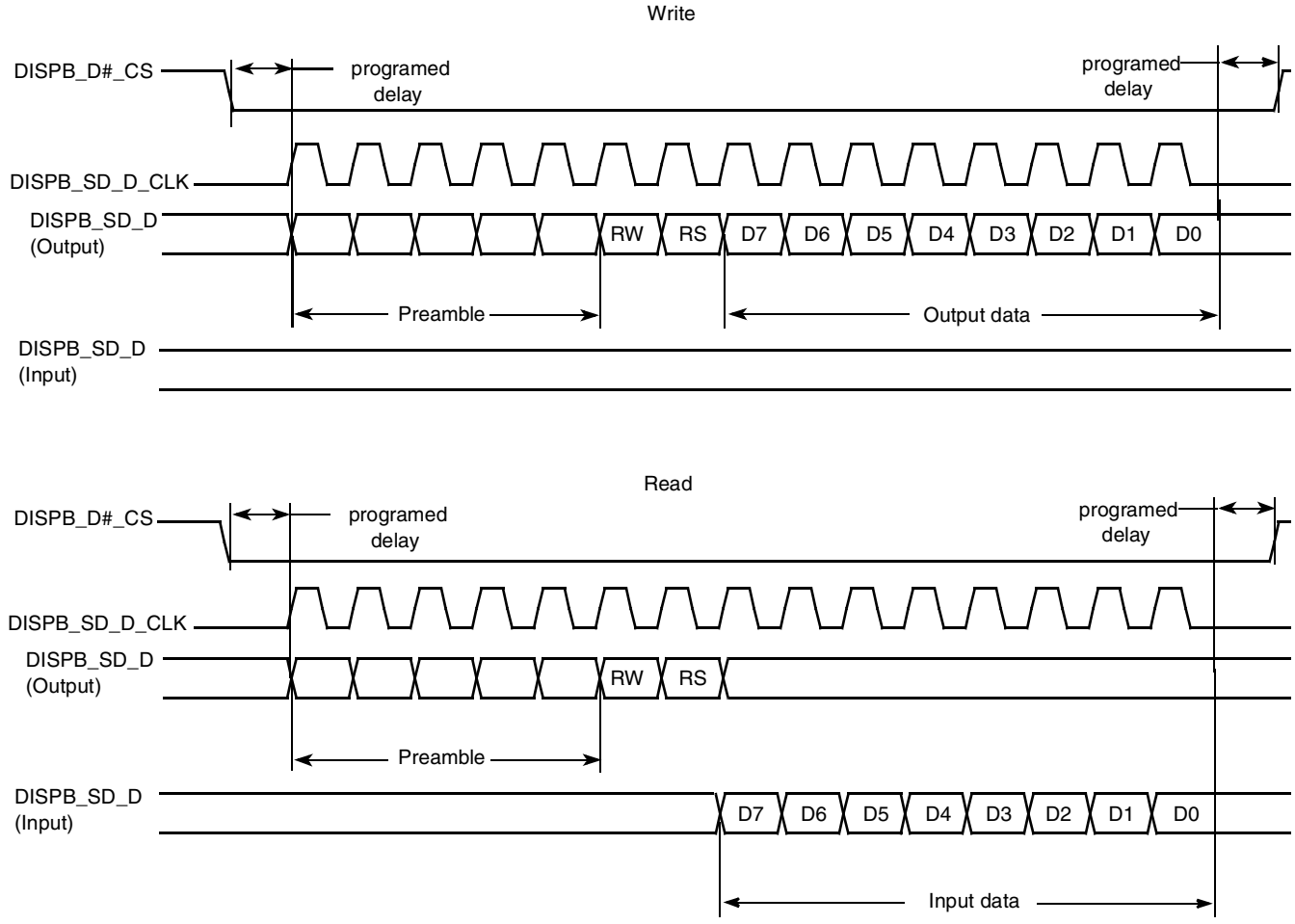

Figure 65. 4-Wire Serial Interface Timing Diagram

4.7.12.1 Reset Sequence

4.7.12.1.1 Cards with internal reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 85):

- After power up, the clock signal is enabled on SIMx_CLKy(time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

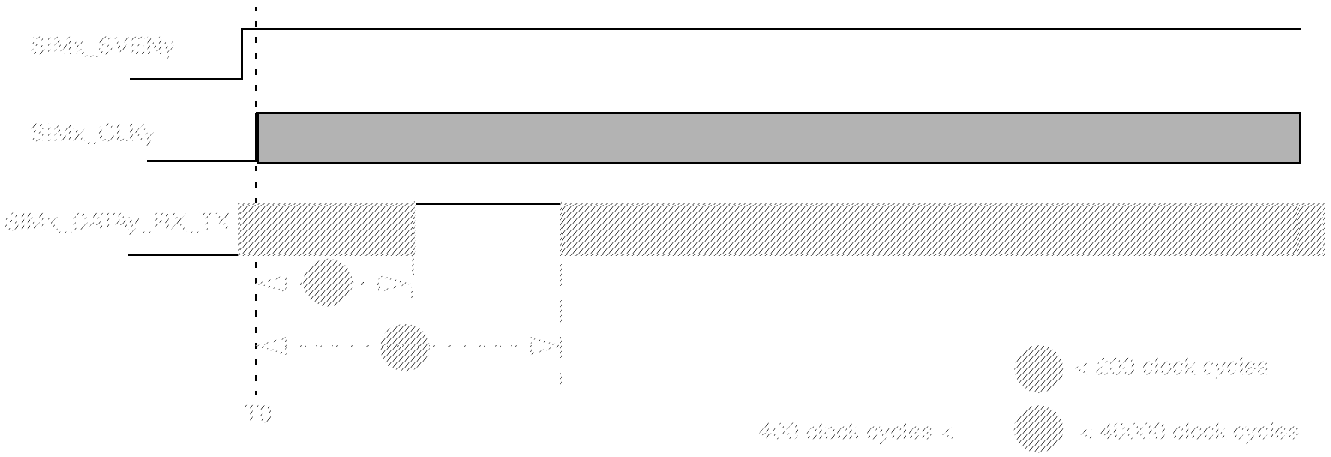

Figure 85. Internal-Reset Card Reset Sequence

4.7.12.1.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 86):

- After power-up, the clock signal is enabled on SIMx_CLKy (time T0)
- After 200 clock cycles, SIMx_DATAy_RX_TX must be high.
- SIMx_RSTy must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
- SIMx_RSTy is set High (time T1)
- SIMx_RSTy must remain High for at least 40000 clock cycles after T1 and a response must be received on SIMx_DATAy_RX_TX between 400 and 40000 clock cycles after T1.

Each of these steps is done in one CKIL period (usually 32 kHz). Power-down can be started because of a SIM Card removal detection or launched by the processor. Figure 87 and Table 98 shows the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

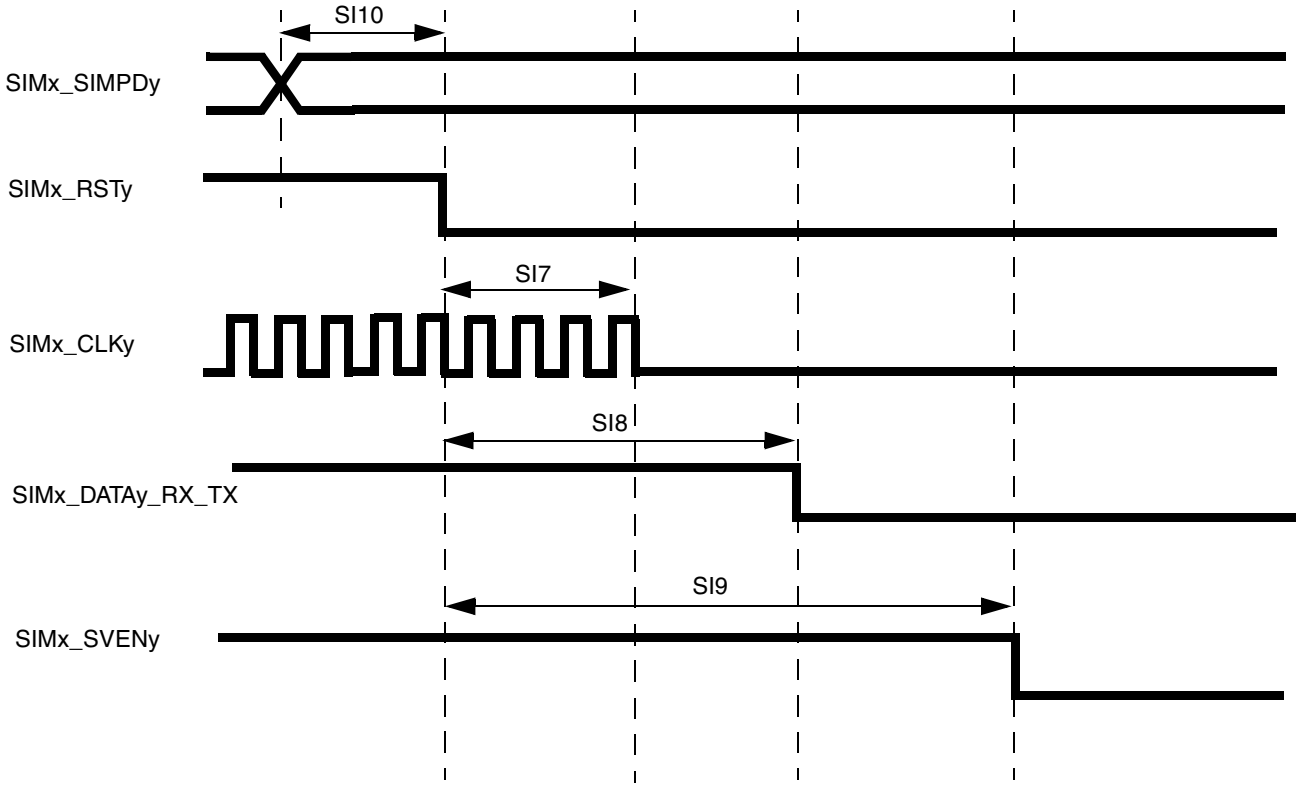

Figure 87. SmartCard Interface Power Down AC Timing

Table 98. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9×1/Fckil	1.1×1/Fckil	ns
SI8	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8×1/Fckil	2.2×1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7×1/Fckil	3.3×1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9×1/Fckil	1.1×1/Fckil	ns

5.1.1 BGA—Case 2058 13 x 13 mm, 0.5 mm Pitch

Figure 109 shows the top view, bottom view, and side view of the 13 ×13 mm package.

Figure 109. Package: Case 2058—0.5 mm Pitch

5.1.1.1 13 x 13 mm Package Drawing Notes

The following notes apply to Figure 109.

1 All dimensions in millimeters.

2 Dimensioning and tolerancing per ASME Y14.5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

Table 130. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
VDD_ANA_PLL_B	W19
VDD_DIG_PLL_A	U6
VDD_DIG_PLL_B	W18
VDD_FUSE	R7
VDDA	G8, H8, H12, M8, P16, T13
VDDA33	L18
VDDGP	F6, F7, F8, F9, F10, F11, F12, G6, G7, H7, J7, K7
VREFOUT	U15
VREF	R5
VREG	K21

5.2.2.2 19 x 19 mm, Signal Assignments, Power Rails, and I/O

Table 131 displays an alpha-sorted list of the signal assignments including power rails.

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
AUD3_BB_CK	C8	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_FS	A9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_RXD	B9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_TXD	E9	NVCC_PER9	GPIO	Input	Keeper
BOOT_MODE0	AB21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
BOOT_MODE1	AB22	NVCC_PER3	LVIO	Input	100 kΩ pull-up
CKIH1	V19	NVCC_PER3	Analog	Input	Analog
CKIH2	AA20	NVCC_PER3	Analog	Input	Analog
CKIL	Y16	NVCC_SRTC_POW	GPIO	Input	Standard CMOS
CLK_SS	AA21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
COMP[2]	Y17	AHVDDRGB	Analog	Input	Analog
CSI1_D10	R22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D11	R23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D12	P22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D13	P23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D14	M20	NVCC_HS10	HSGPIO	Input	Keeper

Table 133. 13 × 13 mm, 0.5 mm Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_D11	DRAM_D8	DRAM_SDQS1_B	DRAM_DQM0	DRAM_A4	DRAM_A6	DRAM_A11	1
2	DRAM_D10	DRAM_D9	DRAM_SDQS1	DRAM_DQM1	DRAM_A5	DRAM_A7	DRAM_A14	2
3	DRAM_D4	DRAM_D6	DRAM_SDQS0	DRAM_A1	DRAM_A3	DRAM_A8	DRAM_CS1	3
4	DRAM_D5	DRAM_D7	DRAM_SDQS0_B	DRAM_A0	DRAM_A2	DRAM_A10	DRAM_A13	4
5	NVCC_EMI_DRAM	NVCC_EMI_DRAM	GND	—	GND	NVCC_EMI_DRAM	NVCC_EMI_DRAM	5
6	—	EIM_A20	EIM_CS1	EIM_CRE	VREF	VDDA	VDDA	6
7	GND	EIM_CS5	—	—	—	—	—	7
8	—	EIM_CS3	—	NVCC_EMI	NVCC_EMI	GND	GND	8
9	—	EIM_A24	—	NVCC_PER14	GND	GND	GND	9
10	GND	EIM_BCLK	—	NVCC_PER3	GND	GND	GND	10
11	—	EIM_D28	—	NVCC_I2C	GND	GND	GND	11
12	—	EIM_A16	—	NVCC_SRTC_POW	GND	GND	GND	12
13	GND	EIM_A18	—	AHVSSRGB	GND	GND	VCC	13
14	—	EIM_OE	—	AHVSSRGB	VCC	VCC	VCC	14
15	—	EIM_RW	—	AHVDDRGB	VCC	VCC	VCC	15
16	GND	VDDA	—	AHVDDRGB	VCC	VCC	VDDA33	16
17	—	EIM_CS0	—	DISP2_DAT9	—	—	—	17
18	—	EIM_DA5	—	DI1_PIN11	DISP2_DAT13	DI1_D1_CS	DISP2_DAT10	18
19	GND	I2C1_DAT	—	—	—	—	—	19
20	—	DISPB2_SER_DIO	DI1_D0_CS	NVCC_IPU2	DISP2_DAT14	DISP2_DAT0	DISP2_DAT6	20
21	—	—	—	—	GND	—	—	21
22	CKIL	CLK_SS	BOOT_MODE0	NVCC_IPU8	DISP2_DAT2	DISP1_DAT1	DISP1_DAT5	22
23	CKIH2	DISPB2_SER_DIN	DISPB2_SER_RS	DISP2_DAT15	DISP2_DAT3	DISP1_DAT0	DISP1_DAT4	23
24	BOOT_MODE1	POR_B	DI1_PIN13	DISP2_DAT11	DISP2_DAT4	DISP1_DAT2	CSI1_D10	24
25	RESET_IN_B	DISPB2_SER_CLK	DI1_PIN12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	CSI1_D11	25
	AA	Y	W	V	U	T	R	

Table 134. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	P	N	M	L	K	J	H	
1	DRAM_SDQS0_B	DRAM_D9	DRAM_D12	DRAM_D18	DRAM_D19	DRAM_SDQS2	DRAM_D25	1
2	DRAM_SDQS0	DRAM_D8	DRAM_DQM1	DRAM_D17	DRAM_DQM2	DRAM_SDQS2_B	DRAM_D26	2
3	DRAM_DQM0	DRAM_SDQS1_B	DRAM_D10	DRAM_D16	DRAM_D20	DRAM_D22	DRAM_SDQS3	3
4	DRAM_D6	DRAM_SDQS1	DRAM_D11	DRAM_D15	DRAM_D21	DRAM_D23	DRAM_SDQS3_B	4
5	DRAM_D5	DRAM_D7	DRAM_D13	DRAM_D14	DRAM_D24	DRAM_D27	DRAM_DQM3	5
6	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	VCC	VCC	VCC	VCC	VDDGP	VDDGP	VDDGP	7
8	GND	GND	VDDA	GND	GND	GND	VDDA	8
9	GND	GND	GND	GND	GND	GND	GND	9
10	GND	GND	GND	GND	GND	GND	NVCC_PER9	10
11	GND	GND	GND	GND	GND	SGND	NVCC_PER10	11
12	GND	GND	GND	GND	GND	GND	VDDA	12
13	GND	GND	GND	GND	GND	GND	VCC	13
14	GND	GND	GND	GND	GND	GND	SVCC	14
15	GND	GND	GND	VCC	VCC	VCC	NVCC_PER15	15
16	VDDA	GND	NVCC_HS10	NGND_USBPHY	VCC	VCC	NVCC_PER8	16
17	VCC	VCC	NVCC_HS6	NVCC_USBPHY	NVCC_IPU7	NVCC_IPU6	NVCC_IPU5	17
18	NVCC_IPU8	NVCC_HS4_2	NVCC_HS4_1	VDDA33	DI2_PIN3	DI1_DISP_CLK	DISP1_DAT19	18
19	DISP2_DAT8	DISP2_DAT6	DISP2_DAT1	ID	RREFEXT	DI_GP2	DISP1_DAT21	19
20	DISP2_DAT2	DISP1_DAT0	CSI1_D14	CSI2_D14	VBUS	DI2_PIN2	DI1_PIN15	20
21	DISP2_DAT3	DISP1_DAT1	CSI1_D15	CSI2_D15	VREG	DI2_DISP_CLK	DI_GP1	21
22	CSI1_D12	CSI1_D16	CSI1_D18	CSI2_D16	DN	DI_GP4	DI_GP3	22
23	CSI1_D13	CSI1_D17	CSI1_D19	CSI2_D17	DP	GPANAIO	DI2_PIN4	23
	P	N	M	L	K	J	H	

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 4	08/2010	• Updated Case Temperature Range column of Table 1, "Ordering Information," on page 3. • Updated Table 13, "i.MX51 Operating Ranges," on page 19 to include separate specification for case temperature for industrial parts. • Removed table footnote in Table 16, "i.MX51 Stop Mode Current and Power Consumption," on page 21. • Removed table footnote in Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. • Updated Table 52, "WEIM Interface Pinout in Various Configurations," on page 55.
Rev. 3	06/2010	• Updated Max column of Table 15, "Fuse Supply Current," on page 21. Deleted eFuse Read Current row from the same table. • Updated Symbol, Test Conditions, and Max columns of Table 18, "GPIO/HSGPIO DC Electrical Characteristics," on page 25. • Updated Max and Unit columns of Table 19, "DDR2 I/O DC Electrical Parameters," on page 26. • Updated Test Conditions, Max, and Unit columns of Table 20, "LVIO DC Electrical Characteristics," on page 26 • Updated Symbol, Test Conditions, Max, and Unit columns of Table 21, "UHVIO DC Electrical Characteristics," on page 27. • Updated Max and Unit columns of Table 22, "I2C Standard/Fast/High-Speed Mode Electrical Parameters for Low/Medium Drive Strength," on page 29. • Added a new table Table 25, "I/O Leakage Current," on page 31.