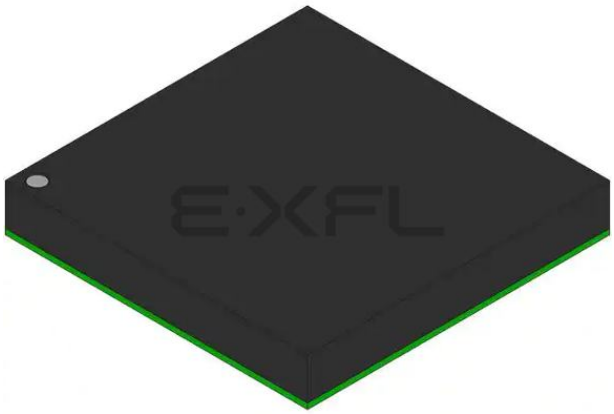

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1.1 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information[1]

Part Number[2,]	Mask Set	Features	Case Temperature Range (°C)	Package[3]
MCIMX512CJM6C	M77X	No hardware video codecs No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX512DJM8C	M77X	No hardware video codecs No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513CJM6C	M77X	No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513DJM8C	M77X	No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515CJM6C	M77X	Full specification	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DJM8C	M77X	Full specification	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DVK8C	M77X	Full specification	–20 to 85	13 x 13 mm, 0.5 mm pitch BGA Case 2058

1 For Junction Temperature (Tj) maximum ratings, see Table 11, "Absolute Maximum Ratings," on page 18.

2 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon ( )

3 Case 2017 and Case 2058 are RoHS compliant, lead-free, MSL = 3.

3.4 eCSPI/CSPI IOMUX Pin Configuration

The contacts assigned to the signals used by the three SPI modules is shown in Table 7.

Table 7. SPI IOMUX Pin Configuration

Signal	eCSPI1	eCSPI2	CSPI
MISO	CSPI1_MISO.alt0	NANDF_RB3.alt2	USBH1_NXT.alt1
MOSI	CSPI1_MOSI.alt0	NANDF_D15.alt2	USBH1_DIR.alt1
RDY	CSPI1_RDY.alt0	NANDF_RB1.alt2	USBH1_STP.alt1
SCLK	CSPI1_SCLK.alt0	NANDF_RB2.alt2	USBH1_CLK.alt1
SS0	N/A[1]	N/A	N/A
SS1	N/A	N/A	USBH1_DATA5.alt1
SS2	N/A	N/A	N/A
SS3	N/A	N/A	N/A

[1] N/A in the ROM code indicates the pins are not available.

3.5 Wireless External Interface Module (WEIM)

The WEIM interface signals are not configured in the IOMUX. The WEIM interface uses dedicated contacts on the IC.

3.6 UART IOMUX Pin Configuration

The contacts assigned to the signals used by the three UART modules are shown in Table 8.

Table 8. UART IOMUX Pin Configuration

Signal	UART1	UART2	UART3
TXD	UART1_TXD.alt0	UART2_TXD.alt0	UART3_TXD.alt1
RXD	UART1_RXD.alt0	UART2_RXD.alt0	UART3_RXD.alt1
CTS	UART1_CTS.alt0	USBH1_DATA0.alt1	KEY_COL5.alt2
RTS	UART1_RTS.alt0	USBH1_DATA3.alt1	KEY_COL4.alt2

3.7 USB-OTG IOMUX Pin Configuration

The interface signals of the UTMI PHY are not configured in the IOMUX. The UTMI PHY interface uses dedicated contacts on the IC.

Table 9. ULPI PHY IOMUX Pin Configuration

Signal	ULPI PHY
USB_PWR	GPIO1_8.alt1
USB_OC	GPIO1_9.alt1

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. AC electrical characteristics for slow and fast I/O are presented in the Table 29 and Table 30, respectively.

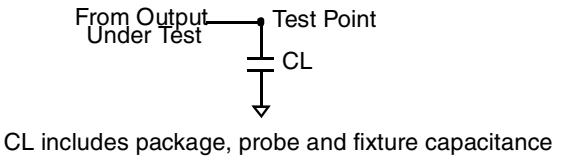

Figure 4. Load Circuit for Output

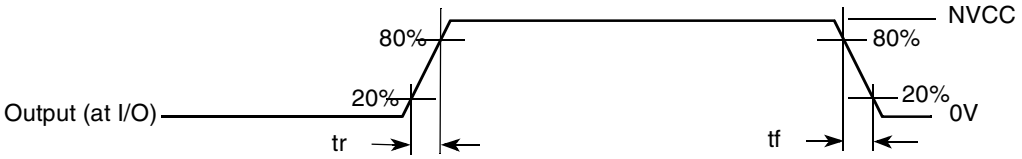

Figure 5. Output Transition Time Waveform

4.5.1 Slow I/O AC Parameters

Table 29 shows the slow I/O AC parameters.

Table 29. Slow I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.98/1.52 3.08/2.69	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.31/1.838 3.8/2.4	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.92/2.43 5.37/4.99	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.93/4.53 10.55/9.79	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	mA/ns

Table 53. WEIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—

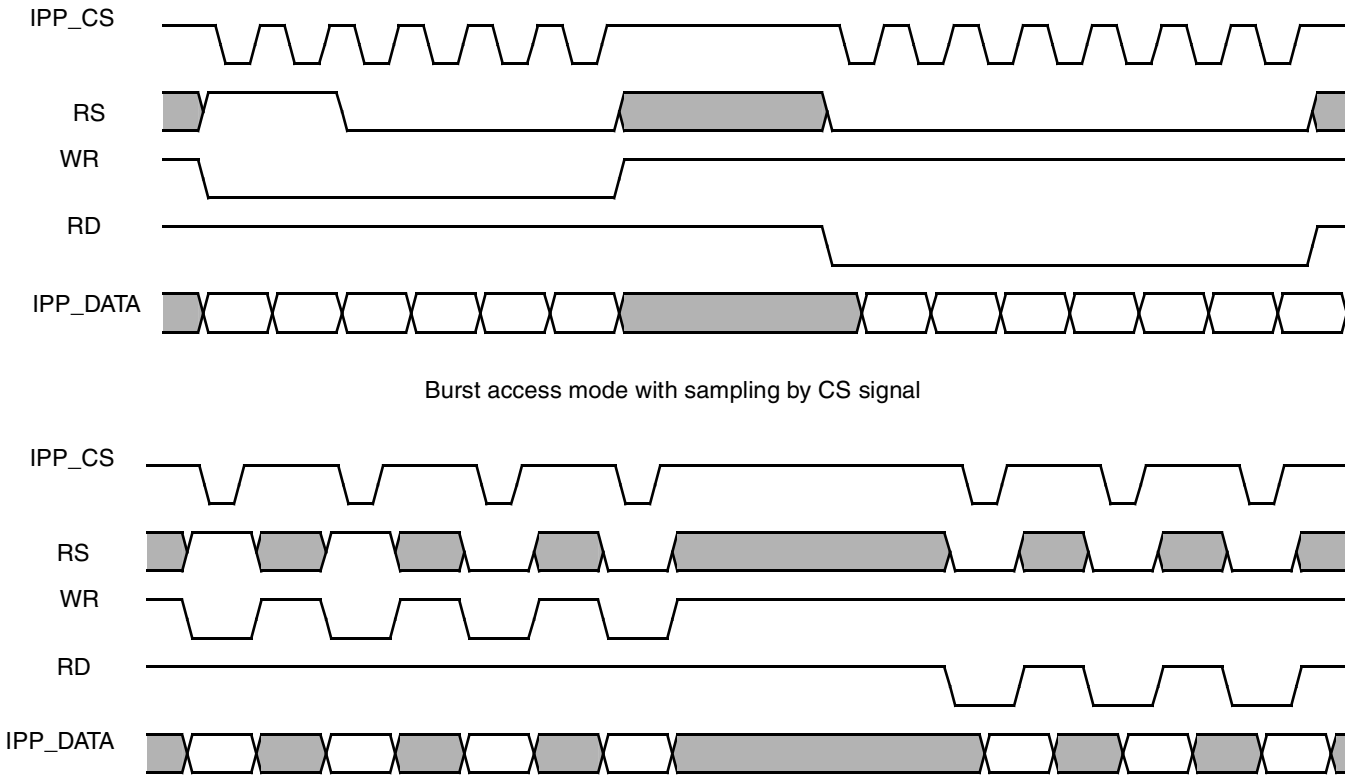

Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

4.7.8.7.2 Asynchronous Parallel Interface Timing Parameters

Figure 63 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 84 shows the timing characteristics at display access level. Table 83 shows the timing characteristics at the logical level—from configuration perspective. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

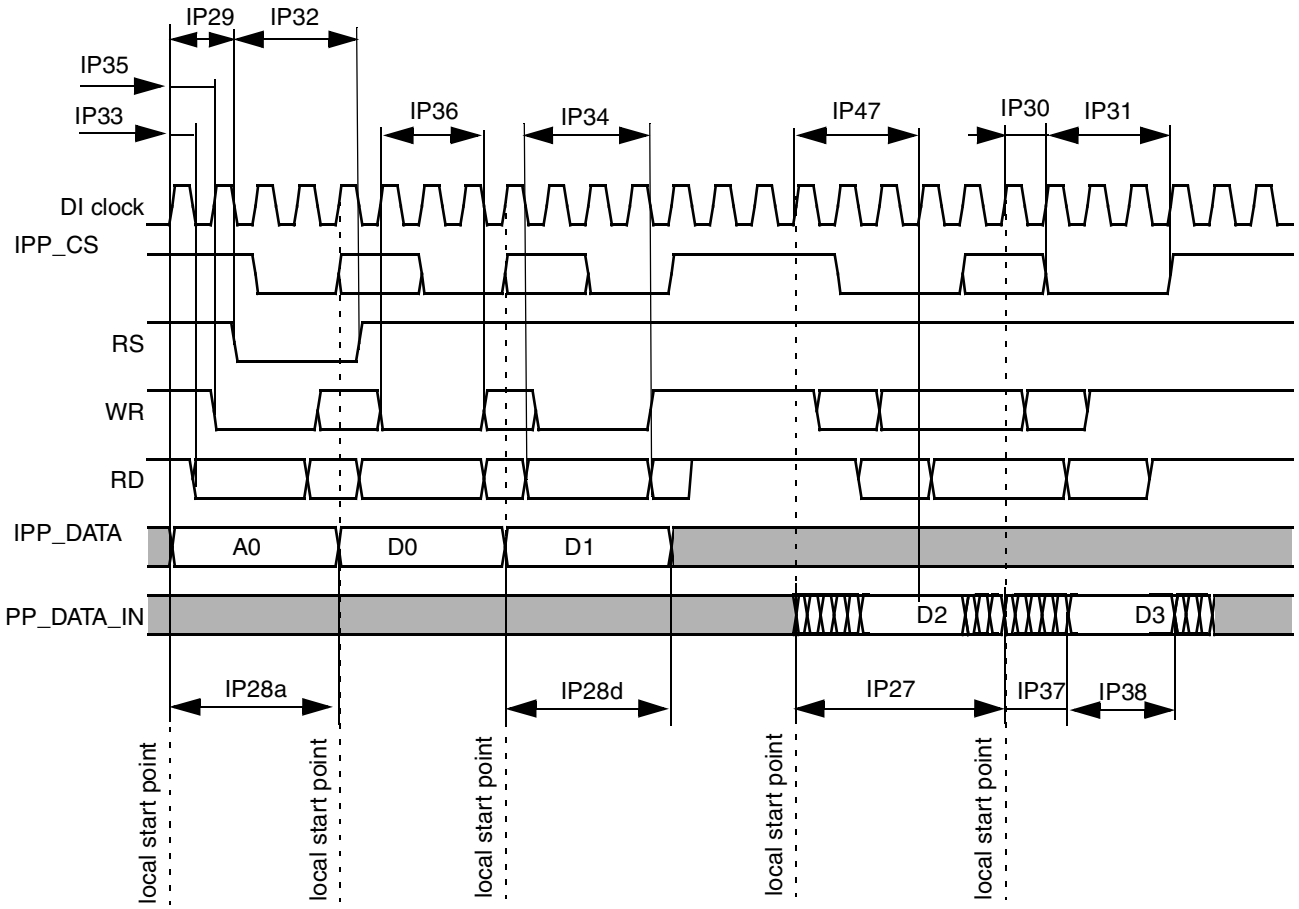

Figure 63. Asynchronous Parallel Interface Timing Diagram

Table 83. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP27	Read system cycle time	Tcycr	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns

Table 84. Asynchronous Parallel Interface Timing Parameters (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP39	Setup time for wait signal	Tswait	—	—	—	—
IP47	Read time point[13]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display period value for read

$$Tdicpr = T_{DI\_CLK} \times ceil\left[\frac{DI\_ACCESS\_SIZE\_\#}{DI\_CLK\_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER

[3]Display period value for write

$$Tdicpw = T_{DI\_CLK} \times ceil\left[\frac{DI\_ACCESS\_SIZE\_\#}{DI\_CLK\_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER

[4]Display control down for CS

$$Tdicdcs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[5]Display control up for CS

$$Tdicucs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[6]Display control down for RS

$$Tdicdrs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[7]Display control up for RS

$$Tdicurs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[8]Display control down for read

$$Tdicdr = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

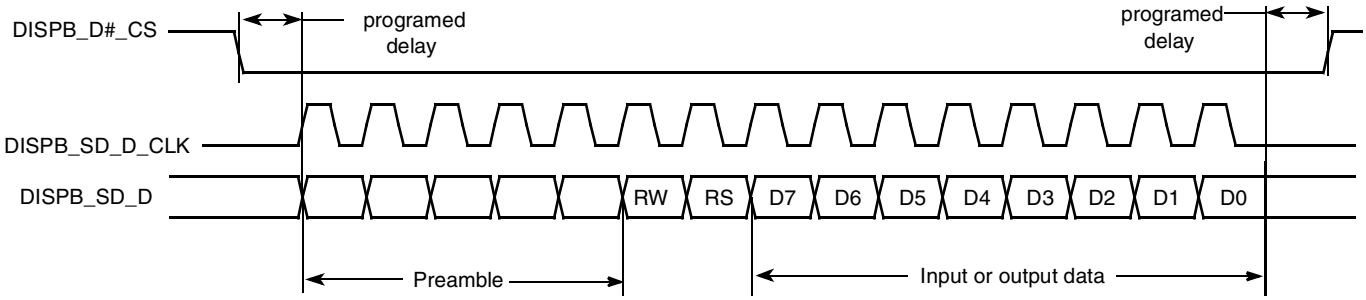

Figure 64. 3-Wire Serial Interface Timing Diagram

Figure 65 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

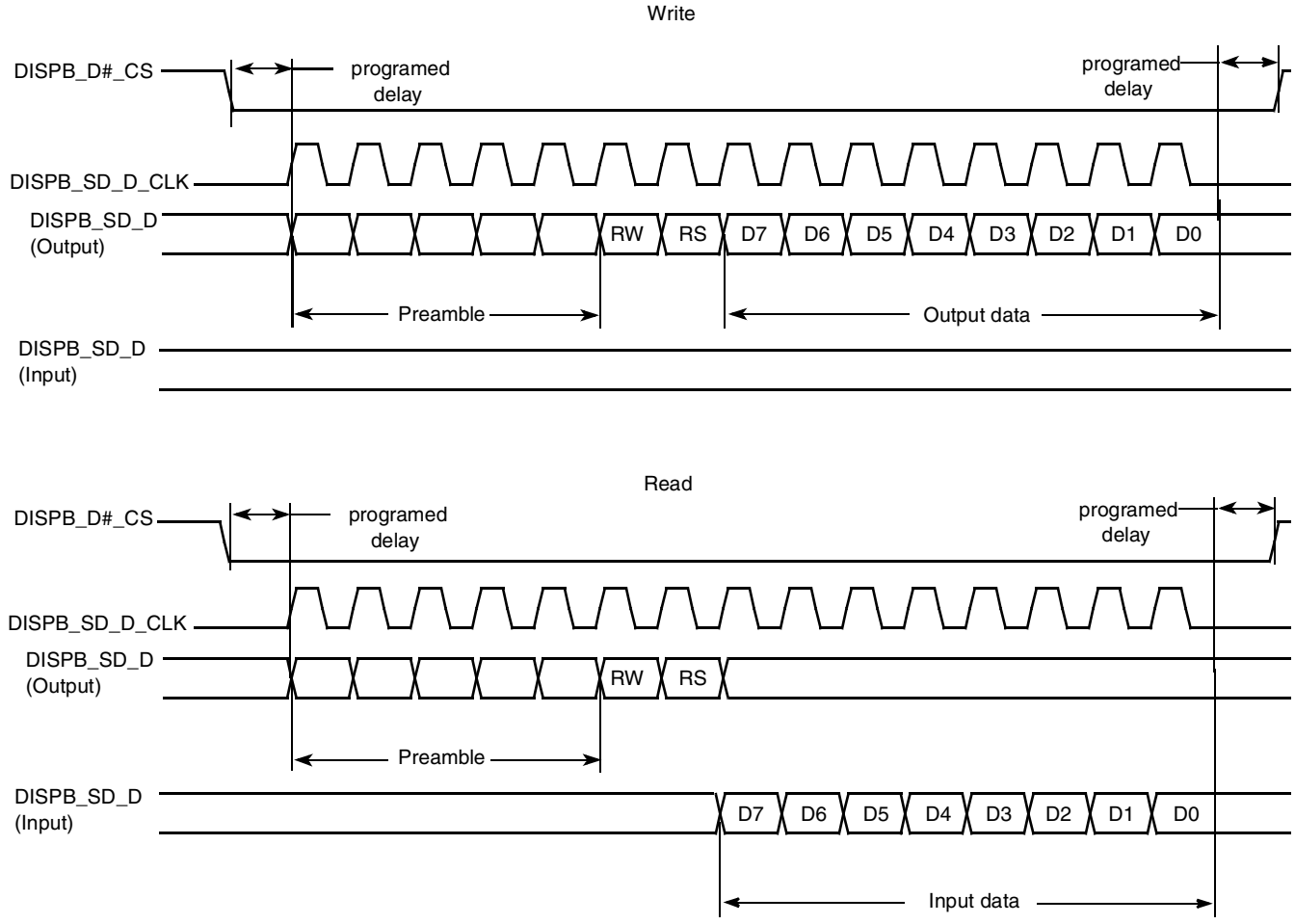

Figure 65. 4-Wire Serial Interface Timing Diagram

Figure 66 depicts timing of the 5-wire serial interface. For this interface, a separate RS line is added.

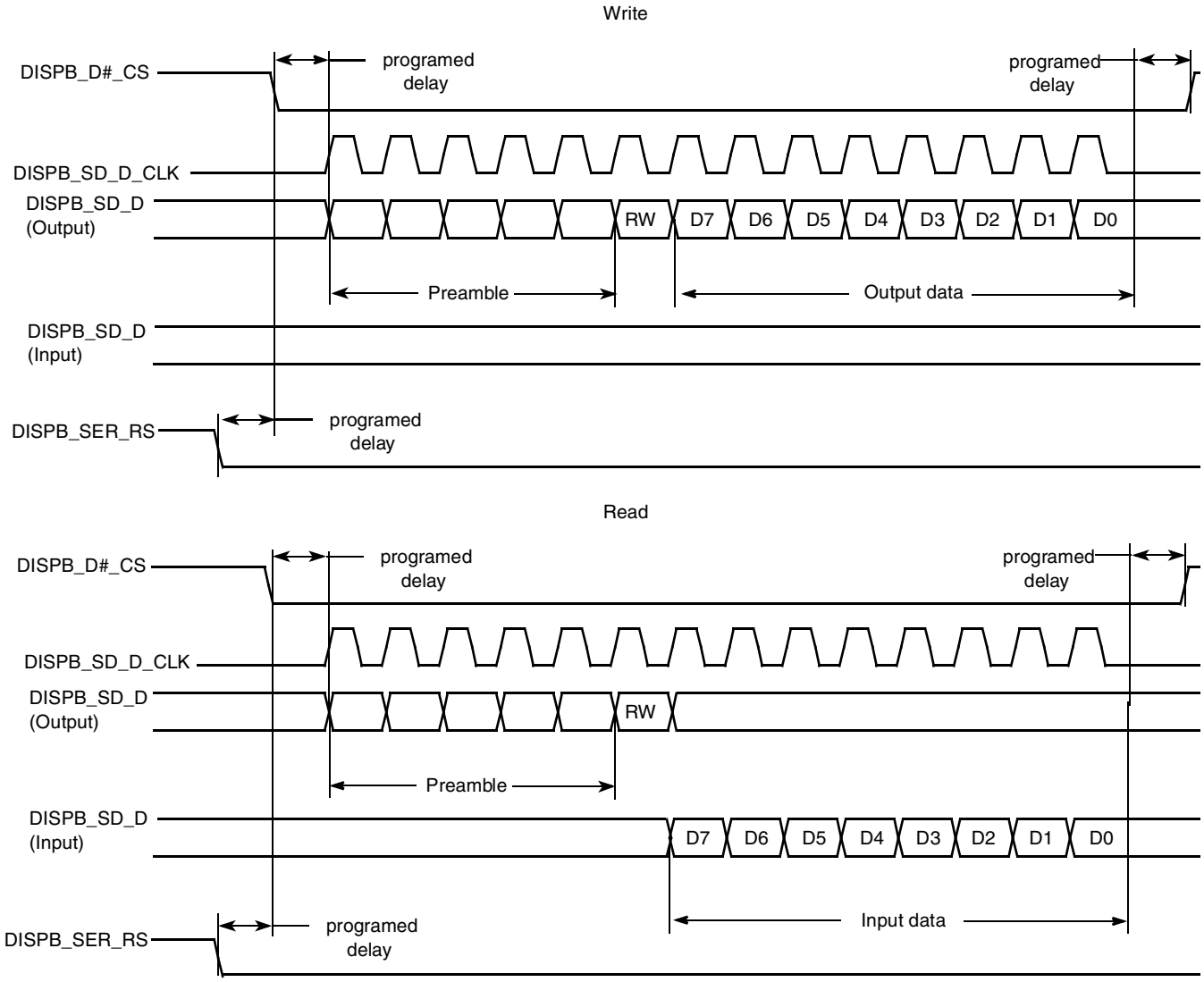

Figure 66. 5-Wire Serial Interface Timing Diagram

[4]Display interface clock down time for read

$$Tdicdr = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

[5]Display interface clock up time for read

$$Tdicur = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

[6]Display interface clock down time for write

$$Tdicdw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

[7]Display interface clock up time for write

$$Tdicuw = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

[8]This parameter is a requirement to the display connected to the IPU

[9]Data read point

$$Tdrp = T_{DI\_CLK} \times ceil\left[\frac{DISP\_READ\_EN}{DI\_CLK\_PERIOD}\right]$$

DISP_RD_EN is predefined in REGISTER

[10]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

[11]Display interface clock offset value

$$Toclk = T_{DI\_CLK} \times ceil\left[\frac{DISP\_CLK\_OFFSET}{DI\_CLK\_PERIOD}\right]$$

CLK_OFFSET is predefined in REGISTER

[12]Display RS up time

$$Tdicurs = T_{DI\_CLK} \times ceil\left[\frac{DISP\_RS\_UP\_\#}{DI\_CLK\_PERIOD}\right]$$

DISP_RS_UP is predefined in REGISTER

[13]Display RS down time

$$Tdicdrs = T_{DI\_CLK} \times ceil\left[\frac{DISP\_RS\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]$$

DISP_RS_DOWN is predefined in REGISTER

[14]Display RS up time

$$Tdicucs = T_{DI\_CLK} \times ceil\left[\frac{DISP\_CS\_UP\_\#}{DI\_CLK\_PERIOD}\right]$$

DISP_CS_UP is predefined in REGISTER

4.7.13 SCAN JTAG Controller (SJC) Timing Parameters

Figure 88 depicts the SJC test clock input timing. Figure 89 depicts the SJC boundary scan timing. Figure 91 depicts the TRST timing with respect to TCK. Figure 90 depicts the SJC test access port. Signal parameters are listed in Table 99.

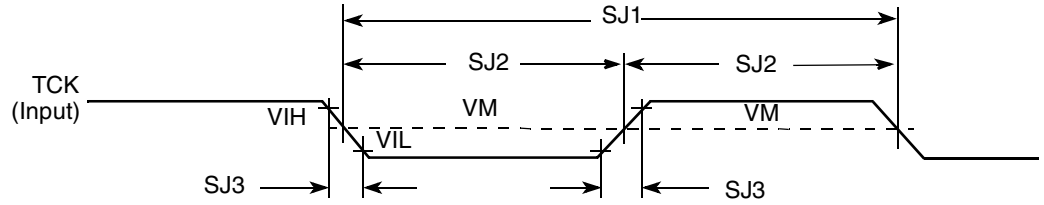

Figure 88. Test Clock Input Timing Diagram

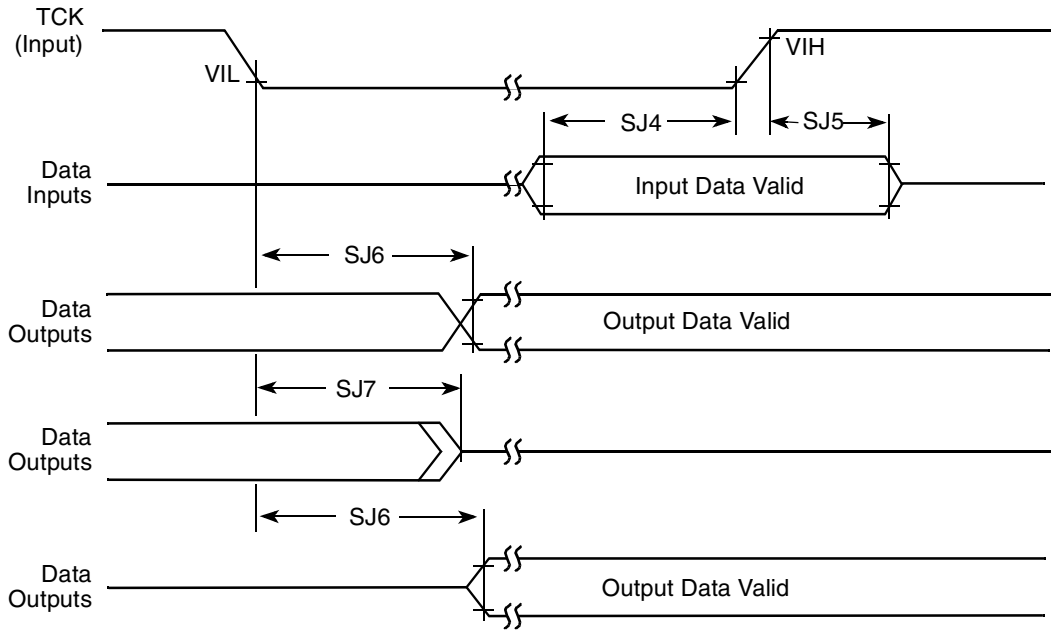

Figure 89. Boundary Scan (JTAG) Timing Diagram

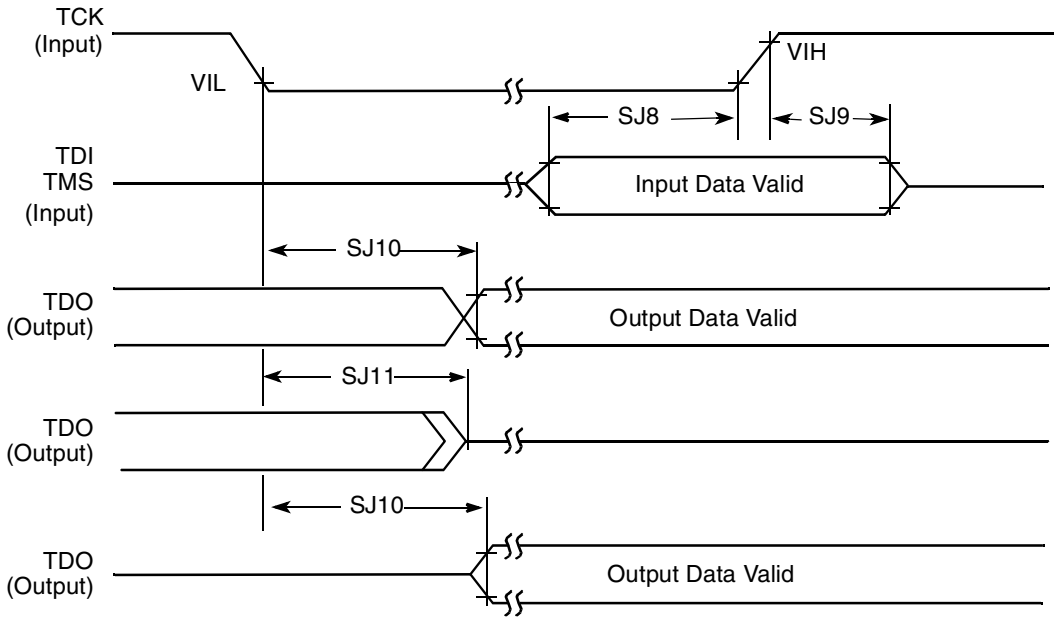

Figure 90. Test Access Port Timing Diagram

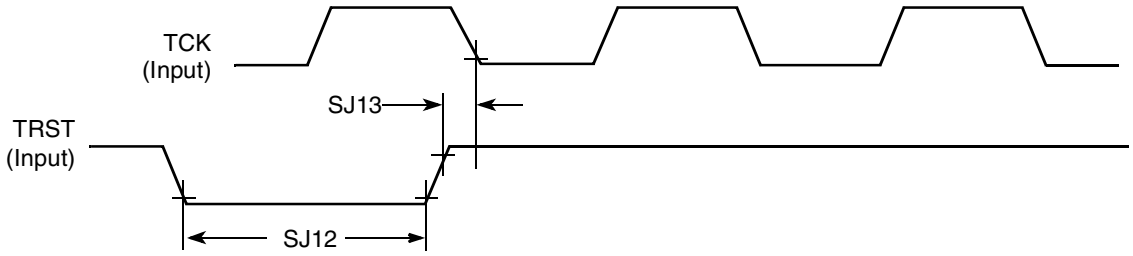

Figure 91. $\overline{\text{TRST}}$ Timing Diagram

Table 99. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
CSI1_D19	N22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D8	A20	NVCC_PER8	GPIO	Input	Keeper
CSI1_D9	B20	NVCC_PER8	GPIO	Input	Keeper
CSI1_HSYNC	C19	NVCC_PER8	GPIO	Input	Keeper
CSI1_MCLK	F19	NVCC_PER8	GPIO	Input	Keeper
CSI1_PIXCLK	D19	NVCC_PER8	GPIO	Input	Keeper
CSI1_VSYNC	B19	NVCC_PER8	GPIO	Input	Keeper
CSI2_D12	F11	NVCC_PER9	GPIO	Input	Keeper
CSI2_D13	D8	NVCC_PER9	GPIO	Input	Keeper
CSI2_D14	M25	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D15	M24	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D16	M23	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D17	M22	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D18	A7	NVCC_PER9	GPIO	Input	Keeper
CSI2_D19	C7	NVCC_PER9	GPIO	Input	Keeper
CSI2_HSYNC	J20	NVCC_PER8	GPIO	Input	Keeper
CSI2_PIXCLK	D21	NVCC_PER8	GPIO	Input	Keeper
CSI2_VSYNC	C20	NVCC_PER8	GPIO	Input	Keeper
CSPI1_MISO	F12	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_MOSI	D9	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_RDY	A8	NVCC_PER10	GPIO	Input	Keeper
CSPI1_SCLK	D11	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS0	D10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS1	F13	NVCC_PER10	GPIO	Input	100 kΩ pull-up
DI_GP1	F20	NVCC_IPU6	GPIO	Input	Keeper
DI_GP2	K20	NVCC_IPU6	GPIO	Input	Keeper
DI_GP3	H23	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI_GP4	K23	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI1_D0_CS	W20	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	T18	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J22	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	V18	NVCC_IPU2	GPIO	Output	High

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_PIN12	W25	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	W24	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	G20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	J18	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	H20	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J24	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	H24	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	J25	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	J23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	T22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	E24	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[1]	E25	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[1]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[1]	E23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[1]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[1]	F22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[1]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[1]	F24	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[1]	G23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[1]	G22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	T24	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[1]	G25	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[1]	F25	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[1]	G24	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[1]	H25	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	T25	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	R23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT5	R22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[1]	D25	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[1]	D24	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[1]	C23	NVCC_IPU4	GPIO	Input	Keeper

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A21[1]	AD6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB9	NVCC_EMI	GPIO	Output	High
EIM_A23[1]	AE5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	Y9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AD5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AB7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AC6	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	V6	NVCC_EMI	GPIO	Output	High
EIM_CS0	Y17	NVCC_EMI	GPIO	Output	High
EIM_CS1	W6	NVCC_EMI	GPIO	Output	High
EIM_CS2	AE4	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	Y8	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AC7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AB12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	AE8	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AD9	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	AC10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AD10	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	AE10	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AE11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AE9	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	AC9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AD8	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	Y11	NVCC_EMI	GPIO	Input	Keeper
EIM_D29	AD7	NVCC_EMI	GPIO	Input	Keeper
EIM_D30	AC8	NVCC_EMI	GPIO	Input	Keeper
EIM_D31	AB8	NVCC_EMI	GPIO	Input	Keeper
EIM_DA0	AE15	NVCC_EMI	GPIO	Input	Keeper

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
STR	A15	NVCC_PER12	—	—	—
TEST_MODE	V20	NVCC_PER3	GPIO	Input	100 kΩ pull-down
UART1_CTS	B14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RTS	D13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RXD	E13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_TXD	A13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_RXD	A14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_TXD	C14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART3_RXD	F14	NVCC_PER12	GPIO	Input	Keeper
UART3_TXD	B15	NVCC_PER12	GPIO	Input	Keeper
USBH1_CLK	D11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA0	E12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA1	A11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA2	B12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA3	C12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA4	D12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA5	A12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA6	B13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA7	C13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DIR	B11	NVCC_PER11	GPIO	Input	Keeper
USBH1_NXT	C11	NVCC_PER11	GPIO	Input	Keeper
USBH1_STP	E11	NVCC_PER11	GPIO	Input	Keeper
XTAL[2]	AC20	NVCC_OSC	Analog	Output	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 See Table 3 on page 12 for more information.

3 During power-on reset this port acts as input for fuse override signal. See Table 132 on page 189 for more information.

4 During power-on reset this port acts as output for diagnostic signal. See Table 132 on page 189 for more information.

5.2.2.3 Fuse Override Considerations

Table 132 lists the contacts that can be overridden with fuse settings.

Table 132. Fuse Override Contacts

Contact Name	Direction After Reset	Configuration After Reset	Signal Configuration[1]	External Termination for Fuse Override
DISP1_DAT10	Input	Keeper	BT_SPARE_SIZE	4.7 kΩ pull-up or pull-down
DISP1_DAT11	Input	Keeper	BT_LPB_FREQ[2]	4.7 kΩ pull-up or pull-down
DISP1_DAT12	Input	Keeper	BT_MLC_SEL	4.7 kΩ pull-up or pull-down
DISP1_DAT13	Input	Keeper	BT_MEM_CTL[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT14	Input	Keeper	BT_MEM_CTL[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT15	Input	Keeper	BT_BUS_WIDTH	4.7 kΩ pull-up or pull-down
DISP1_DAT16	Input	Keeper	BT_PAGE_SIZE[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT17	Input	Keeper	BT_PAGE_SIZE[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT18	Input	Keeper	BT_WEIM_MUXED[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT19	Input	Keeper	BT_WEIM_MUXED[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT20	Input	Keeper	BT_MEM_TYPE[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT21	Input	Keeper	BT_MEM_TYPE[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT22	Input	Keeper	BT_LPB_FREQ[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT23	Input	Keeper	BT_LPB_FREQ[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT6	Input	Keeper	BT_USB_SRC[2]	4.7 kΩ pull-up or pull-down
DISP1_DAT7	Input	Keeper	BT_EEPROM_CFG	4.7 kΩ pull-up or pull-down
DISP1_DAT8	Input	Keeper	BT_SRC[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT9	Input	Keeper	BT_SRC[1]	4.7 kΩ pull-up or pull-down
EIM_A16	Input	100 kΩ pull-up	OSC_FREQ_SEL[0]	4.7 kΩ pull-down or none for high level[3]
EIM_A17	Input	100 kΩ pull-up	OSC_FREQ_SEL[1]	4.7 kΩ pull-down or none for high level[2]
EIM_A18	Input	100 kΩ pull-up	BT_LPB[0]	4.7 kΩ pull-down or none for high level[2]
EIM_A19	Input	100 kΩ pull-up	BT_LPB[1]	4.7 kΩ pull-down or none for high level[2]
EIM_A20	Input	100 kΩ pull-up	BT_UART_SRC[0]	4.7 kΩ pull-down or none for high level[2]
EIM_A21	Input	100 kΩ pull-up	BT_UART_SRC[1]	4.7 kΩ pull-down or none for high level[2]
KEY_COL3	Output	High	Output for diagnostic signal INT_BOOT during power-on reset	—

Table 132. Fuse Override Contacts (continued)

Contact Name	Direction After Reset	Configuration After Reset	Signal Configuration[1]	External Termination for Fuse Override
KEY_COL4	Output	Low	Output for diagnostic signal ANY_PU_RST during power-on reset	—
KEY_COL5	Output	Low	Output for diagnostic signal JTAG_ACT during power-on reset	—

1 Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration is controlled by fuses.

2 External USB PHY selection is not functional.

3 Consider using an external 68 kΩ pull-up if system constraints indicate that the on-chip 100 kΩ pull-up is too weak.

5.2.3 19 x 19 Ball Map

See Section 5.4, “19 x 19 mm, 0.8 Pitch Ball Map.”

Table 133. 13 × 13 mm, 0.5 mm Pitch Ball Map (continued)

	P	N	M	L	K	J	H	
1	DRAM_A9	DRAM_SDCKE0	DRAM_SDCLK	DRAM_SDCKE1	DRAM_SDQS3_B	DRAM_D25	DRAM_D27	1
2	DRAM_A12	DRAM_DQM3	DRAM_SDCLK_B	EIM_SDODT0	DRAM_SDQS3	DRAM_D26	DRAM_D28	2
3	DRAM_CS0	DRAM_RAS	DRAM_SDWE	EIM_SDODT1	DRAM_SDQS2	DRAM_D22	DRAM_D20	3
4	EIM_SDBA0	DRAM_CAS	DRAM_DQM2	EIM_SDBA1	DRAM_SDQS2_B	DRAM_D24	DRAM_D23	4
5	—	GND	NVCC_EMI_DRAM	NVCC_EMI_DRAM	GND	—	—	5
6	VDD_FUSE	GND	VDDGP	VDDGP	EIM_SDBA2	NANDF_D15	NANDF_D9	6
7	—	—	—	—	—	—	—	7
8	GND	GND	VDDGP	VDDGP	VDDGP	NVCC_NANDF_A	NVCC_NANDF_B	8
9	GND	GND	VDDGP	VDDGP	VDDGP	VDDGP	NVCC_NANDF_C	9
10	SGND	GND	VDDGP	VDDGP	VDDGP	VDDGP	NVCC_PER9	10
11	GND	GND	SVDDGP	VDDGP	VDDGP	VDDGP	NVCC_PER11	11
12	VCC	VCC	GND	VDDGP	VDDGP	VDDGP	NVCC_PER10	12
13	VCC	SVCC	GND	GND	GND	GND	VDDA	13
14	VCC	VCC	GND	GND	GND	GND	NVCC_PER13	14
15	VCC	VCC	GND	GND	GND	NVCC_PER8	NVCC_PER12	15
16	NVCC_USBPHY	NVCC_IPU4	NVCC_IPU6	NVCC_IPU9	NVCC_IPU5	NVCC_PER17	NVCC_PER15	16
17	—	—	—	—	—	—	—	17
18	DISP2_DAT1	VDDA	DISP2_DAT12	DISP2_DAT8	RREFEXT	DI1_PIN2	GPIO1_0	18
19	—	—	—	—	—	—	—	19
20	NVCC_HS4_2	NVCC_HS6	NVCC_HS10	NVCC_HS4_1	DI_GP2	CSI2_HSYNC	DI1_PIN3	20
21	GND	—	—	GND	—	—	—	21
22	CSI1_D12	CSI1_D19	CSI2_D17	VBUS	GPANAIO	DI1_DISP_CLK	NVCC_IPU7	22
23	CSI1_D13	CSI1_D18	CSI2_D16	NGND_USBPHY	DI_GP4	DI2_PIN4	DI_GP3	23
24	CSI1_D14	CSI1_D16	CSI2_D15	VREG	DP	DI2_DISP_CLK	DI2_PIN2	24
25	CSI1_D15	CSI1_D17	CSI2_D14	ID	DN	DI2_PIN3	DISP1_DAT23	25
	P	N	M	L	K	J	H	

Table 134. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_SDCKE0	DRAM_A7	DRAM_RAS	EIM_SDBA0	DRAM_A13	DRAM_D0	DRAM_D3	1
2	DRAM_A1	DRAM_A5	DRAM_A8	DRAM_A10	DRAM_A12	DRAM_A14	DRAM_D2	2
3	DRAM_A2	DRAM_CS1	DRAM_A6	DRAM_A9	EIM_SDBA1	DRAM_SDCLK	DRAM_D1	3
4	EIM_BCLK	DRAM_CS0	DRAM_A4	DRAM_CAS	DRAM_A11	DRAM_SDCLK_B	DRAM_D4	4
5	EIM_CS5	EIM_DTACK	DRAM_SDCKE1	DRAM_A3	DRAM_SDWE	GND	VREF	5
6	EIM_CS4	EIM_CS1	EIM_CS0	VDD_ANA_PLL_A	VDD_DIG_PLL_A	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	EIM_OE	EIM_CS2	EIM_D31	NVCC_EMI	GND_ANA_PLL_A	GND_DIG_PLL_A	VDD_FUSE	7
8	EIM_A19	EIM_D29	EIM_D27	EIM_D23	NVCC_EMI	VCC	GND	8
9	EIM_A16	EIM_D25	EIM_D21	EIM_EB3	NVCC_EMI	VCC	GND	9
10	EIM_D24	EIM_D19	EIM_D17	EIM_EB2	NVCC_EMI	VCC	GND	10
11	EIM_D18	EIM_DA15	EIM_DA13	EIM_DA11	NVCC_EMI	VCC	GND	11
12	EIM_DA12	EIM_DA9	EIM_EB1	EIM_EB0	NVCC_EMI	VCC	GND	12
13	EIM_DA6	EIM_DA5	EIM_DA7	EIM_DA1	NVCC_PER14	VDDA	GND	13
14	EIM_DA2	JTAG_TDI	JTAG_TRSTB	JTAG_MOD	NVCC_SRTC_POW	NVCC_I2C	GND	14
15	JTAG_TDO	PMIC_STBY_REQ	I2C1_CLK	JTAG_TCK	VREFOUT	NGND_TV_BACK	GND	15
16	PMIC_INT_REQ	CKIL	PMIC_ON_REQ	TVDAC_DHVDD	NVCC_TV_BACK	GND	GND	16
17	PMIC_RDY	COMP	NVCC_OSC	NGND_OSC	GND_ANA_PLL_B	VCC	VCC	17
18	AHVDDRGB	AHVDDRGB	VDD_DIG_PLL_B	GND_DIG_PLL_B	NVCC_PER3	NVCC_IPU2	NVCC_IPU9	18
19	AHVSSRGB	AHVSSRGB	VDD_ANA_PLL_B	CKIH1	DISPB2_SER_DIN	DISP2_DAT13	DISP2_DAT11	19
20	CKIH2	FASTR_DIG	FASTR_ANA	TEST_MODE	POR_B	DI1_PIN13	DISP2_DAT9	20
21	CLK_SS	RESET_IN_B	DISPB2_SER_RS	DISPB2_SER_DIO	DI1_D0_CS	DISP2_DAT15	DISP2_DAT0	21
22	DI1_PIN12	DI1_PIN11	DISP2_DAT10	DISP2_DAT4	DISP1_DAT2	DISP1_DAT4	CSI1_D10	22
23	DISP2_DAT14	DISP2_DAT12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	DISP1_DAT5	CSI1_D11	23
	AA	Y	W	V	U	T	R	