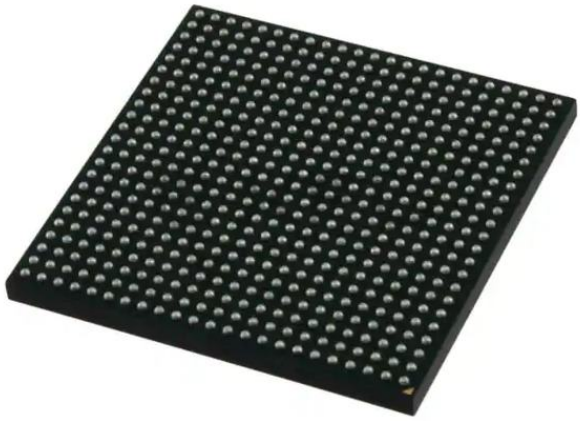

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 95°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx515cjm6cr2

Features include the following:

- **Smart Speed Technology**—The heart of the i.MX51 processors is a level of power management throughout the device that enables the rich suite of multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Smart Speed Technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than typical industry expectations.
- **Applications Processor**—The i.MX51 processors boost the capabilities of high-tier portable applications by providing for the ever-increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) allows the device run at much lower voltage and frequency with sufficient MIPS for tasks such as audio decode resulting in significant power reduction.
- **Multimedia Powerhouse**—The multimedia performance of the i.MX51 processors is boosted by a multi-level cache system and further enhanced by a Multi-Standard Hardware Video Codec, autonomous Image Processing Unit, SD and HD720p Triple Video (TV) Encoder with triple video DAC, Neon (including Advanced SIMD, 32-bit Single-Precision floating point support and Vector Floating Point co-processor), and a programmable smart DMA (SDMA) controller.
- **Powerful Graphics Acceleration**—Graphics is the key to mobile game navigation, web browsing, and other applications. The i.MX51 processors provide two independent, integrated Graphics Processing Units: OpenGL ES 2.0 3D graphics accelerator (27 Mtri/s, 166 Mpix/s) and OpenVG 1.1 2D graphics accelerator (166 Mpix/s).
- **Interface Flexibility**—The i.MX51 processor interface supports connection to all popular types of external memories: DDR2, Mobile DDR, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC), and OneNAND. Designers seeking to provide products that deliver a rich multimedia experience find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, High-Speed USB On-The-Go with PHY, and three High-Speed USB hosts, multiple expansion card ports (High-Speed MMC/SDIO Host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, I^2S serial audio, and SIM card, among others).
- **Increased Security**—Because the need for advanced security for mobile devices continues to increase, the i.MX51 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the MX51 security features contact your Freescale representative.

1.2 Block Diagram

Figure 1 shows the functional modules of the processor.

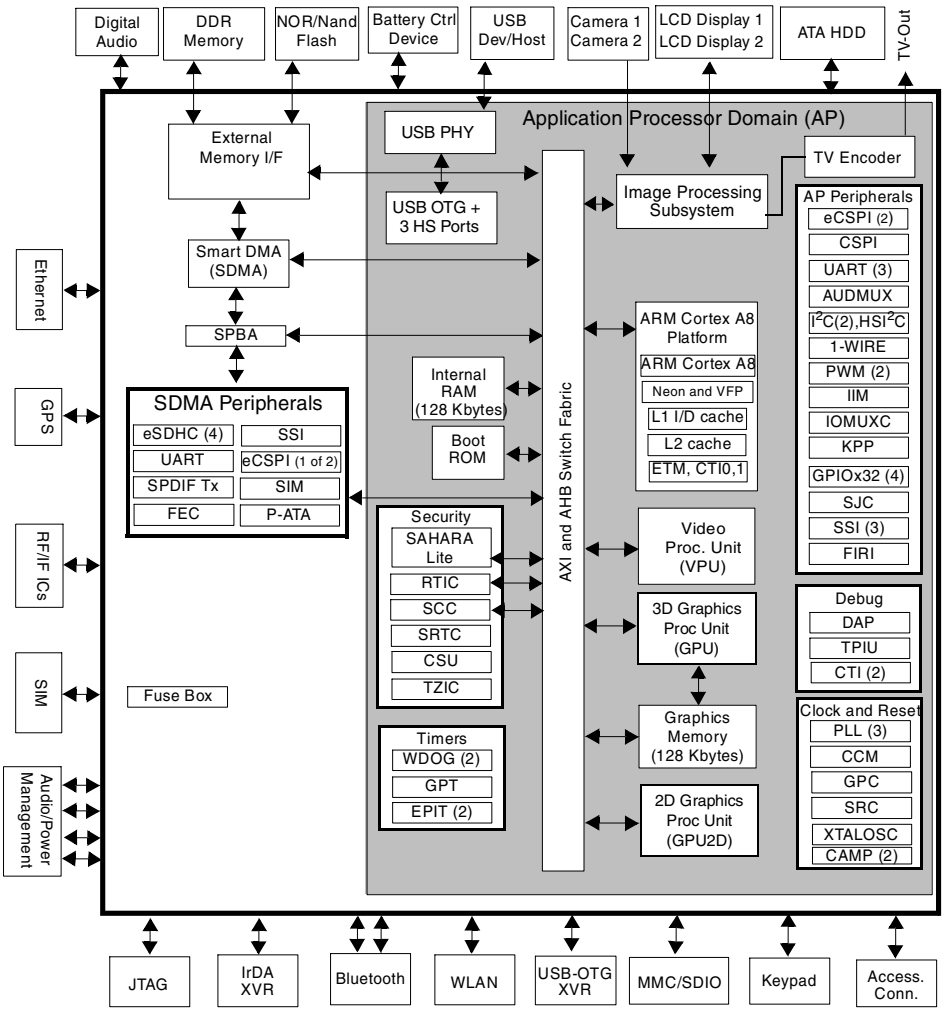

Figure 1. Functional Block Diagram

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHC-4 (muxed with P-ATA)	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	Can be configured as eSDHC (see above) and is muxed with the P-ATA interface.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
FIRI	Fast Infra-Red Interface	Connectivity Peripherals	Fast Infra-Red Interface
GPIO-1 GPIO-2 GPIO-3 GPIO-4	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing Unit	Multimedia Peripherals	The GPU provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution. It supports color representation up to 32 bits per pixel. The GPU with its 128 KByte memory enables high performance mobile 3D and 2D vector graphics at rates up to 27 Mtriangles/sec, 166 Mpixels/sec, 664 Mpixels/sec (Z).
GPU2D	Graphics Processing Unit-2D Ver. 1	Multimedia Peripherals	The GPU2D provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution.
I^2C-1 I^2C-2 HS-I^2C	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 Kbps are supported by two of the I^2C ports. Data rates of up to 3.4 Mbps (I^2C Specification v2.1) are supported by the HS-I^2C. **Note:** See the errata for the HS-I^2C in the i.MX51 Chip Errata. The two standard I^2C modules have no errata.

Table 13. i.MX51 Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies	—			V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V
NVCC_HS4_1 NVCC_HS4_2 NVCC_HS6 NVCC_HS10	HS-GPIO additional digital power supplies	1.65	—	3.1	V
NVCC_I2C	I^2C and HS-I^2C I/O Supply[7]	1.65	1.875	1.95	V
		2.7	3.0	3.3	
NVCC_SRTC_ POW	SRTC Core and I/O Supply (LVIO)	1.1	1.2	1.3	V
VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 11 and Table 126 for details. This is not a power supply.	—	—	—	—
T_C	Case Temperature (MCIMX51xD—Consumer)	–20	—	85	°C
	Case Temperature (MCIMX51xC—Industrial)	–40	—	95	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 The NVCC_IPUx rails are isolated from one another. This allows the connection of different supply voltages for each one. For example, NVCC_IPU2 can operate at 1.8 V while NVCC_IPU4 operates at 3.0 V.

4.1.2 USB PHY Current Consumption

Table 17 shows the USB PHY current consumption.

Table 17. USB PHY Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply VDDA33 (3.3 V)	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply NVCC_USBPHY (2.5 V)	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	6	7	mA
		TX	6	7	
	High Speed	RX	6	7	
		TX	6	7	
VDDA33 + NVCC_USBPHY + VCC	Suspend		50	100	µA

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX51 processor (worst-case scenario)

Table 26. LVIO I/O Output Buffer Impedance

Parameter	Symbol	Conditions	Min	Typical		Max	Unit
				OVDD 2.775 V	OVDD 1.875 V		
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 DDR2 Output Buffer Impedance

Table 27 shows the DDR2 output buffer impedance.

Table 27. DDR2 I/O Output Buffer Impedance HVE = 0

Parameter	Symbol	Test Conditions	Best Case T_j = –40 °C OVDD = 1.95 V VCC = 1.3 V	Typical T_j = 25 °C OVDD = 1.8 V VCC = 1.2 V	Worst Case T_j = 105 °C OVDD = 1.6 V VCC = 1.1 V	Unit
			s0–s5 000000	s0–s5 101010	s0–s5 111111	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength	185 92.5 61.7 26.5	140 70 47 19.5	111.4 55.7 37.2 15.4	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength	190.3 95.1 63.4 27.6	145.4 72.7 48.5 19.9	120.6 60.3 40.2 16.9	Ω

The electrical characteristics for I^2C I/O are listed in Table 31 to Table 34. Characteristics are guaranteed using operating ranges per Table 13, unless otherwise noted.

Table 31. I^2C Standard- and Fast-Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 2.7 V–3.3 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output fall time, (low driver strength)	tf	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	52	ns
Output fall time, (medium driver strength)	tf	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	28	ns

Table 32. I^2C Standard- and Fast-Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output fall time, (low driver strength)	t_{of}	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	70	ns
Output fall time, (medium driver strength)	t_{of}	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	35	ns

Table 33. I^2C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 2.7 V–3.3 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3mA external pull-up current source and C_L = 100 pF	—	—	18/21	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3mA external pull-up current source and C_L = 100 pF	—	—	9/9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	—	—	14	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	—	—	8	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	—	—	52	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	—	—	27	ns

4.5.4 AC Electrical Characteristics for DDR2

The load circuit for output pads, the output pad transition time waveform and the output pad propagation and transition time waveform are below.

Figure 10 shows the output pad transition time waveform.

Figure 10. Output Pad Transition Time Waveform

Figure 11 shows the output pad propagation and transition time waveform.

Figure 11. Output Pad Propagation and Transition Time Waveform

AC electrical characteristics in DDR2 mode for fast mode and for ovdd = 1.65 – 1.95 V, ipp_hve = 0 are placed in Table 37.

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.57/0.57 1.29/1.29	0.45/0.44 0.97/0.94	0.45/0.45 0.82/0.85	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	0.98/0.96 1.47/1.50	1.27/1.19 1.63/1.57	1.89/1.72 2.20/2.07	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	2.05/2.05 0.91/0.91	2.40/2.45 1.11/1.15	2.20/2.20 1.21/1.16	V/ns

4.7 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.7.1 CSPI Timing Parameters

This section describes the timing parameters of the CSPI. The CSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

Table 64. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	CSPI1[1], USBH1, and DI1 via IOMUX
eCSPI2	NANDF and USBH1 via IOMUX
CSPI	NANDF, USBH1, SD1, SD2, and GPIO via IOMUX

[1] This set of BGA contacts is labeled CSPI, but is actually an eCSPI channel

4.7.1.1 CSPI Master Mode Timing

Figure 38 depicts the timing of CSPI in Master mode and Table 65 lists the CSPI Master Mode timing characteristics.

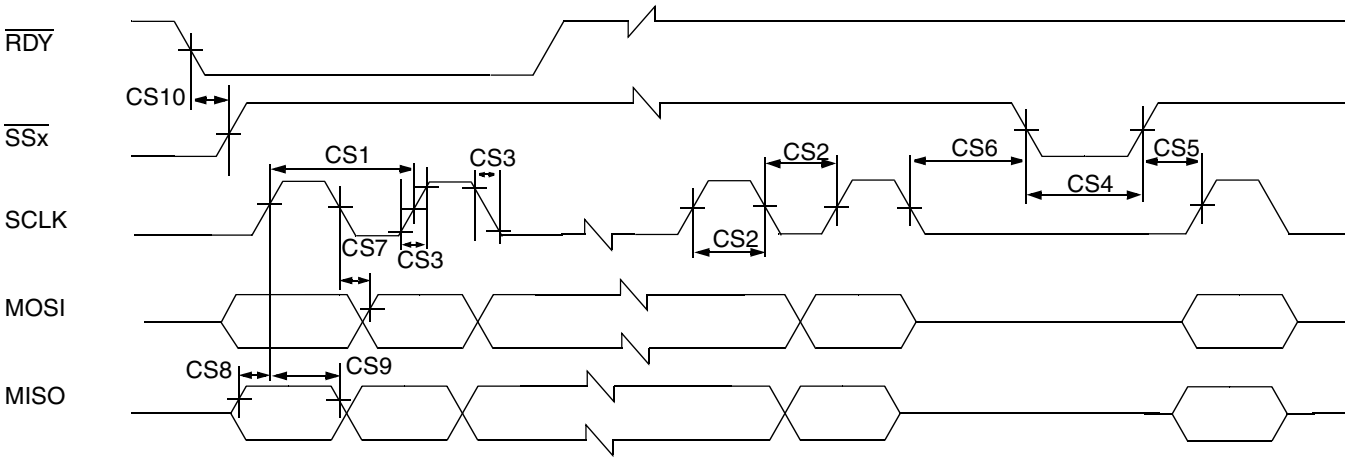

Figure 38. CSPI Master Mode Timing Diagram

Table 65. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns

4.7.6.2 High-Speed Mode Timing Parameters

Figure 48 depicts the high-speed mode timings of HS-I^{2}C module, and Table 76 lists the timing characteristics.

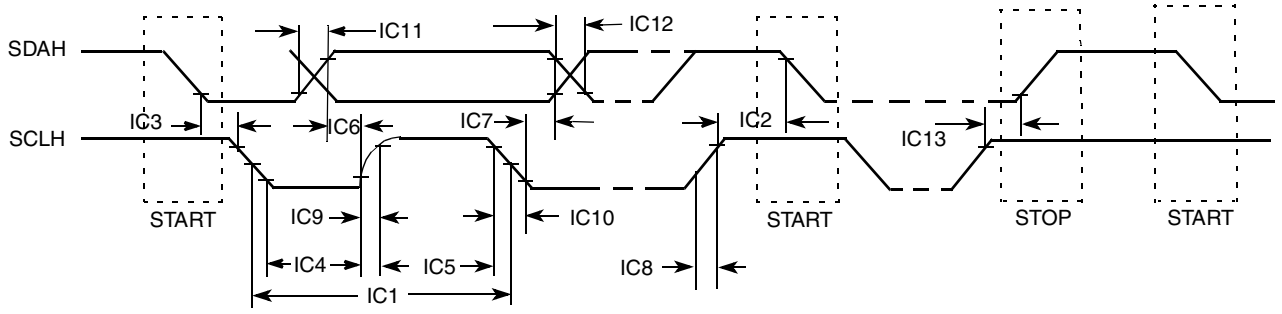

Figure 48. High-Speed Mode Timing

Table 76. HS-I^{2}C High-Speed Mode Timing Parameters

ID	Parameter	High-Speed Mode		Unit
		Min	Max	
IC1	SCLH cycle time	10	3.4	MHz
IC2	Setup time (repeated) START condition	160	—	ns
IC3	Hold time (repeated) START condition	160	—	ns
IC4	LOW Period of the SCLH Clock	160	—	ns
IC5	HIGH Period of SCLH Clock	60	—	ns
IC6	Data set-up time	10	—	ns
IC7	Data hold time	0[1]	70	ns
IC8	Rise time of SCLH	10	40	ns
IC9	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	ns
IC10	Fall time of SCLH signal	10	40	ns
IC11	Rise time of SDAH signal	10	80	ns
IC12	Fall time of SDAH signal	10	80	ns
IC13	Set-up time for STOP condition	160	—	ns
IC14	Capacitive load for each bus line (C_b)	—	100	pF

[1] A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

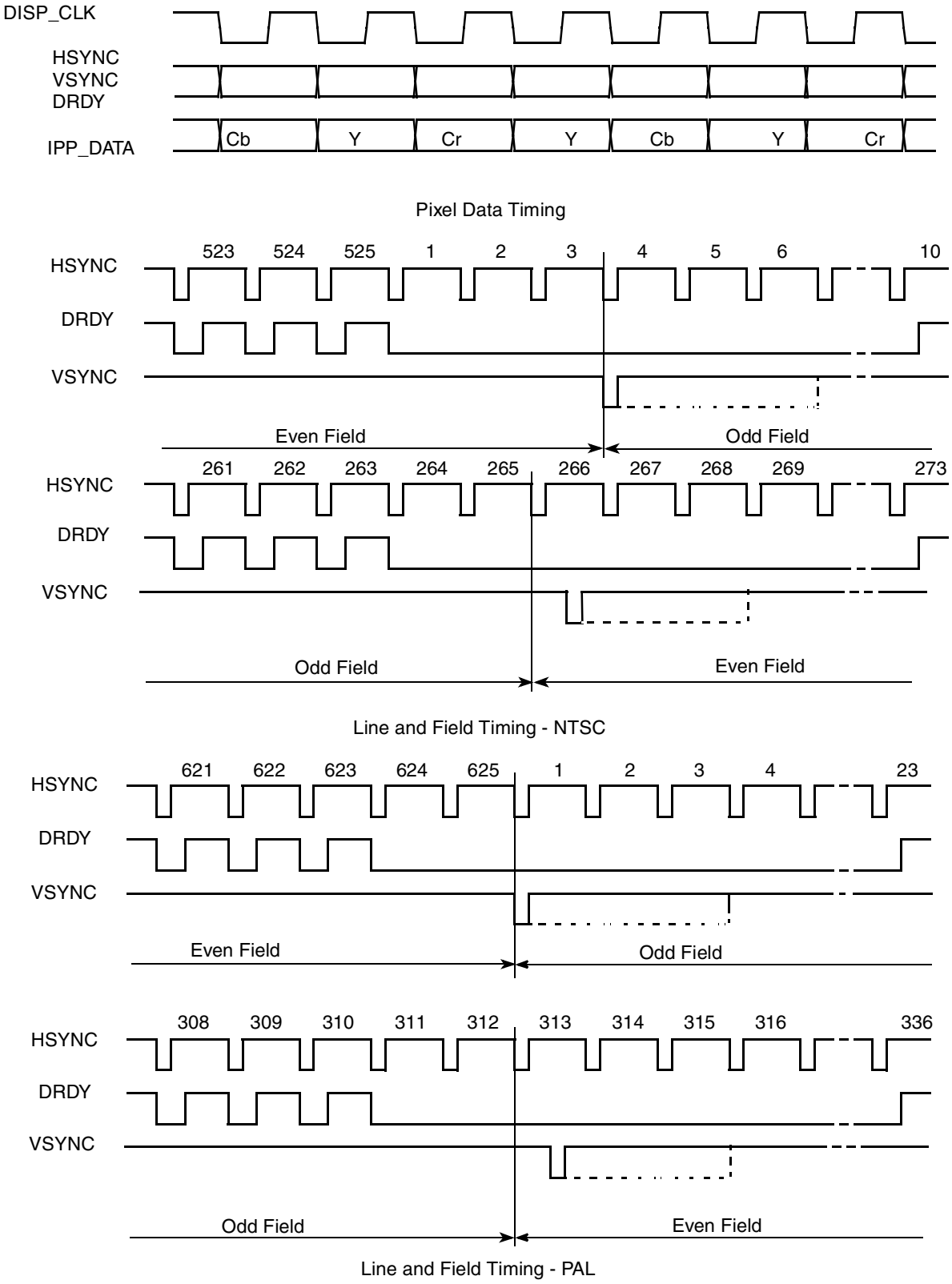

Figure 57. TV Encoder Interface Timing Diagram

Figure 70 depicts Write 1 Sequence timing, Figure 71 depicts the Read Sequence timing, and Table 88 lists the timing parameters.

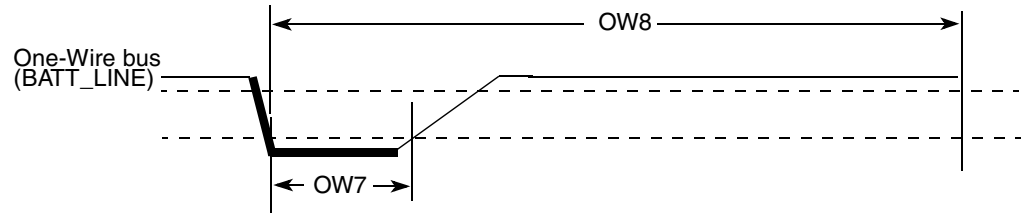

Figure 70. Write 1 Sequence Timing Diagram

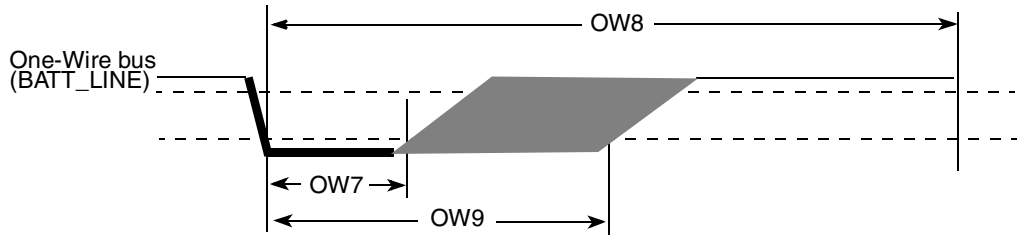

Figure 71. Read Sequence Timing Diagram

Table 88. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write /Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.7.10 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM.The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

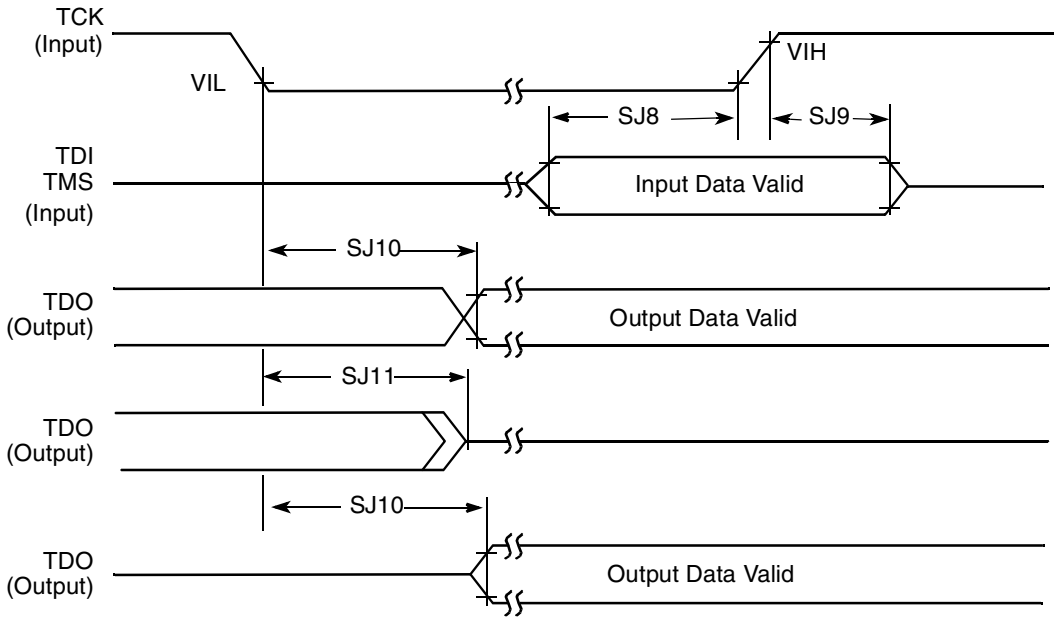

Figure 90. Test Access Port Timing Diagram

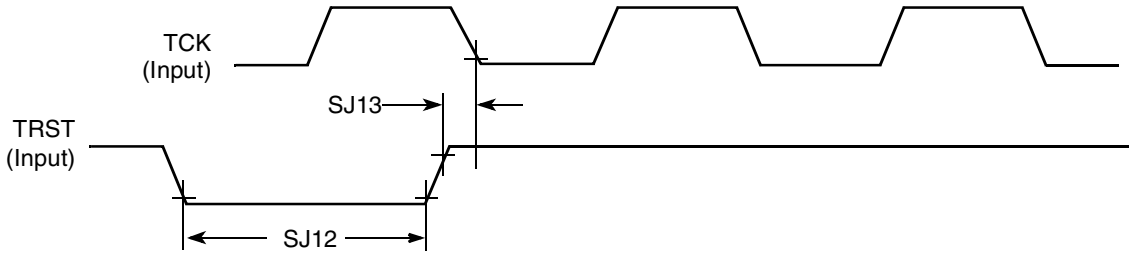

Figure 91. $\overline{\text{TRST}}$ Timing Diagram

Table 99. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 102. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	30	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- ”Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

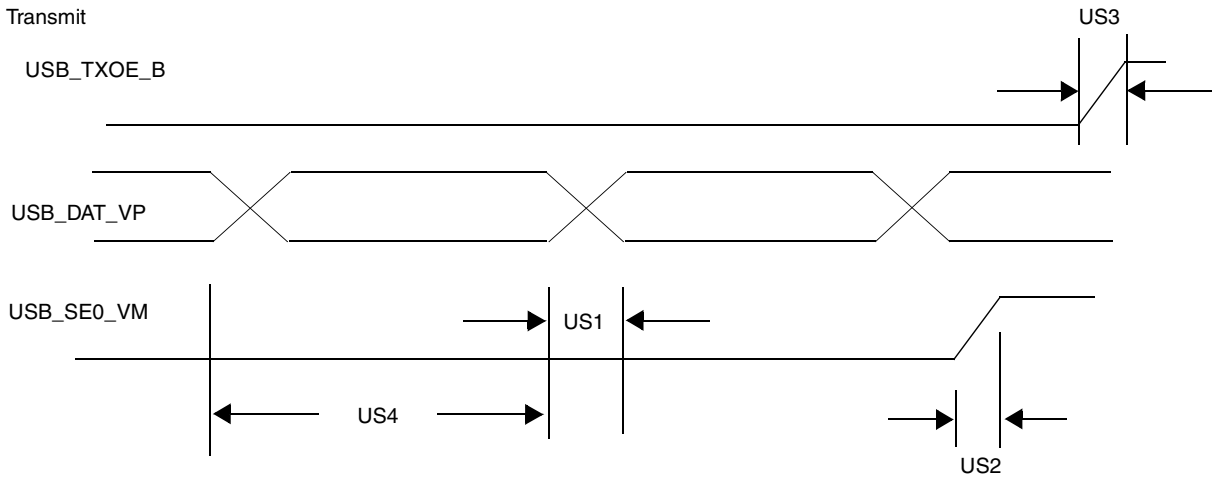

Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

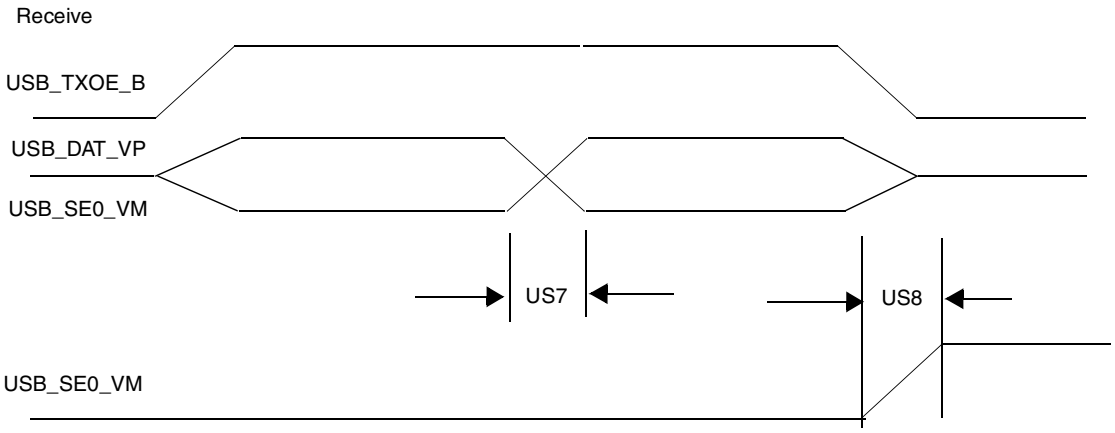

Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

5.1.1 BGA—Case 2058 13 x 13 mm, 0.5 mm Pitch

Figure 109 shows the top view, bottom view, and side view of the 13 ×13 mm package.

Figure 109. Package: Case 2058—0.5 mm Pitch

5.1.1.1 13 x 13 mm Package Drawing Notes

The following notes apply to Figure 109.

1 All dimensions in millimeters.

2 Dimensioning and tolerancing per ASME Y14.5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5 Parallelism measurement shall exclude any effect of mark on top surface of package.

5.1.2 13 x 13 mm, 0.5 Pitch Ball Assignment Lists

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name. Table 128 displays an alpha-sorted list of the signal assignments. Table 129 provides a listing of the no-connect contacts.

5.1.2.1 13 x 13 mm Ball Contact Assignments

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
AHVDDRGB	V15, V16
AHVSSRGB	V13, V14
GND	A1, A24, A25, B1, B25, E7, E13, E16, E19, G5, J13, J14, K5, K13, K14, K15, L13, L14, L15, L21, M12, M13, M14, M15, N5, N6, N8, N9, N10, N11, P8, P9, P11, P21, R8, R9, R10, R11, R12, T8, T9, T10, T11, T12, T13, U5, U9, U10, U11, U12, U13, U21, W5, AA7, AA10, AA13, AA16, AA19, AD1, AD2, AD25, AE1, AE24, AE25
GND_ANA_PLL_A	AE3
GND_ANA_PLL_B	AC25
GND_DIG_PLL_A	AE2
GND_DIG_PLL_B	AD24
NGND_OSC	AC23
NGND_TV_BACK	AB22
NGND_USBPHY	L23
NVCC_EMI	U8, V8
NVCC_EMI_DRAM	L5, M5, R5, T5, Y5, AA5
NVCC_HS10	M20
NVCC_HS4_1	L20
NVCC_HS4_2	P20
NVCC_HS6	N20
NVCC_I2C	V11
NVCC_IPU2	V20
NVCC_IPU4	N16
NVCC_IPU5	K16
NVCC_IPU6	M16

5.1.3 13 x 13 mm Ball Map

See Section 5.3, “13 × 13 mm, 0.5 Pitch Ball Map.”

5.2 19 x 19 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power/reference ID (by ball grid location) for the 19 × 19 mm, 0.8 mm pitch package.

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
CSI1_D15	M21	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D16	N22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D17	N23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D18	M22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D19	M23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D8	E18	NVCC_PER8	GPIO	Input	Keeper
CSI1_D9	A21	NVCC_PER8	GPIO	Input	Keeper
CSI1_HSYNC	A20	NVCC_PER8	GPIO	Input	Keeper
CSI1_MCLK	B20	NVCC_PER8	GPIO	Input	Keeper
CSI1_PIXCLK	F18	NVCC_PER8	GPIO	Input	Keeper
CSI1_VSYNC	G18	NVCC_PER8	GPIO	Input	Keeper
CSI2_D12	B8	NVCC_PER9	GPIO	Input	Keeper
CSI2_D13	C7	NVCC_PER9	GPIO	Input	Keeper
CSI2_D14	L20	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D15	L21	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D16	L22	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D17	L23	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D18	D9	NVCC_PER9	GPIO	Input	Keeper
CSI2_D19	A8	NVCC_PER9	GPIO	Input	Keeper
CSI2_HSYNC	C18	NVCC_PER8	GPIO	Input	Keeper
CSI2_PIXCLK	E19	NVCC_PER8	GPIO	Input	Keeper
CSI2_VSYNC	F19	NVCC_PER8	GPIO	Input	Keeper
CSPI1_MISO	C10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_MOSI	D10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_RDY	C9	NVCC_PER10	GPIO	Input	Keeper
CSPI1_SCLK	A10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS0	E10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS1	B10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
DI_GP1	H21	NVCC_IPU6	GPIO	Input	Keeper
DI_GP2	J19	NVCC_IPU6	GPIO	Input	Keeper
DI_GP3	H22	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI_GP4	J22	NVCC_IPU7	GPIO	Input	100 kΩ pull-up

Table 132. Fuse Override Contacts (continued)

Contact Name	Direction After Reset	Configuration After Reset	Signal Configuration[1]	External Termination for Fuse Override
KEY_COL4	Output	Low	Output for diagnostic signal ANY_PU_RST during power-on reset	—
KEY_COL5	Output	Low	Output for diagnostic signal JTAG_ACT during power-on reset	—

1 Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration is controlled by fuses.

2 External USB PHY selection is not functional.

3 Consider using an external 68 kΩ pull-up if system constraints indicate that the on-chip 100 kΩ pull-up is too weak.

5.2.3 19 x 19 Ball Map

See Section 5.4, “19 x 19 mm, 0.8 Pitch Ball Map.”