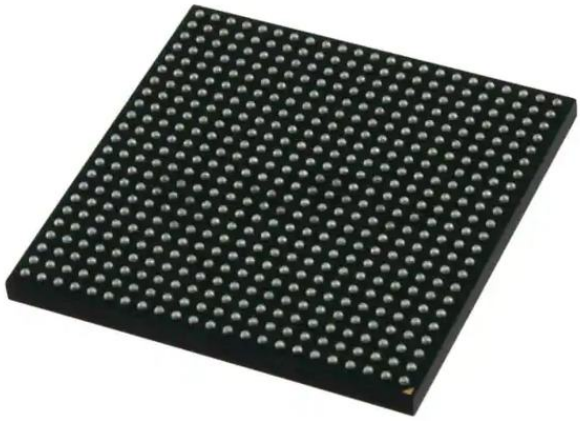

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx515djm8c

1.1 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information[1]

Part Number[2,]	Mask Set	Features	Case Temperature Range (°C)	Package[3]
MCIMX512CJM6C	M77X	No hardware video codecs No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX512DJM8C	M77X	No hardware video codecs No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513CJM6C	M77X	No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513DJM8C	M77X	No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515CJM6C	M77X	Full specification	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DJM8C	M77X	Full specification	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DVK8C	M77X	Full specification	–20 to 85	13 x 13 mm, 0.5 mm pitch BGA Case 2058

1 For Junction Temperature (Tj) maximum ratings, see Table 11, "Absolute Maximum Ratings," on page 18.

2 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon ( )

3 Case 2017 and Case 2058 are RoHS compliant, lead-free, MSL = 3.

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	IPU enables connectivity to displays and image sensors, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces. • Legacy Interfaces • Analog TV interfaces (through a TV encoder bridge) The processing includes: • Support for camera control • Image enhancement: color adjustment and gamut mapping, gamma correction and contrast enhancement, sharpening and noise reduction • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Synchronization and control capabilities, allowing autonomous operation. • Hardware de-interlacing support
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
P-ATA (Muxed with eSDHC-4	Parallel ATA	Connectivity Peripherals	The P-ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA-5 (UDMA-4) compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. This is muxed with eSDHC-4 interfaces.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	Unified RAM, can be split between Secure RAM and Non-Secure RAM
ROM 36 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes

Table 16. i.MX51 Stop Mode Current and Power Consumption (continued)

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled. USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow T_A = 25°C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	0.012	
		Total	1.09	mW
Stop Mode • External reference clocks enabled • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.20 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	1.5	
		Total	4.8	mW
Stop Mode • External reference clocks enabled • No power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	50	mA
		VCC	2	
		VDDA	1.15	
		NVCC_OSC	1.5	
		Total	63	mW

4.6.7.3 General WEIM Timing-Synchronous Mode

Figure 20, Figure 21, and Table 53 specify the timings related to the WEIM module. All WEIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

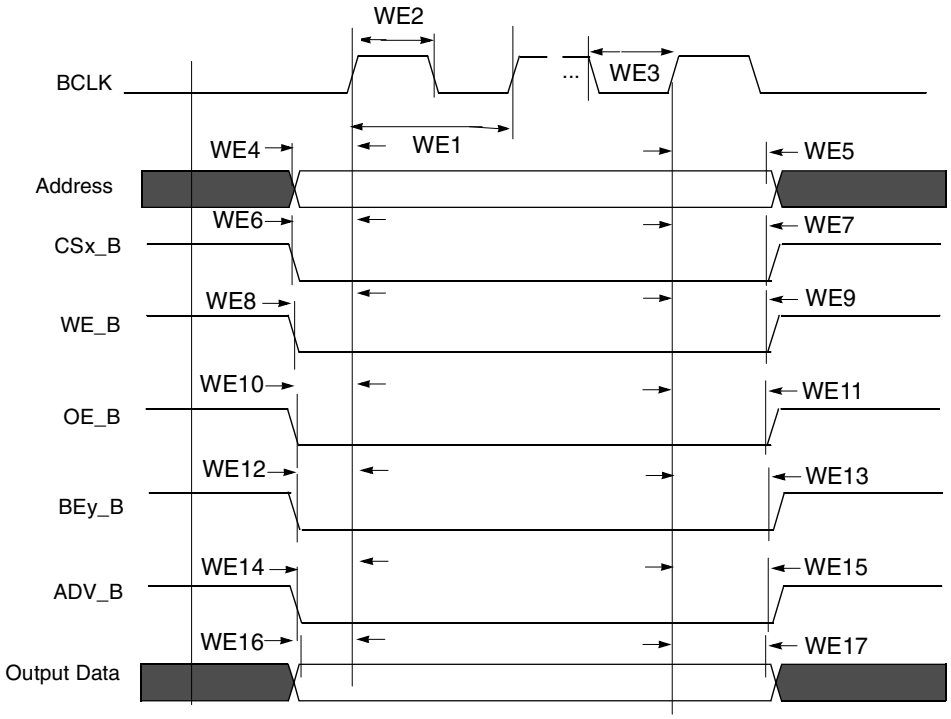

Figure 20. WEIM Outputs Timing Diagram

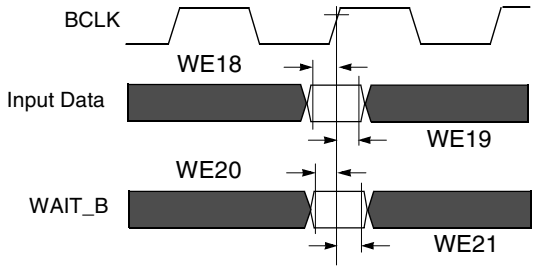

Figure 21. WEIM Inputs Timing Diagram

Table 53. WEIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t		2 x t		3 x t		4 x t	
WE2	BCLK Low Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 53.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

Table 67. eCSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.7.2.2 eCSPI Slave Mode Timing

Figure 41 depicts the timing of eCSPI in Slave mode and Table 68 lists the eCSPI Slave Mode timing characteristics.

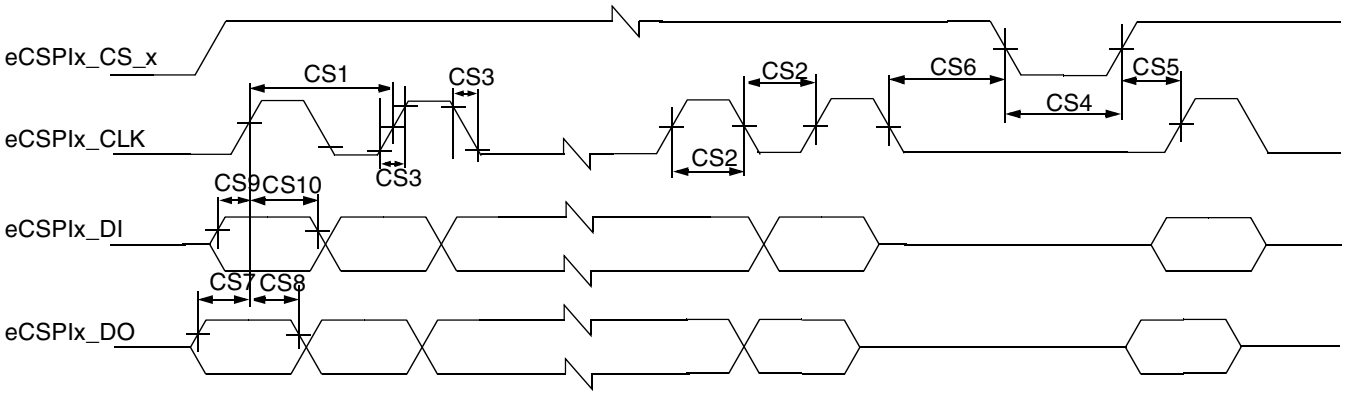

Figure 41. eCSPI Slave Mode Timing Diagram

Table 68. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: display processing, image conversions, and other related functions.
- Synchronization and control capabilities such as avoidance of tearing artifacts.

4.7.8.1 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.1.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.1.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 50.

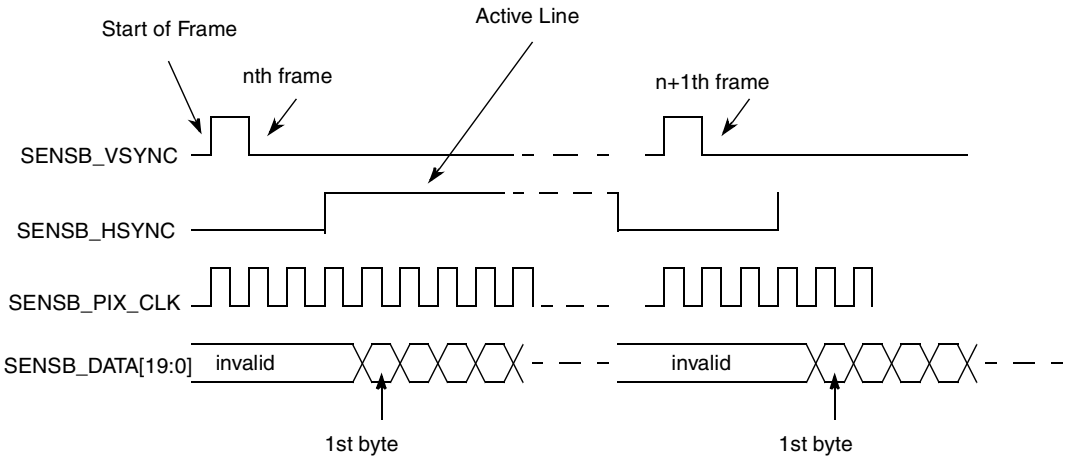

Figure 50. Gated Clock Mode Timing Diagram

Table 79. Video Signal Cross-Reference

i.MX51	LCD								Comment[1]
Port Name (x=1,2)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24-bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

Table 85. Asynchronous Serial Interface Timing Characteristics (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]-Tdicur-1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5	—	Tdicpr-Tdicdr-1.5	ns
IP60	Write data setup time	Tds	Tdicdw-1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns
IP69	Clock offset[11]	Toclk	Toclk-1.5	Toclk	Toclk+1.5	ns
IP70	RS up time[12]	Tdicurs	Tdicurs–1.5	Tdicurs	Tdicurs+1.5	ns
IP71	RS down time[13]	Tdicdrs	Tdicdrs -1.5	Tdicdrs	Tdicdrs+1.5	ns
IP72	CS up time[14]	Tdicucs	Tdicucs –1.5	Tdicucs	Tdicucs+1.5	ns
IP73	CS down time[15]	Tdicdcs	Tdicdcs –1.5	Tdicdcs	Tdicdcs+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display interface clock period value for read

$$Tdicpr = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_RD}{DI\_CLK\_PERIOD}\right]$$

[3]Display interface clock period value for write

$$Tdicpw = T_{DI\_CLK} \times ceil\left[\frac{DISP\#\_IF\_CLK\_PER\_WR}{DI\_CLK\_PERIOD}\right]$$

4.7.11.1 PIO Mode Read Timing

Figure 74 shows timing for PIO read and Table 92 lists the timing parameters for PIO read.

Figure 74. PIO Read Timing Diagram

Table 92. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 74	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)×T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

Table 94. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.11.2 Ultra DMA (UDMA) Input Timing

Figure 78 shows timing when the UDMA in transfer starts, Figure 79 shows timing when the UDMA in host terminates transfer, Figure 80 shows timing when the UDMA in device terminates transfer, and Table 95 lists the timing parameters for UDMA in burst.

Figure 78. UDMA In Transfer Starts Timing Diagram

Figure 79. UDMA In Host Terminates Transfer Timing Diagram

Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

[2] Make ton and toff big enough to avoid bus contention.

4.7.12 SIM (Subscriber Identification Module) Timing

This section describes the electrical parameters of the SIM module. Each SIM module interface consists of 12 signals (two separate ports each containing six signals). Typically a a port uses five signals.

The interface is designed to be used with synchronous SIM cards meaning the SIM module provides the clock used by the SIM card. The clock frequency is typically 372 times the Tx/Rxdata rate, however the SIM module can work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data in the same manner as standard UART data exchanges. All six signals (5 for bi-directional Tx/Rx) of the SIM module are asynchronous to each other.

There are no required timing relationships between signals in normal mode. The SIM card is initiated by the interface device; the SIM card responds with Answer to Reset. Although the SIM interface has no defined requirements, the ISO-7816 defines reset and power-down sequences. (For detailed information, see ISO-7816.)

Table 97 defines the general timing requirements for the SIM interface.

Table 97. SIM Timing Parameters, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI1	SIM Clock Frequency (SIMx_CLKy)[1],	S_{freq}	0.01	25	MHz
SI2	SIM Clock Rise Time (SIMx_CLKy)[2]	S_{rise}	—	$0.09\times(1/S_{freq})$	ns
SI3	SIM Clock Fall Time (SIMx_CLKy)[3]	S_{fall}	—	$0.09\times(1/S_{freq})$	ns
SI4	SIM Input Transition Time (SIMx_DATAy_RX_TX, SIMx_SIMPDy)	S_{trans}	10	25	ns
SI5	SIM I/O Rise Time / Fall Time(SIMx_DATAy_RX_TX)[4]	Tr/Tf	—	1	µs
SI6	SIM RST Rise Time / Fall Time(SIMx_RSTy)[5]	Tr/Tf	—	1	µs

1 50% duty cycle clock

2 With C = 50 pF

3 With C = 50 pF

4 With Cin = 30 pF, Cout = 30 pF

5 With Cin = 30 pF

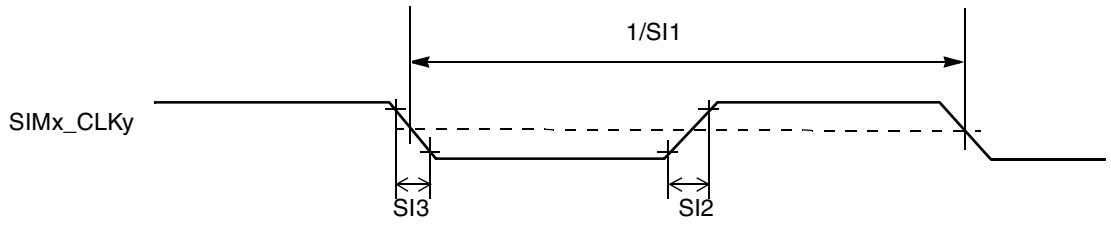

Figure 84. SIM Clock Timing Diagram

4.7.16.1.1 UART RS-232 Serial Mode Timing

UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 107 lists the UART RS-232 serial mode transmit timing characteristics.

Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 107. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1]$-T_{ref\_clk}$[2]	$1/F_{baud\_rate}+T_{ref\_clk}$	—

[1] $1/F_{baud\_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists serial mode receive timing characteristics.

Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 108. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2]$-1/(16\times F_{baud\_rate})$	$1/F_{baud\_rate}+1/(16\times F_{baud\_rate})$	—

[1] The UART receiver can tolerate 1/(16×Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16×Fbaud_rate).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.7.16.1.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
VDDA	H13, N18, R6, T6, Y16
VDDA33	R16
VDDGP	E10, J9, J10, J11, J12, K8, K9, K10, K11, K12, L6, L8, L9, L10, L11, L12, M6, M8, M9, M10
VREF	U6
VREFOUT	AB20
VREG	L24

5.1.2.2 13 x 13 mm Signal Assignments, Power Rails, and I/O

Table 128 shows signal assignment connect list including the associated power supplies. Table 132 lists the contacts that can be overridden with fuse settings.

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
AUD3_BB_CK	C9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_FS	C8	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_RXD	B8	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_TXD	B7	NVCC_PER9	GPIO	Input	Keeper
BOOT_MODE0	W22	NVCC_PER3	LVIO	Input	100 kΩ pull-up
BOOT_MODE1	AA24	NVCC_PER3	LVIO	Input	100 kΩ pull-up
CKIH1	AB24	NVCC_PER3	Analog	Input	Analog
CKIH2	AA23	NVCC_PER3	Analog	Input	Analog
CKIL	AA22	NVCC_SRTC_POW	GPIO	Input	Standard CMOS
CLK_SS	Y22	NVCC_PER3	LVIO	Input	100 kΩ pull-up
COMP[2]	AC20	AHVDDRGB	Analog	Input	Analog
CSI1_D10	R24	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D11	R25	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D12	P22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D13	P23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D14	P24	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D15	P25	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D16	N24	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D17	N25	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D18	N23	NVCC_HS10	HSGPIO	Input	Keeper

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D5	A5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	C6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	E7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	D4	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	B3	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	E2	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	E1	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	D1	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	E14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AA16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	W16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AA17	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	Y15	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	U20	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	Y21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A17	NVCC_PER15	UHVIO	Output	—
SD1_CMD	E16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	D16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	A18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	F17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	A19	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	B18	NVCC_PER17	UHVIO	Output	—
SD2_CMD	G17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	E17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B19	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	D17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	C17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down

Table 133. 13 × 13 mm, 0.5 mm Pitch Ball Map (continued)

	P	N	M	L	K	J	H	
1	DRAM_A9	DRAM_SDCKE0	DRAM_SDCLK	DRAM_SDCKE1	DRAM_SDQS3_B	DRAM_D25	DRAM_D27	1
2	DRAM_A12	DRAM_DQM3	DRAM_SDCLK_B	EIM_SDODT0	DRAM_SDQS3	DRAM_D26	DRAM_D28	2
3	DRAM_CS0	DRAM_RAS	DRAM_SDWE	EIM_SDODT1	DRAM_SDQS2	DRAM_D22	DRAM_D20	3
4	EIM_SDBA0	DRAM_CAS	DRAM_DQM2	EIM_SDBA1	DRAM_SDQS2_B	DRAM_D24	DRAM_D23	4
5	—	GND	NVCC_EMI_DRAM	NVCC_EMI_DRAM	GND	—	—	5
6	VDD_FUSE	GND	VDDGP	VDDGP	EIM_SDBA2	NANDF_D15	NANDF_D9	6
7	—	—	—	—	—	—	—	7
8	GND	GND	VDDGP	VDDGP	VDDGP	NVCC_NANDF_A	NVCC_NANDF_B	8
9	GND	GND	VDDGP	VDDGP	VDDGP	VDDGP	NVCC_NANDF_C	9
10	SGND	GND	VDDGP	VDDGP	VDDGP	VDDGP	NVCC_PER9	10
11	GND	GND	SVDDGP	VDDGP	VDDGP	VDDGP	NVCC_PER11	11
12	VCC	VCC	GND	VDDGP	VDDGP	VDDGP	NVCC_PER10	12
13	VCC	SVCC	GND	GND	GND	GND	VDDA	13
14	VCC	VCC	GND	GND	GND	GND	NVCC_PER13	14
15	VCC	VCC	GND	GND	GND	NVCC_PER8	NVCC_PER12	15
16	NVCC_USBPHY	NVCC_IPU4	NVCC_IPU6	NVCC_IPU9	NVCC_IPU5	NVCC_PER17	NVCC_PER15	16
17	—	—	—	—	—	—	—	17
18	DISP2_DAT1	VDDA	DISP2_DAT12	DISP2_DAT8	RREFEXT	DI1_PIN2	GPIO1_0	18
19	—	—	—	—	—	—	—	19
20	NVCC_HS4_2	NVCC_HS6	NVCC_HS10	NVCC_HS4_1	DI_GP2	CSI2_HSYNC	DI1_PIN3	20
21	GND	—	—	GND	—	—	—	21
22	CSI1_D12	CSI1_D19	CSI2_D17	VBUS	GPANAIO	DI1_DISP_CLK	NVCC_IPU7	22
23	CSI1_D13	CSI1_D18	CSI2_D16	NGND_USBPHY	DI_GP4	DI2_PIN4	DI_GP3	23
24	CSI1_D14	CSI1_D16	CSI2_D15	VREG	DP	DI2_DISP_CLK	DI2_PIN2	24
25	CSI1_D15	CSI1_D17	CSI2_D14	ID	DN	DI2_PIN3	DISP1_DAT23	25
	P	N	M	L	K	J	H	

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	05/2010	• Updated CaseTemperature Range column in Table 1, "Ordering Information," on page 3. • Changed the VREFOUT column in Table 3, "Special Signal Considerations," on page 12. • Added Section 3, “IOMUX Configuration for Boot Media”. • Updated Figure 2, "Power-Up Sequence," on page 24. • Updated the Minimum and Maximum columns in Table 13, "i.MX51 Operating Ranges," on page 19. • Added a note in Section 4.2.1, “Power-Up Sequence”. • Updated Section 4.2.1, “Power-Up Sequence.” • Changed the Input current (47 kΩ Pull-up) column in Table 21, "UHVIO DC Electrical Characteristics," on page 27 to Input current (75 kO Pull-up). • Added new table for parameters for DDR2 Pad output buffer Impedance. See Table 27, "DDR2 I/O Output Buffer Impedance HVE = 0," on page 32. • Added new section under Section 4.5, “I/O AC Parameters”. See Section 4.5.4, “AC Electrical Characteristics for DDR2”. • Updated Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. In the VIH (for square wave input) parameter, the minimum frequency was changed to NVCC_PER3 - 0.25V and the maximum frequency was changed to NVCC_PER3. • Added a note in Section 4.6.6, “NAND Flash Controller (NFC) Parameters” after Table 49. • Updated Asymmetric Mode Min, Symmetric Mode Min, and Max columns of Table 50. • Removed Conditions parameters of the Full scale output voltage row in Table 82. • Updated Section 4.7.11, “P-ATA Timing Parameters”. Replaced ATA/ATAPI-6 specification with ATA/ATAPI-5 specification. • In Table 102, "SSI Transmitter Timing with Internal Clock," on page 135, under the Synchronous Internal Clock Operation sections for the ID SS42, minimum frequency was changed from 10.0 to 30. • In Table 103, "SSI Receiver Timing with Internal Clock," on page 136, under the Internal Clock Operation section for ID SS20, minimum frequency was changed from 10.0 to 30. • In Table 104, "SSI Transmitter Timing with External Clock," on page 138, under the External Clock Operation section for ID SS38, maximum frequency was changed from 15.0 to 30. • Added a new section Section 4.7.16.1, “UART Electrical”, under Section 4.7.16, “UART”. • In Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148, for IDs SS28 and SS29, direction was changed from out to in. • In Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150, for IDs US40 and US41, direction was changed from out to in and the reference signal was changed to USB_VM1 and USB_VP1 respectively. • In Table 122, "USB Timing Specification for ULPI Parallel Mode," on page 151, added an extra row for ID17. • Updated Signal and Direction columns in Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150. • Updated Signal names in Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148.
Rev. 1	10/2009	Initial public release.