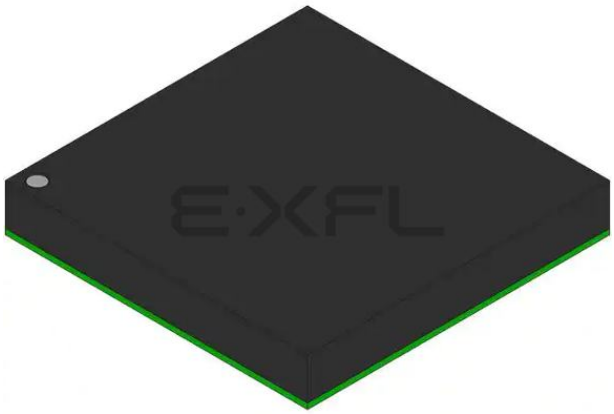

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx515djm8cr2

2 Features

The i.MX51 processor contains a large number of digital and analog modules that are described in Table 2.

Table 2. i.MX51 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity Peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM Cortex™-A8	ARM Cortex™-A8 Platform	ARM	The ARM Cortex™-A8 Core Platform consists of the ARM Cortex™-A8 processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the Level 2 Cache Controller, 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, and a 256 Kbyte L2 cache. The platform also contains an Event Monitor and Debug modules. It also has a NEON co-processor with SIMD media processing architecture, register file with 32 × 64-bit general-purpose registers, an Integer execute pipeline (ALU, Shift, MAC), dual, single-precision floating point execute pipeline (FADD, FMUL), load/store and permute pipeline and a Non-Pipelined Vector Floating Point (VFP) co-processor (VFPv3).
Audio Subsystem	Audio Subsystem	Multimedia Peripherals	The elements of the audio subsystem are three Synchronous Serial Interfaces (SSI1-3), a Digital Audio Mux (AUDMUX), and Digital Audio Out (SPDIF TX). See the specific interface listings in this table.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The modules include three PLLs and a Frequency Pre-Multiplier (FPM).
CSPI-1, eCSPI-2 eCSPI-3	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX51 platform, and for sharing security information between the various security modules. The Security Control Registers (SCR) of the CSU are set during boot time by the High Assurance Boot (HAB) code and are locked to prevent further writing.
Debug System	Debug System	System Control	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, cross-system triggers, counters, and sequencers.

4.3.7 USB Port Electrical DC Characteristics

Table 23 and Table 24 list the electrical DC characteristics.

Table 23. USBOTG Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	VDD x 0.7	VDD	V	—
Input low Voltage	VIL	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	0	VDD × 0.3	V	—
Output High Voltage	VOH	USB_VPOUT USB_VMOUT USB_TXENB	VDD – 0.43	—	V	7 mA Drv at IOH = 5 mA
Output Low Voltage	VOL	USB_VPOUT USB_VMOUT USB_TXENB	—	0.43	V	7 mA Drv at IOH = 5 mA

Table 24. USB Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	VDD x 0.7	VDD	V	—
Input Low Voltage	VIL	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	0	VDD x 0.3	V	—
Output High Voltage	VOH	USB_DAT_VP USB_SE0_VM USB_TXOE_B	VDD –0.43	—	V	7 mA Drv at Iout = 5 mA
Output Low Voltage	VOL	USB_DAT_VP USB_SE0_VM USB_TXOE_B	—	0.43	V	7 mA Drv at Iout = 5 mA

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt[1]	di/dt	—	390	201	99	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Slow mode and for ovdd=1.65 – 1.95 V, ipp_hve = 0 are placed in Table 38:

Table 38. AC Electrical Characteristics of DDR2 IO Pads for Slow Mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.75/0.76 1.39/1.40	0.70/0.74 1.18/1.21	1.06/1.00 1.49/1.47	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.50/1.55 2.05/2.16	1.90/1.95 2.36/2.48	3.23/3.10 3.82/3.75	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	1.56/1.54 0.84/0.84	1.54/1.46 0.92/0.89	0.93/0.99 0.66/0.67	V/ns
Output Pad di/dt[1]	di/dt	—	82	40	19	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

Figure 33 shows the timing diagram for mDDR SDRAM write cycle. The timing parameters for this diagram is shown in Table 56.

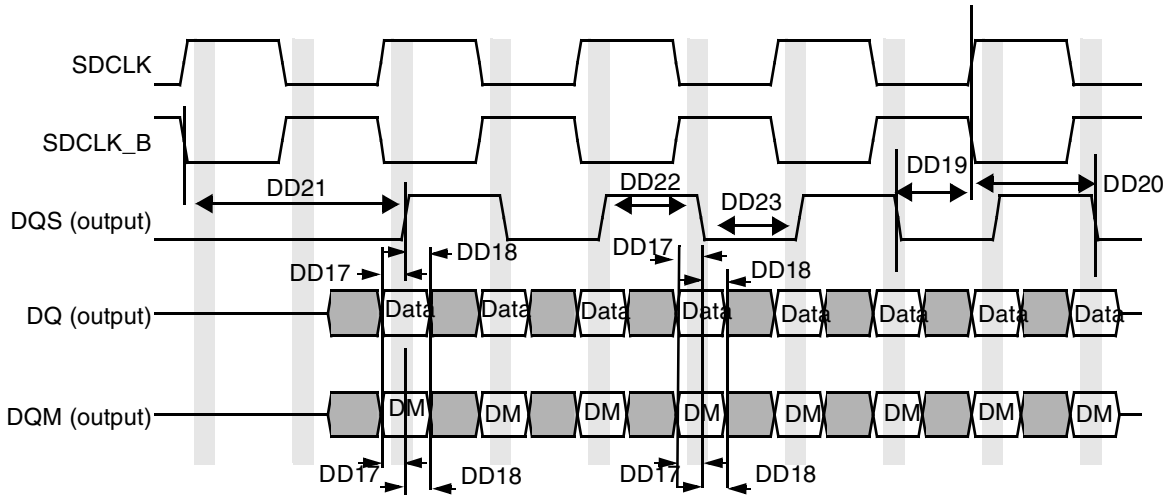

Figure 33. mDDR SDRAM Write cycle Timing Diagram

Table 56. mDDR SDRAM Write Cycle Parameter Table[1]

ID	Parameter	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD17	DQ and DQM setup time to DQS	t_{DS}[3]	0.48	—	0.6	—	0.8	—	ns
DD18	DQ and DQM hold time to DQS	t_{DH}[1]	0.48	—	0.6	—	0.8	—	ns
DD19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.2	—	0.2	—	0.2	—	tCK
DD20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.2	—	0.2	—	0.2	—	tCK
DD21	Write command to first DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DD22	DQS high level width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DD23	DQS low level width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	tCK

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

3 This parameter is affected by pad timing. If the slew rate is < 1 V/ns, 0.1 ns should be increased to this value.

Table 58. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}[1]	1.7	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

[1] These values are for command/address slew rates of 1 V/ns and SDCLK / SDCLK_B differential slew rate of 2 V/ns. For different values use the settings shown in Table 59.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 59. Derating Values for DDR2-400 (SDCLK = 200 MHz)

Command / Address Slew Rate (V/ns)	SDCLK Differential Slew Rates[1,2]						Unit
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	+0	+0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

Table 69. eSDHCv2 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time	t_{IH}[5]	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 Measurement taken with CLoad = 20 pF

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps-only 7-wire interface, which uses 7 of the MII pins, for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).

This section describes the AC timing specifications of the FEC.

4.7.4.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 70 lists the MII receive channel signal timing parameters and Figure 43 shows MII receive signal timings.

Table 70. MII Receive Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

1 FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.7.8.1.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.7.8.1.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 51. All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

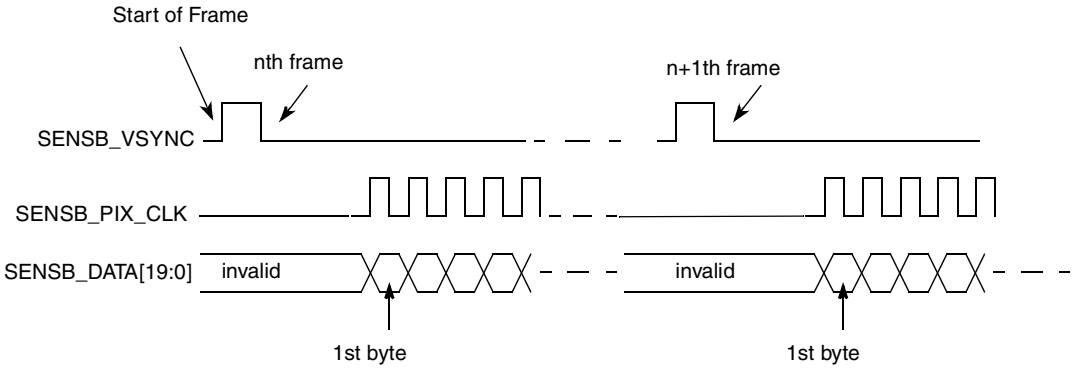

Figure 51. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 51 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.8.2 Electrical Characteristics

Figure 52 shows the sensor interface timing diagram. SENSB_PIX_CLK signal described here is not generated by the IPU. Table 78 shows the timing characteristics for the diagram shown in Figure 52.

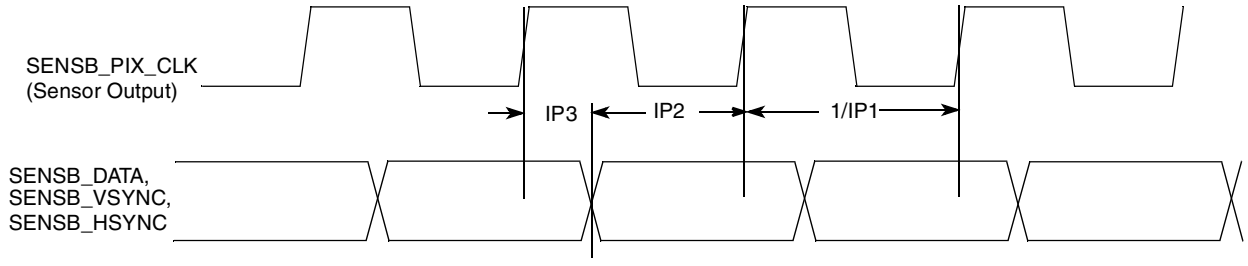

Figure 52. Sensor Interface Timing Diagram

Table 78. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	120	MHz
IP2	Data and control setup time	Tsu	3	—	ns
IP3	Data and control holdup time	Thd	2	—	ns

4.7.8.3 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 79 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 79. Video Signal Cross-Reference

i.MX51	LCD								Comment[1]
Port Name (x=1,2)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24-bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on base of an internal generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point.

4.7.8.5.2 LCD Interface Functional Description

Figure 53 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (For DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

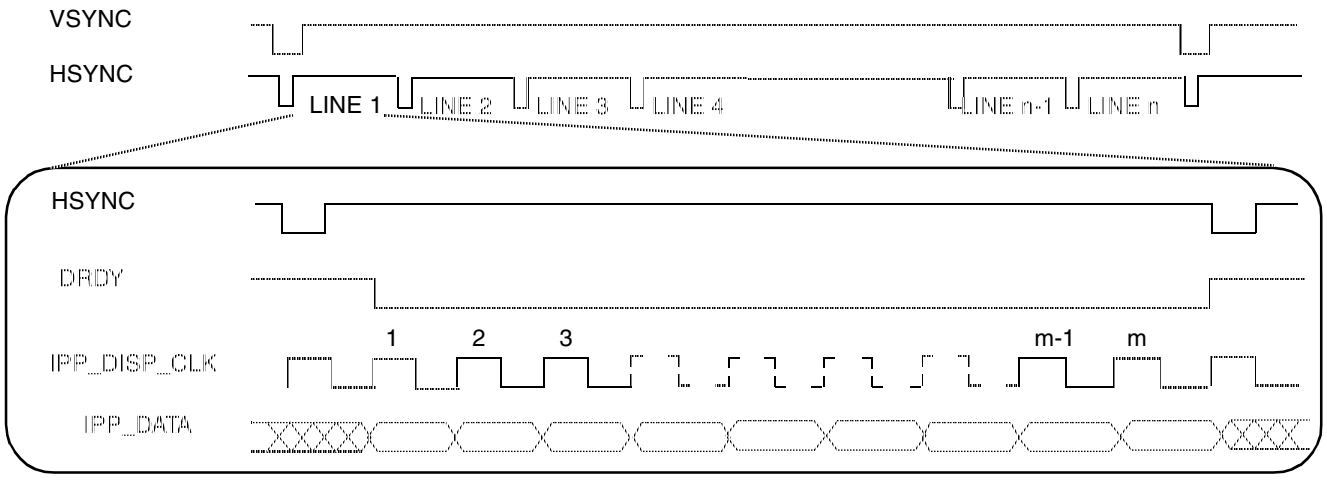

Figure 53. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.5.3 TFT Panel Sync Pulse Timing Diagrams

Figure 54 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All shown on the figure parameters are programmable. All controls are started by corresponding

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

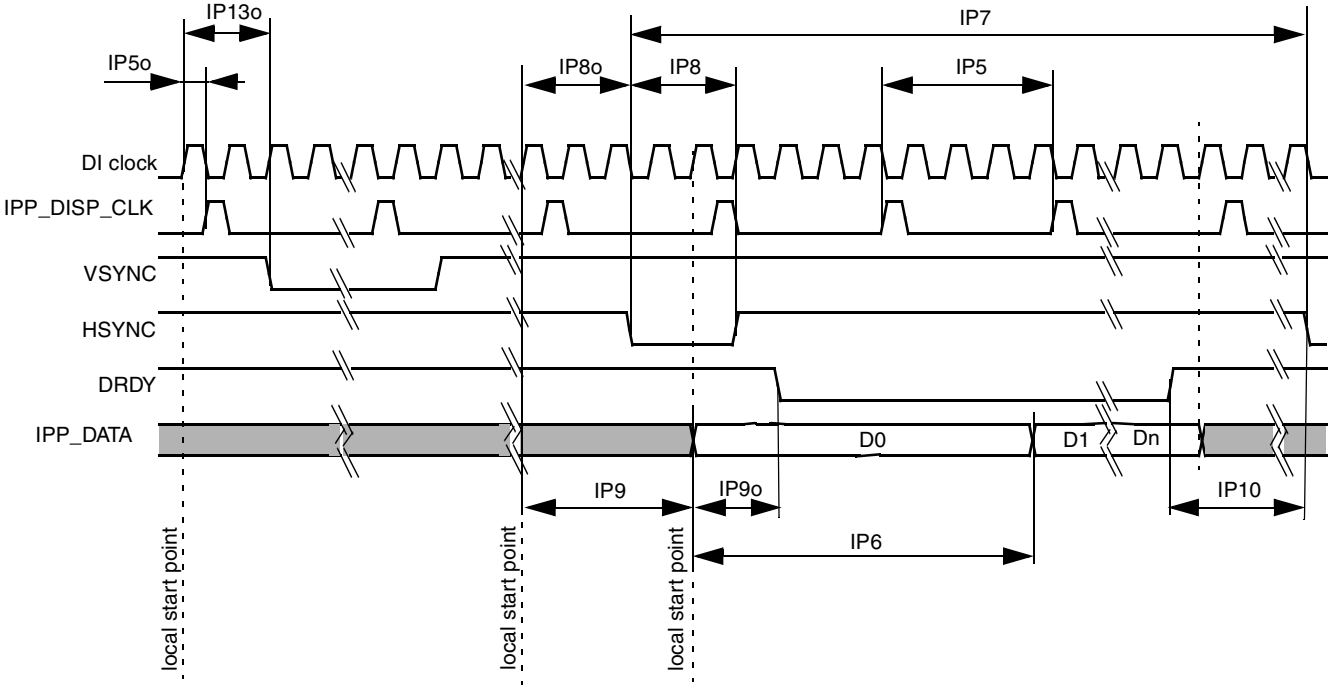

Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

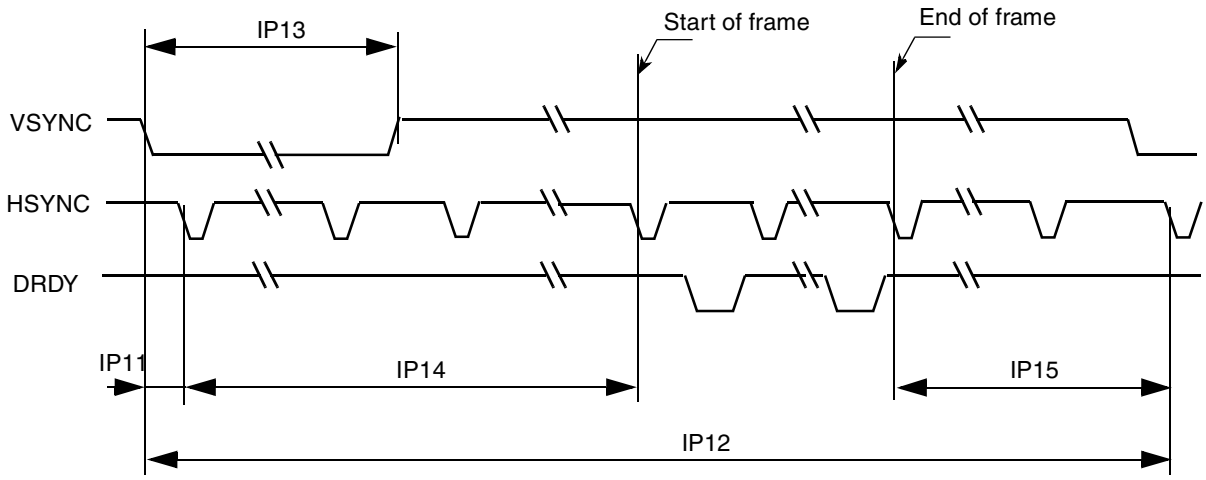

Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

4.7.11.1 PIO Mode Read Timing

Figure 74 shows timing for PIO read and Table 92 lists the timing parameters for PIO read.

Figure 74. PIO Read Timing Diagram

Table 92. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 74	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)×T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

Figure 76 shows timing for MDMA read, Figure 77 shows timing for MDMA write, and Table 94 lists the timing parameters for MDMA read and write.

Figure 76. MDMA Read Timing Diagram

Figure 77. MDMA Write Timing Diagram

Table 94. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)×T – (tsu + tco + 2×tbuf + 2×tcable2)	time_d, time_k

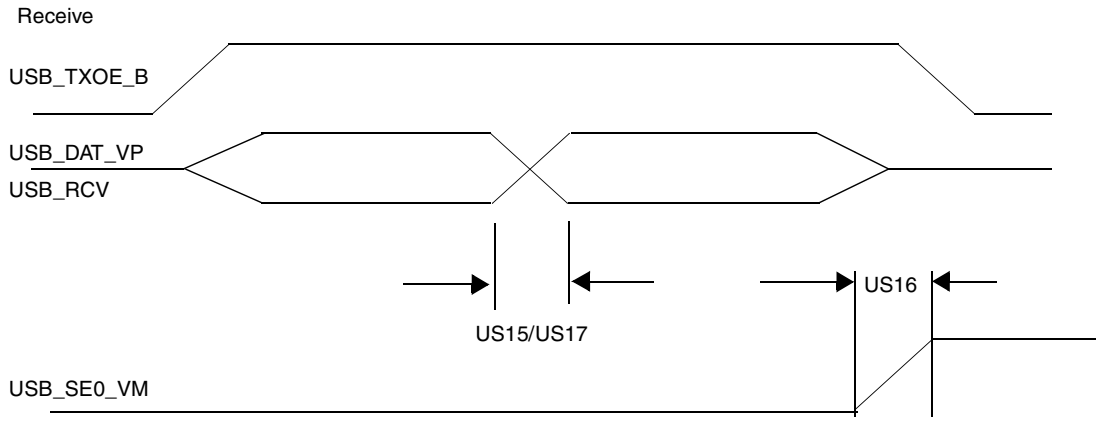

Figure 103. USB Receive Waveform in DAT_SE0 Uni-directional Mode

Table 116 shows the USB port timing specification in DAT_SE0 uni-directional mode.

Table 116. USB Port Timing Specification in DAT_SE0 Uni-Directional Mode

ID	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition/ Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US17	RX Rise/Fall Time	USB_RCV	In	—	3.0	ns	35 pF

4.7.17.1.3 USB VP_VM Bi-Directional Mode

Table 117 shows the signal definitions in VP_VM bi-directional mode. Figure 104 and Figure 105 shows the USB transmit/receive waveform in VP_VM bi-directional mode respectively.

Table 117. Signal Definitions—VP_VM Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	TX VP data when USB_TXOE_B is low RX VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	TX VM data when USB_TXOE_B low RX VM data when USB_TXOE_B high
USB_RCV	In	Differential RX data

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5 Parallelism measurement shall exclude any effect of mark on top surface of package.

5.1.2 13 x 13 mm, 0.5 Pitch Ball Assignment Lists

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name. Table 128 displays an alpha-sorted list of the signal assignments. Table 129 provides a listing of the no-connect contacts.

5.1.2.1 13 x 13 mm Ball Contact Assignments

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 127. 13 x 13 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
AHVDDRGB	V15, V16
AHVSSRGB	V13, V14
GND	A1, A24, A25, B1, B25, E7, E13, E16, E19, G5, J13, J14, K5, K13, K14, K15, L13, L14, L15, L21, M12, M13, M14, M15, N5, N6, N8, N9, N10, N11, P8, P9, P11, P21, R8, R9, R10, R11, R12, T8, T9, T10, T11, T12, T13, U5, U9, U10, U11, U12, U13, U21, W5, AA7, AA10, AA13, AA16, AA19, AD1, AD2, AD25, AE1, AE24, AE25
GND_ANA_PLL_A	AE3
GND_ANA_PLL_B	AC25
GND_DIG_PLL_A	AE2
GND_DIG_PLL_B	AD24
NGND_OSC	AC23
NGND_TV_BACK	AB22
NGND_USBPHY	L23
NVCC_EMI	U8, V8
NVCC_EMI_DRAM	L5, M5, R5, T5, Y5, AA5
NVCC_HS10	M20
NVCC_HS4_1	L20
NVCC_HS4_2	P20
NVCC_HS6	N20
NVCC_I2C	V11
NVCC_IPU2	V20
NVCC_IPU4	N16
NVCC_IPU5	K16
NVCC_IPU6	M16

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT9[1]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	T20	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	P18	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	R18	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	V24	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	M18	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	U18	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	U20	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	V23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	U22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	U23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	U24	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	U25	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	R20	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	V25	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	L18	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	V17	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	Y25	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	Y23	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	Y20	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W23	NVCC_IPU2	GPIO	Output	High
DN	K25	VDDA33	Analog	Output	—
DP	K24	VDDA33	Analog	Output	—
DRAM_A0	V4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	V3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	T4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	R1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	P2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A13	R4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A14	R2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A2	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A3	U3	NVCC_EMI_DRAM	DDR2	Output	High

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A21[1]	AD6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB9	NVCC_EMI	GPIO	Output	High
EIM_A23[1]	AE5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	Y9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AD5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AB7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AC6	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	V6	NVCC_EMI	GPIO	Output	High
EIM_CS0	Y17	NVCC_EMI	GPIO	Output	High
EIM_CS1	W6	NVCC_EMI	GPIO	Output	High
EIM_CS2	AE4	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	Y8	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AC7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AB12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	AE8	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AD9	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	AC10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AD10	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	AE10	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AE11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AE9	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	AC9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AD8	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	Y11	NVCC_EMI	GPIO	Input	Keeper
EIM_D29	AD7	NVCC_EMI	GPIO	Input	Keeper
EIM_D30	AC8	NVCC_EMI	GPIO	Input	Keeper
EIM_D31	AB8	NVCC_EMI	GPIO	Input	Keeper
EIM_DA0	AE15	NVCC_EMI	GPIO	Input	Keeper

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
TEST_MODE	AB25	NVCC_PER3	GPIO	Input	100 kΩ pull-down
UART1_CTS	B13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RTS	C13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RXD	D13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_TXD	A12	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_RXD	A13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_TXD	C14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART3_RXD	B14	NVCC_PER12	GPIO	Input	Keeper
UART3_TXD	A14	NVCC_PER12	GPIO	Input	Keeper
USBH1_CLK	C11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA0	B11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA1	A10	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA2	A9	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA3	C10	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA4	B9	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA5	F14	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA6	C12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA7	B12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DIR	B10	NVCC_PER11	GPIO	Input	Keeper
USBH1_NXT	D12	NVCC_PER11	GPIO	Input	Keeper
USBH1_STP	A11	NVCC_PER11	GPIO	Input	Keeper
XTAL[2]	AE23	NVCC_OSC	Analog	Output	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 See Table 3 on page 12 for more information.

3 During power-on reset this port acts as input for fuse override signal. See Table 132 on page 189 for more information.

4 During power-on reset this port acts as output for diagnostic signal. See Table 132 on page 189 for more information.

Table 129. 13 x 13 mm No Connect Assignments (continued)

Ball Status	Ball Assignments
NC	H17
NC	H19
NC	H21
NC	J5
NC	J7
NC	J17
NC	J19
NC	J21
NC	K7
NC	K17
NC	K19
NC	K21
NC	L7
NC	L17
NC	L19
NC	M7
NC	M17
NC	M19
NC	M21
NC	N7
NC	N17
NC	N19
NC	N21
NC	P5
NC	P7
NC	P17
NC	P19
NC	R7
NC	R17
NC	R19
NC	R21
NC	T7
NC	T17

Table 133. 13 × 13 mm, 0.5 mm Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_D11	DRAM_D8	DRAM_SDQS1_B	DRAM_DQM0	DRAM_A4	DRAM_A6	DRAM_A11	1
2	DRAM_D10	DRAM_D9	DRAM_SDQS1	DRAM_DQM1	DRAM_A5	DRAM_A7	DRAM_A14	2
3	DRAM_D4	DRAM_D6	DRAM_SDQS0	DRAM_A1	DRAM_A3	DRAM_A8	DRAM_CS1	3
4	DRAM_D5	DRAM_D7	DRAM_SDQS0_B	DRAM_A0	DRAM_A2	DRAM_A10	DRAM_A13	4
5	NVCC_EMI_DRAM	NVCC_EMI_DRAM	GND	—	GND	NVCC_EMI_DRAM	NVCC_EMI_DRAM	5
6	—	EIM_A20	EIM_CS1	EIM_CRE	VREF	VDDA	VDDA	6
7	GND	EIM_CS5	—	—	—	—	—	7
8	—	EIM_CS3	—	NVCC_EMI	NVCC_EMI	GND	GND	8
9	—	EIM_A24	—	NVCC_PER14	GND	GND	GND	9
10	GND	EIM_BCLK	—	NVCC_PER3	GND	GND	GND	10
11	—	EIM_D28	—	NVCC_I2C	GND	GND	GND	11
12	—	EIM_A16	—	NVCC_SRTC_POW	GND	GND	GND	12
13	GND	EIM_A18	—	AHVSSRGB	GND	GND	VCC	13
14	—	EIM_OE	—	AHVSSRGB	VCC	VCC	VCC	14
15	—	EIM_RW	—	AHVDDRGB	VCC	VCC	VCC	15
16	GND	VDDA	—	AHVDDRGB	VCC	VCC	VDDA33	16
17	—	EIM_CS0	—	DISP2_DAT9	—	—	—	17
18	—	EIM_DA5	—	DI1_PIN11	DISP2_DAT13	DI1_D1_CS	DISP2_DAT10	18
19	GND	I2C1_DAT	—	—	—	—	—	19
20	—	DISPB2_SER_DIO	DI1_D0_CS	NVCC_IPU2	DISP2_DAT14	DISP2_DAT0	DISP2_DAT6	20
21	—	—	—	—	GND	—	—	21
22	CKIL	CLK_SS	BOOT_MODE0	NVCC_IPU8	DISP2_DAT2	DISP1_DAT1	DISP1_DAT5	22
23	CKIH2	DISPB2_SER_DIN	DISPB2_SER_RS	DISP2_DAT15	DISP2_DAT3	DISP1_DAT0	DISP1_DAT4	23
24	BOOT_MODE1	POR_B	DI1_PIN13	DISP2_DAT11	DISP2_DAT4	DISP1_DAT2	CSI1_D10	24
25	RESET_IN_B	DISPB2_SER_CLK	DI1_PIN12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	CSI1_D11	25
	AA	Y	W	V	U	T	R	