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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	527-TFBGA
Supplier Device Package	527-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx515djzk8c

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

Table 20. LVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Schmitt trigger VT+[1, 2]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1, 2]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	VI = 0 or OVDD	—	—	See Note [3]	—
Input current (22 kΩ Pull-up)	Iin	VI = 0	—	—	161	μA
Input current (47 kΩ Pull-up)	Iin	VI = 0	—	—	76	μA
Input current (100 kΩ Pull-up)	Iin	VI = 0	—	—	36	μA
Input current (100 kΩ Pull-down)	Iin	VI = OVDD	—	—	36	μA
Keeper Circuit Resistance	—	OVDD = 1.875 V OVDD = 2.775 V	— —	22 17	— —	kΩ

1 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3 I/O leakage currents are listed in Table 25.

4.3.4 Ultra-High Voltage I/O (UHVIO) DC Parameters

The parameters in Table 21 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 21. UHVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = –1mA	OVDD–0.15	—	—	V
Low-level output voltage	Vol	Iout = 1mA	—	—	0.15	V
High-level output current, low voltage mode	Ioh_lv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –2.2 –4.4 –6.6	—	—	 mA
High-level output current, high voltage mode	Ioh_hv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –5.1 –10.2 –15.3	—	—	 mA
Low-level output current, low voltage mode	Iol_lv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 2.2 4.4 6.6	—	—	 mA
Low-level output current, high voltage mode	Iol_hv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 5.1 10.2 15.3	—	—	 mA
High-Level DC input voltage[1,2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[2,3]	VIL	—	0	—	0.3 × OVDD	V

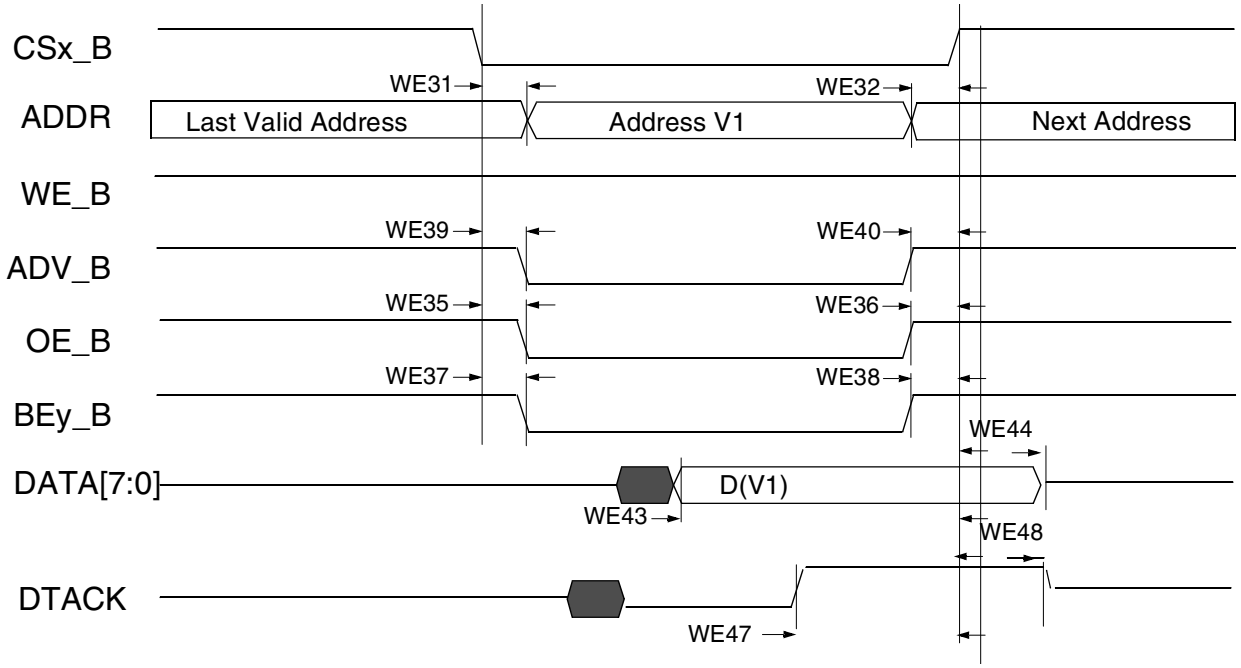

Figure 30. DTACK Read Access (DAP=0)

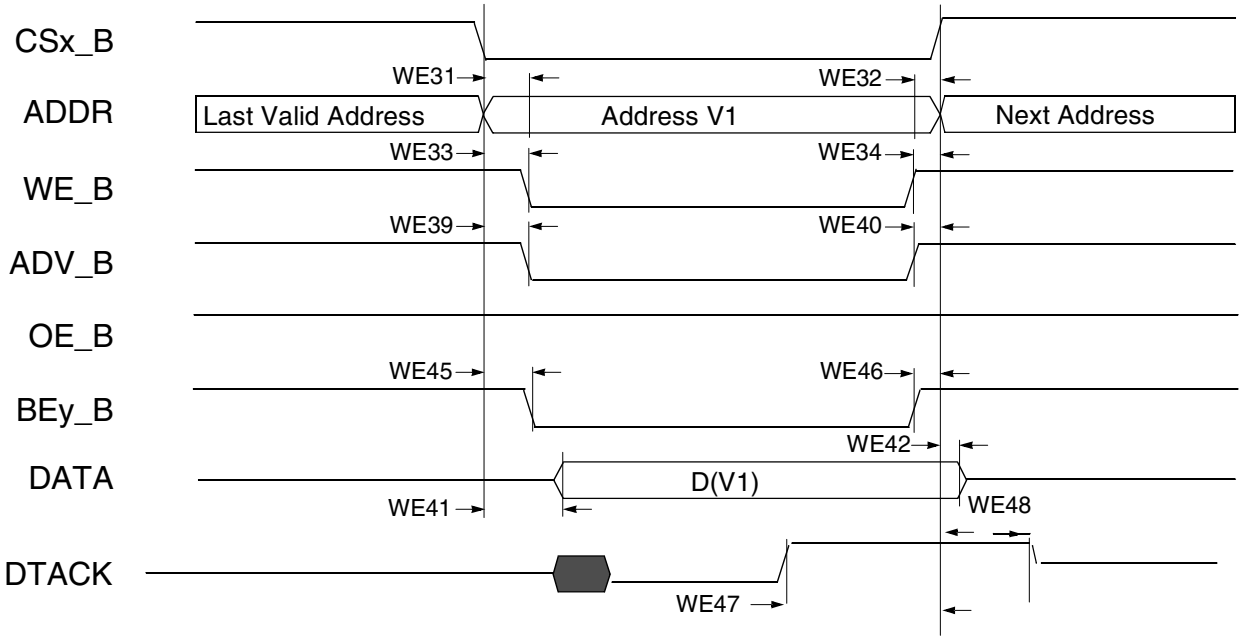

Figure 31. DTACK Write Access (DAP=0)

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[3]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[4]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[5] + WE4 - WE7 + (ADVN + ADVA + 1 - CSA[3])	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN_CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-CSA)	3 + (OEA + RADVN+RADVA+AD H+1-CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA[6] - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	3 - (RBEN[7]- CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 53.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

Table 67. eCSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.7.2.2 eCSPI Slave Mode Timing

Figure 41 depicts the timing of eCSPI in Slave mode and Table 68 lists the eCSPI Slave Mode timing characteristics.

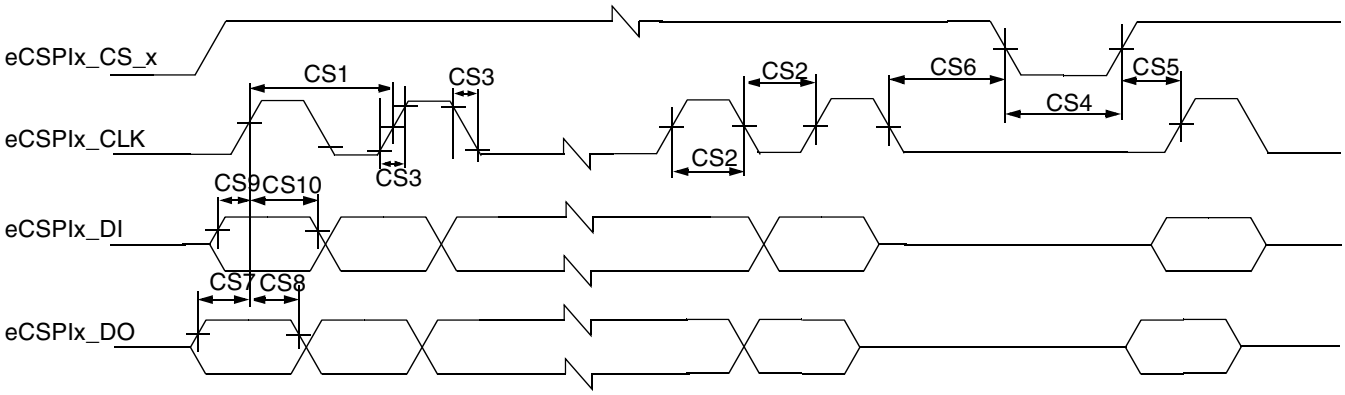

Figure 41. eCSPI Slave Mode Timing Diagram

Table 68. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: display processing, image conversions, and other related functions.
- Synchronization and control capabilities such as avoidance of tearing artifacts.

4.7.8.1 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.1.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.1.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 50.

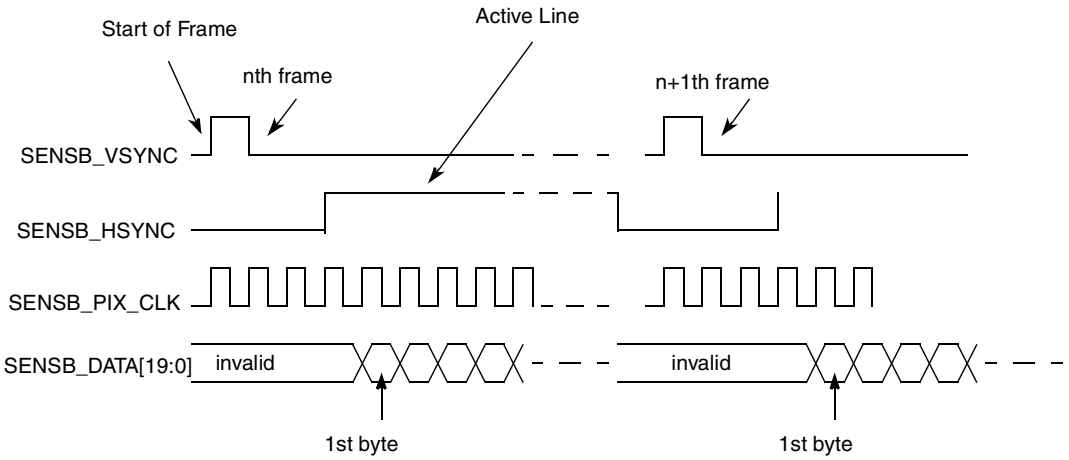

Figure 50. Gated Clock Mode Timing Diagram

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

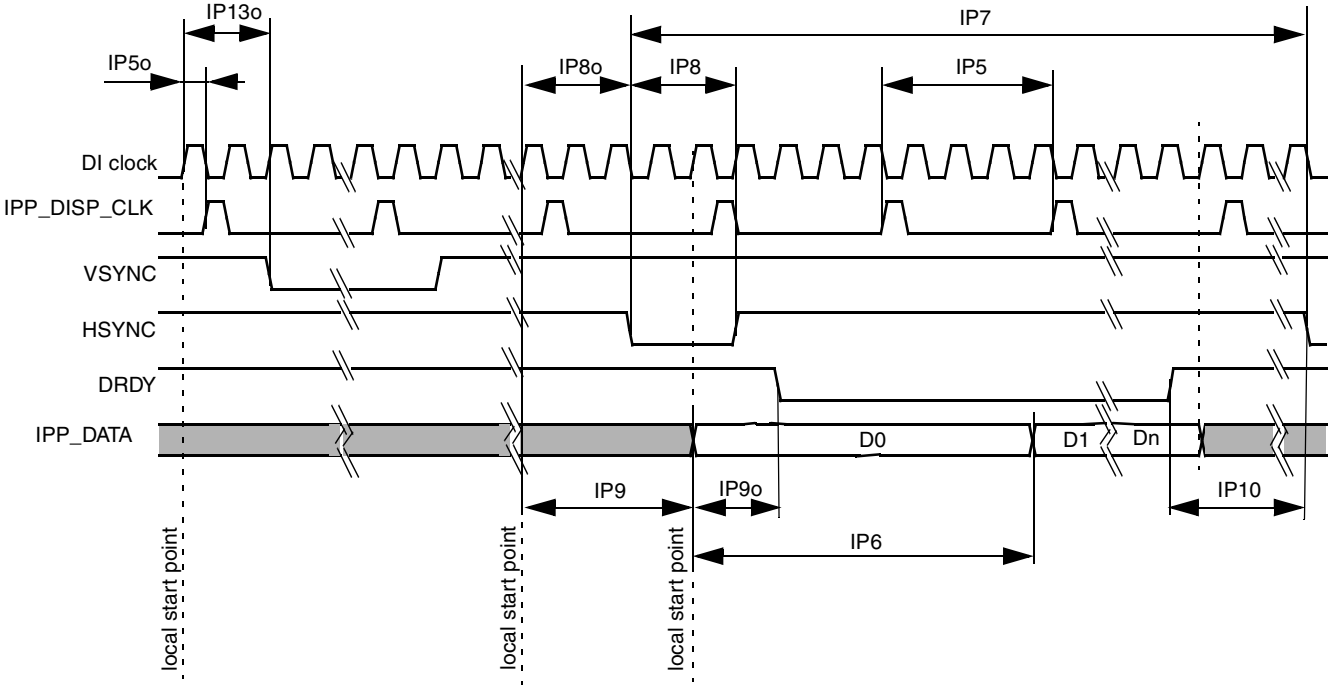

Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

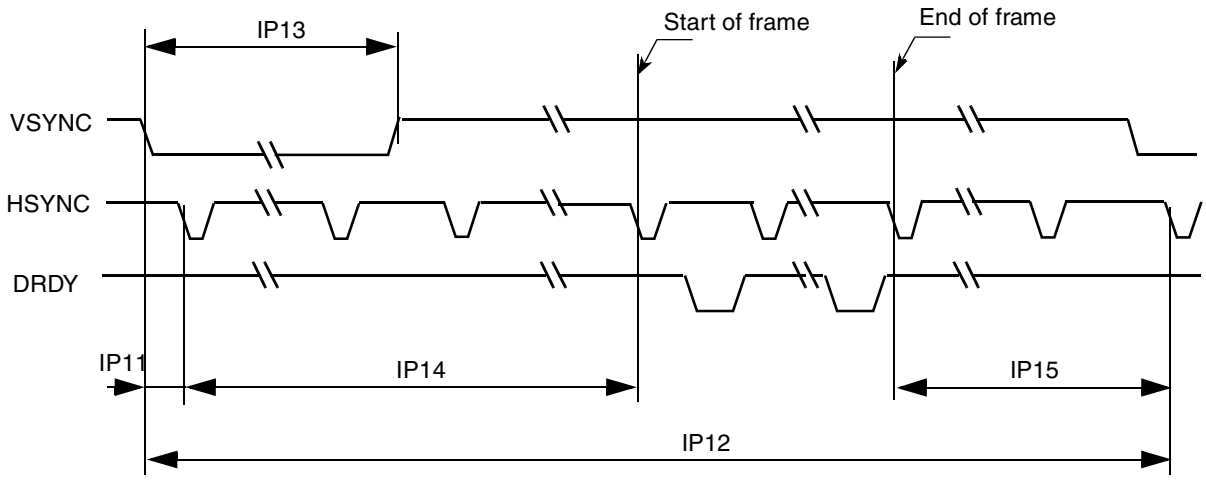

Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

The maximal accuracy of UP/DOWN edge of IPP_DATA is

$$\text{Accuracy} = T_{diclk} \pm 0.75\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed via registers.

Figure 56 shows the synchronous display interface timing diagram for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set by using the register. Table 81 shows the timing characteristics for the diagram shown in Figure 56.

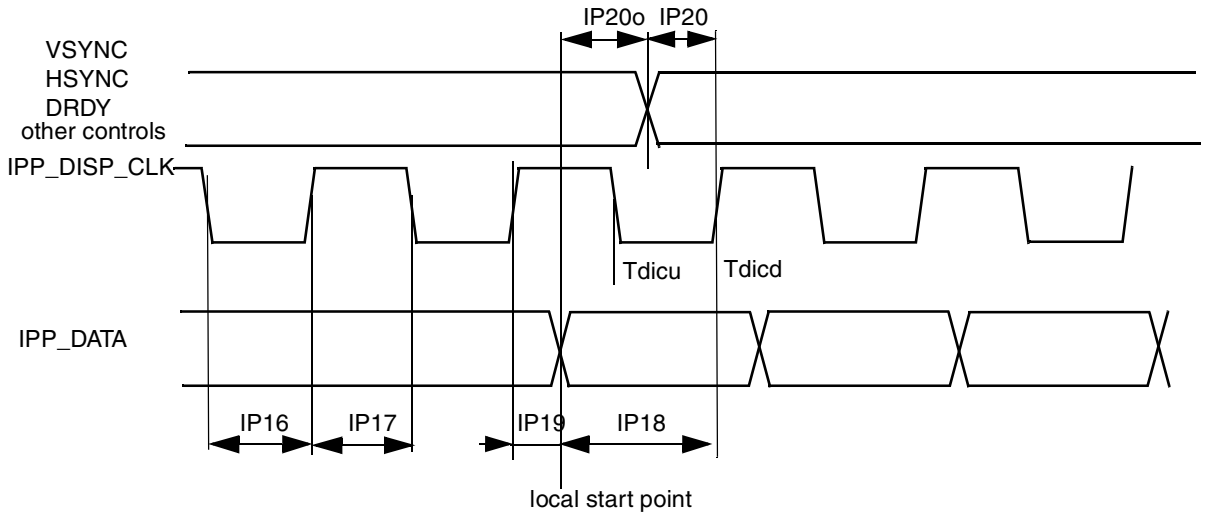

Figure 56. Synchronous Display Interface Timing Diagram—Access Level

Table 81. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–1.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–1.5	Tdicp–Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu–1.5	Tocsu	Tocsu+1.5	—
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd–1.5–Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

Figure 66 depicts timing of the 5-wire serial interface. For this interface, a separate RS line is added.

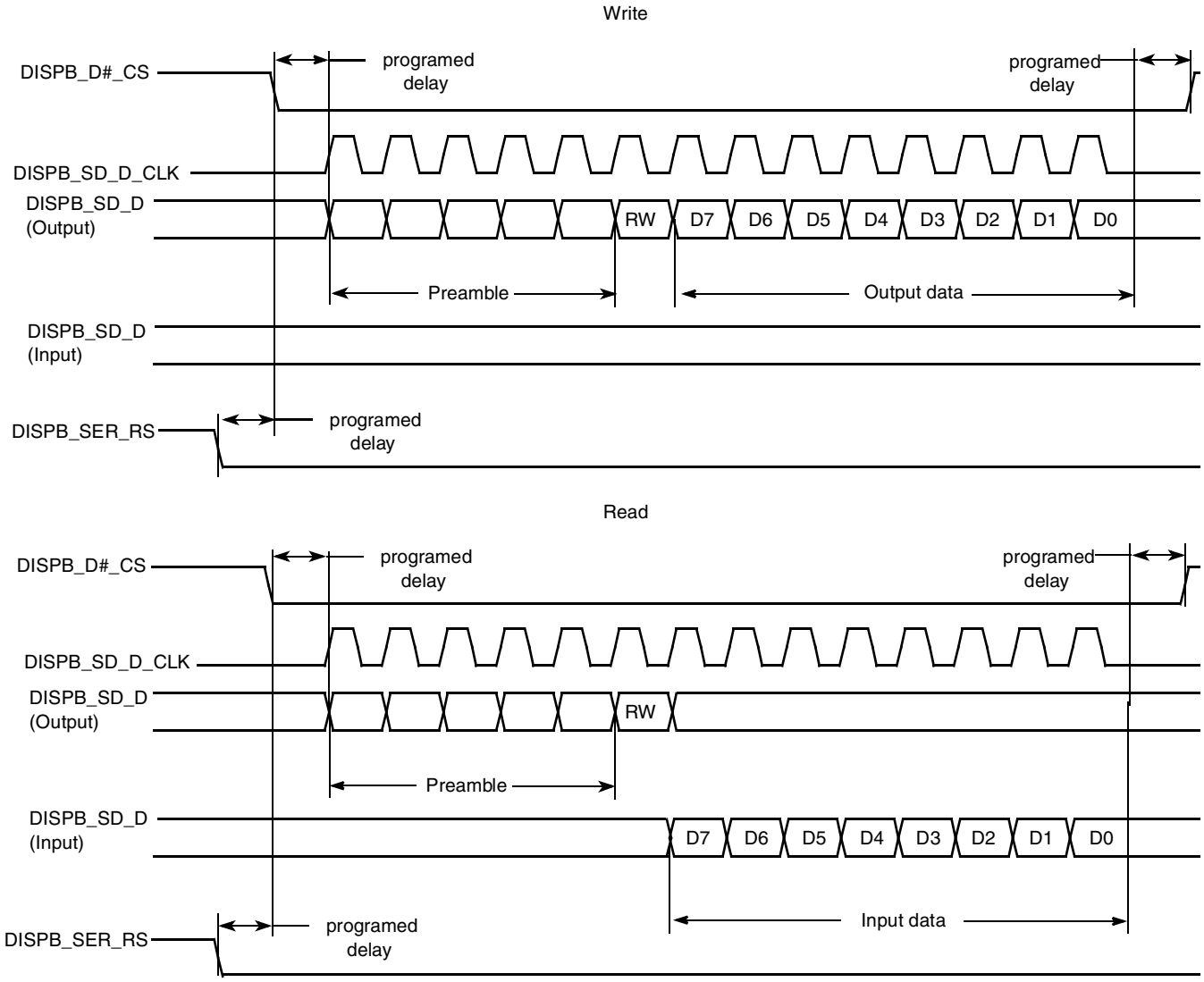

Figure 66. 5-Wire Serial Interface Timing Diagram

Figure 70 depicts Write 1 Sequence timing, Figure 71 depicts the Read Sequence timing, and Table 88 lists the timing parameters.

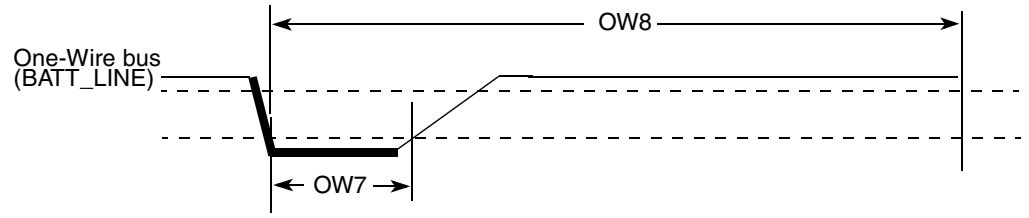

Figure 70. Write 1 Sequence Timing Diagram

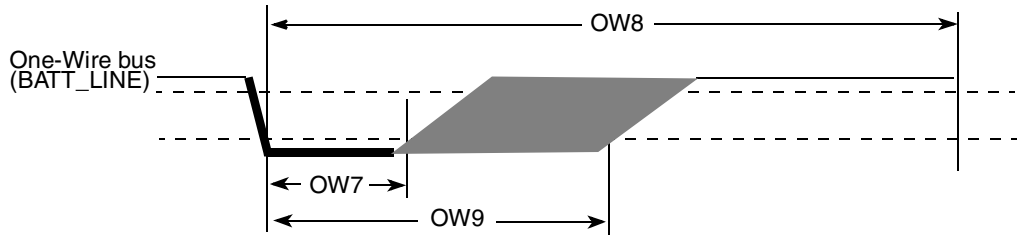

Figure 71. Read Sequence Timing Diagram

Table 88. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write /Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.7.10 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM.The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

4.7.11.3 UDMA Output Timing

Figure 81 shows timing when the UDMA out transfer starts, Figure 82 shows timing when the UDMA out host terminates transfer, Figure 83 shows timing when the UDMA out device terminates transfer, and Table 96 lists the timing parameters for UDMA out burst.

Figure 81. UDMA Out Transfer Starts Timing Diagram

Figure 82. UDMA Out Host Terminates Transfer Timing Diagram

Figure 83. UDMA Out Device Terminates Transfer Timing Diagram

Table 96. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 81, Figure 82, Figure 83	Value	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.16.1.1 UART RS-232 Serial Mode Timing

UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 107 lists the UART RS-232 serial mode transmit timing characteristics.

Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 107. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1]$-T_{ref\_clk}$[2]	$1/F_{baud\_rate}+T_{ref\_clk}$	—

[1] $1/F_{baud\_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists serial mode receive timing characteristics.

Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 108. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2]$-1/(16\times F_{baud\_rate})$	$1/F_{baud\_rate}+1/(16\times F_{baud\_rate})$	—

[1] The UART receiver can tolerate 1/(16×Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16×Fbaud_rate).

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.7.16.1.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

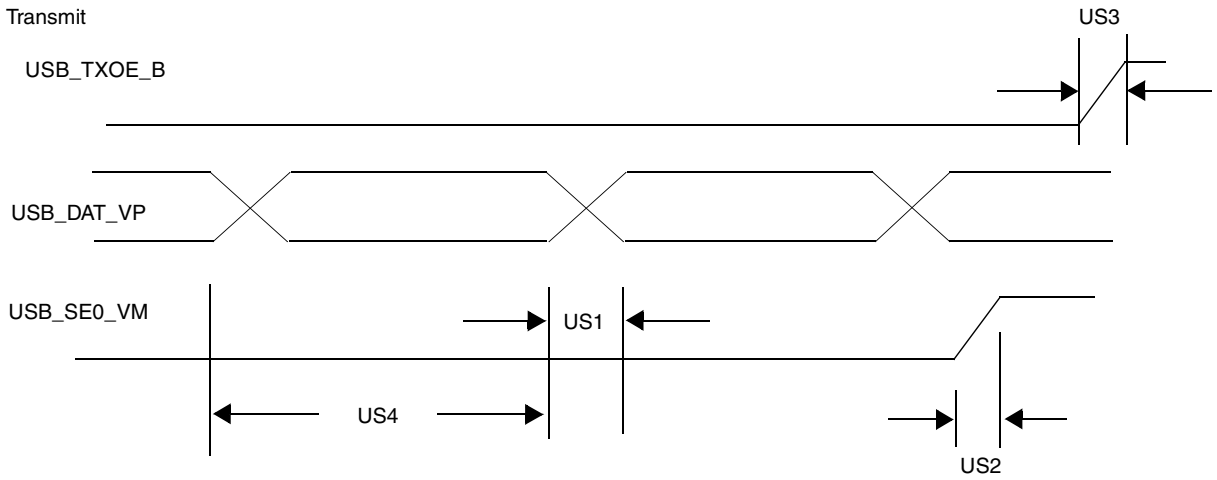

Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

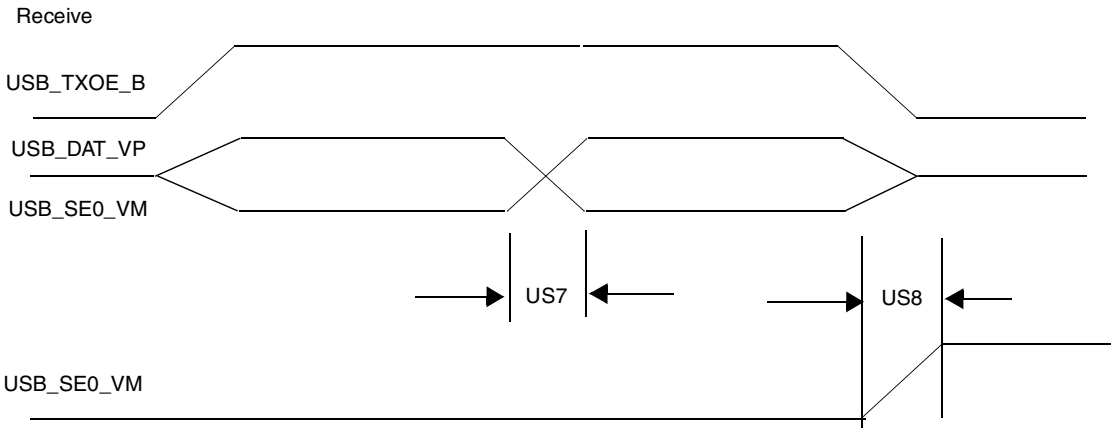

Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

4.7.18 USB Parallel Interface Timing

Electrical and timing specifications of Parallel Interface are presented in the subsequent sections. Table 121 shows the signal definitions in parallel mode. Figure 108 shows the USB transmit/receive waveform in parallel mode. Table 122 shows the USB timing specification for ULPI parallel mode.

Table 121. Signal Definitions—Parallel Interface (Normal ULPI)

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to Clock.
USB_Data[7:0]	I/O	Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the Data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

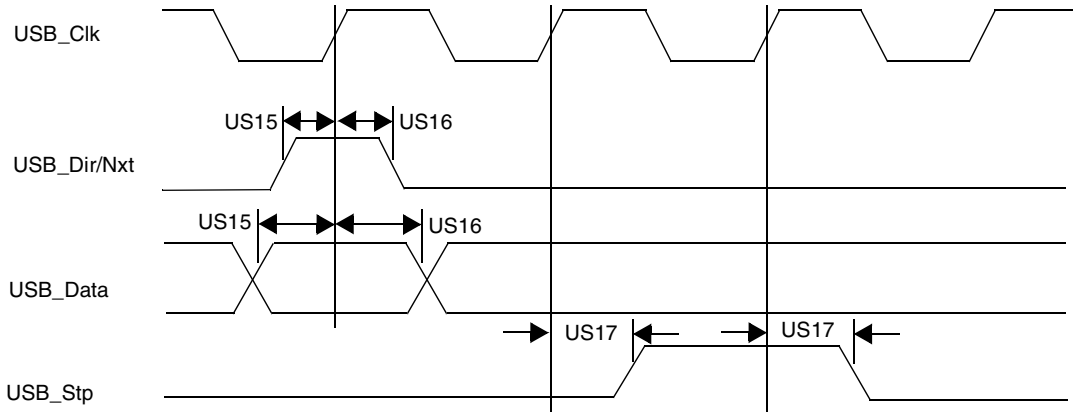

Figure 108. USB Transmit/Receive Waveform in Parallel Mode

Table 122. USB Timing Specification for ULPI Parallel Mode

ID	Parameter	Min	Max	Unit	Conditions/ Reference Signal
US15	Setup Time (Dir, Nxt in, Data in)	6	—	ns	10 pF
US16	Hold Time (Dir, Nxt in, Data in)	0	—	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H3 routed to DISP2 I/O[1] and H1	—	9	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H2	—	11	ns	10 pF

[1] H3 routed to NANDF I/O is recommended for Full and Low-Speed use only.

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_A4	U1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A5	U2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A6	T1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A7	T2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A8	T3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A9	P1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CAS	N4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS0	P3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS1	R3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D0	AC4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D1	AC3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D10	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D11	AA1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D12	AB2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D13	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D14	AC2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D15	AC1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D16	F2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D17	F3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D18	G3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D19	F4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D2	AB3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D20	H3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D21	G4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D22	J3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D23	H4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D24	J4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D25	J1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D26	J2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D27	H1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D28	H2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D29	G1	NVCC_EMI_DRAM	DDR2	Output	High

Table 129. 13 x 13 mm No Connect Assignments (continued)

Ball Status	Ball Assignments
NC	H17
NC	H19
NC	H21
NC	J5
NC	J7
NC	J17
NC	J19
NC	J21
NC	K7
NC	K17
NC	K19
NC	K21
NC	L7
NC	L17
NC	L19
NC	M7
NC	M17
NC	M19
NC	M21
NC	N7
NC	N17
NC	N19
NC	N21
NC	P5
NC	P7
NC	P17
NC	P19
NC	R7
NC	R17
NC	R19
NC	R21
NC	T7
NC	T17

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_WAIT	AB4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EXTAL[2]	AB20	NVCC_OSC	Analog	Input	—
FASTR_ANA[2]	W20	NVCC_PER3	—	Input	—
FASTR_DIG[2]	Y20	NVCC_PER3	—	Input	—
GPANAIO[2]	J23	NVCC_USBPHY	Analog	Output	—
GPIO_NAND	D5	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
GPIO1_0	B21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_1	D20	NVCC_PER5	GPIO	Input	Keeper
GPIO1_2	A22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_3	D18	NVCC_PER5	GPIO	Input	Keeper
GPIO1_4	B22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_5	D19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_6	C19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_7	B23	NVCC_PER5	GPIO	Input	Keeper
GPIO1_8	C21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_9	C20	NVCC_PER5	GPIO	Input	Keeper
I2C1_CLK	W15	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
I2C1_DAT	AB16	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
ID	L19	NVCC_USBPHY	Analog	Input	Pull-up
IOB[2]	AC19	AHVDDRGB	Analog	Output	—
IOB_BACK[2]	AB19	—	Analog	Output	—
IOG[2]	AC18	AHVDDRGB	Analog	Output	—
IOG_BACK[2]	AB18	—	Analog	Output	—
IOR[2]	AC17	AHVDDRGB	Analog	Output	—
IOR_BACK[2]	AB17	—	Analog	Output	—
JTAG_DE_B	AB15	NVCC_PER14	GPIO	Input/Open-drain output	47 kΩ pull-up
JTAG_MOD	V14	NVCC_PER14	GPIO	Input	100 kΩ pull-up
JTAG_TCK	V15	NVCC_PER14	GPIO	Input	100 kΩ pull-down
JTAG_TDI	Y14	NVCC_PER14	GPIO	Input	47 kΩ pull-up
JTAG_TDO	AA15	NVCC_PER14	GPIO	3-state output	Keeper
JTAG_TMS	AC16	NVCC_PER14	GPIO	Input	47 kΩ pull-up

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D5	A5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	C6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	E7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	D4	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	B3	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	E2	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	E1	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	D1	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	E14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AA16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	W16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AA17	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	Y15	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	U20	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	Y21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A17	NVCC_PER15	UHVIO	Output	—
SD1_CMD	E16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	D16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	A18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	F17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	A19	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	B18	NVCC_PER17	UHVIO	Output	—
SD2_CMD	G17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	E17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B19	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	D17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	C17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down