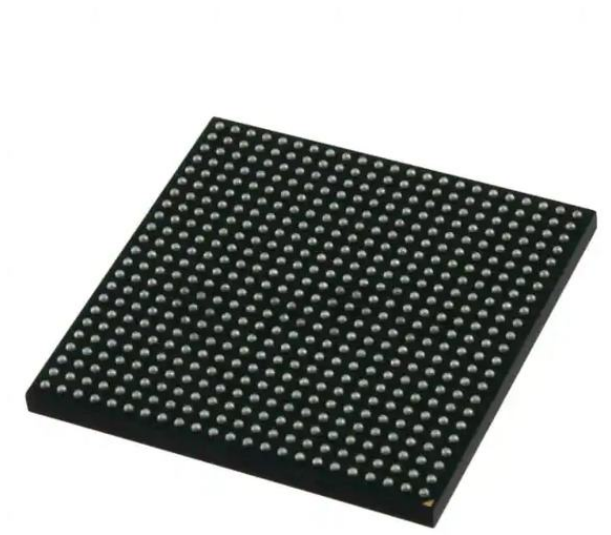

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-20°C ~ 85°C (TC)
Security Features	Boot Security, Cryptography, Hardware ID, RTIC, Secure JTAG
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcimx515djm8c

Features include the following:

- **Smart Speed Technology**—The heart of the i.MX51 processors is a level of power management throughout the device that enables the rich suite of multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Smart Speed Technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than typical industry expectations.
- **Applications Processor**—The i.MX51 processors boost the capabilities of high-tier portable applications by providing for the ever-increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) allows the device run at much lower voltage and frequency with sufficient MIPS for tasks such as audio decode resulting in significant power reduction.
- **Multimedia Powerhouse**—The multimedia performance of the i.MX51 processors is boosted by a multi-level cache system and further enhanced by a Multi-Standard Hardware Video Codec, autonomous Image Processing Unit, SD and HD720p Triple Video (TV) Encoder with triple video DAC, Neon (including Advanced SIMD, 32-bit Single-Precision floating point support and Vector Floating Point co-processor), and a programmable smart DMA (SDMA) controller.
- **Powerful Graphics Acceleration**—Graphics is the key to mobile game navigation, web browsing, and other applications. The i.MX51 processors provide two independent, integrated Graphics Processing Units: OpenGL ES 2.0 3D graphics accelerator (27 Mtri/s, 166 Mpix/s) and OpenVG 1.1 2D graphics accelerator (166 Mpix/s).
- **Interface Flexibility**—The i.MX51 processor interface supports connection to all popular types of external memories: DDR2, Mobile DDR, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC), and OneNAND. Designers seeking to provide products that deliver a rich multimedia experience find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, High-Speed USB On-The-Go with PHY, and three High-Speed USB hosts, multiple expansion card ports (High-Speed MMC/SDIO Host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, I^2S serial audio, and SIM card, among others).
- **Increased Security**—Because the need for advanced security for mobile devices continues to increase, the i.MX51 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the MX51 security features contact your Freescale representative.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_INT_REQ	When using the MC13892 power management IC, the PMIC_INT_REQ high-priority interrupt input on i.MX51 should be either floated or tied to NVCC_SRTC_POW with a 4.7 kΩ to 68 kΩ resistor. This avoids a continuous current drain on the real-time clock backup battery due to a 100 kΩ on-chip pull-up resistor. PMIC_INT_REQ is not used by the Freescale BSP (board support package) software. The BSP requires that the general-purpose INT output from the MC13892 be connected to the i.MX51 GPIO input GPIO1_8 configured to cause an interrupt that is not high-priority. The original intent was for PMIC_INT_REQ to be connected to a circuit that detects when the battery is almost depleted. In this case, the I/O must be configured as alternate mode 0 (ALT0 = power fail).
POR_B	This cold reset negative logic input resets all modules and logic in the IC. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Memory repair – Configuration of memory repair per fuse settings • Cold reset logic of WDOG – Some WDOG logic is only reset by POR_B. See WDOG chapter in *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details.
RREFEXT	Determines the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required.
SGND, SVCC, and SVDDGP	These sense lines provide the ability to sense actual on-chip voltage levels on their respective supplies. SGND monitors differentials of the on-chip ground versus an external power source. SVCC monitors on-chip VCC, and SVDDGP monitors VDDGP. Freescale recommends connection of the SVCC and SVDDGP signals to the feedback inputs of switching power-supplies or to test points.
STR	This signal is reserved for Freescale manufacturing use. The user should float this signal.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
VREG	This regulator is no longer used and should be floated by the user.
XTAL/EXTAL	The user should tie a fundamental-mode crystal across XTAL and EXTAL. The crystal must be rated for a maximum drive level of 100 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. Freescale BSP (Board Support Package) software requires 24 MHz on EXTAL. The crystal can be eliminated if an external 24 MHz oscillator is available. In this case, EXTAL must be directly driven by the external oscillator and XTAL is floated. The EXTAL signal level must swing from NVCC_OSC to GND. If the clock is used for USB, then there are strict jitter requirements: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY. The COSC_EN bit in the CCM (Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. COSC_EN is bit 12 in the CCR register of the CCM.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	100 kΩ pull-down
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_DE_B	Input/open-drain output	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3 IOMUX Configuration for Boot Media

The information provided in this section describes the contacts assigned for each type of bootable media. It also includes data about the clocks used during boot flow and their frequencies. Signals that can be multiplexed appear in tables throughout this section. See the IOMUXC chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details about how to program the IOMUX controller.

Table 13. i.MX51 Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies	—			V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V
NVCC_HS4_1 NVCC_HS4_2 NVCC_HS6 NVCC_HS10	HS-GPIO additional digital power supplies	1.65	—	3.1	V
NVCC_I2C	I^2C and HS-I^2C I/O Supply[7]	1.65	1.875	1.95	V
		2.7	3.0	3.3	
NVCC_SRTC_ POW	SRTC Core and I/O Supply (LVIO)	1.1	1.2	1.3	V
VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 11 and Table 126 for details. This is not a power supply.	—	—	—	—
T_C	Case Temperature (MCIMX51xD—Consumer)	–20	—	85	°C
	Case Temperature (MCIMX51xC—Industrial)	–40	—	95	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 The NVCC_IPUx rails are isolated from one another. This allows the connection of different supply voltages for each one. For example, NVCC_IPU2 can operate at 1.8 V while NVCC_IPU4 operates at 3.0 V.

Table 16. i.MX51 Stop Mode Current and Power Consumption (continued)

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled. USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow T_A = 25°C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	0.012	
		Total	1.09	mW
Stop Mode • External reference clocks enabled • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.20 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	1.5	
		Total	4.8	mW
Stop Mode • External reference clocks enabled • No power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	50	mA
		VCC	2	
		VDDA	1.15	
		NVCC_OSC	1.5	
		Total	63	mW

Table 51. WEIM Signal Cross Reference (continued)

Reference Manual WEIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUX Controller Chapter Nomenclature
ADDR	EIM_A[27:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.7.2 WEIM Internal Module Multiplexing

Table 52 provides WEIM internal muxing information.

Table 52. WEIM Interface Pinout in Various Configurations

	Non Multiplexed Address/Data Mode (MUM=0)							Multiplexed Address/Data Mode (MUM=1)	
	8-Bit (DSZ=100)	8-Bit (DSZ=101)	8-Bit[1] (DSZ=110)	8-Bit (DSZ=111)	16-Bit (DSZ=001)	16-Bit (DSZ=010)	32-Bit (DSZ=011)	16-Bit (DSZ=001)	32-Bit (DSZ=011)
A[15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]
A[27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	NANDF_D [11:0]
D[7:0], EIM_EB0	NANDF_D [7:0]	—	—	—	NANDF_D [7:0]	—	NANDF_D [7:0]	EIM_DA [7:0]	EIM_DA [7:0]
D[15:8], EIM_EB1	—	NANDF_D [15:8]	—	—	NANDF_D [15:8]	—	NANDF_D [15:8]	EIM_DA [15:8]	EIM_DA [15:8]
D[23:16], EIM_EB2	—	—	EIM_D [23:16]	—	—	EIM_D [23:16]	EIM_D [23:16]	—	NANDF_D [7:0]
D[31:24], EIM_EB3	—	—	—	EIM_D [31:24]	—	EIM_D [31:24]	EIM_D [31:24]	—	NANDF_D [15:8]

[1] This mode is not supported due to erratum ENGcm11244.

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[3]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[4]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[5] + WE4 - WE7 + (ADVN + ADVA + 1 - CSA[3])	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN_CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-CSA)	3 + (OEA + RADVN+RADVA+AD H+1-CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA[6] - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	3 - (RBEN[7]- CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

4.7 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.7.1 CSPI Timing Parameters

This section describes the timing parameters of the CSPI. The CSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

Table 64. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	CSPI1[1], USBH1, and DI1 via IOMUX
eCSPI2	NANDF and USBH1 via IOMUX
CSPI	NANDF, USBH1, SD1, SD2, and GPIO via IOMUX

[1] This set of BGA contacts is labeled CSPI, but is actually an eCSPI channel

4.7.1.1 CSPI Master Mode Timing

Figure 38 depicts the timing of CSPI in Master mode and Table 65 lists the CSPI Master Mode timing characteristics.

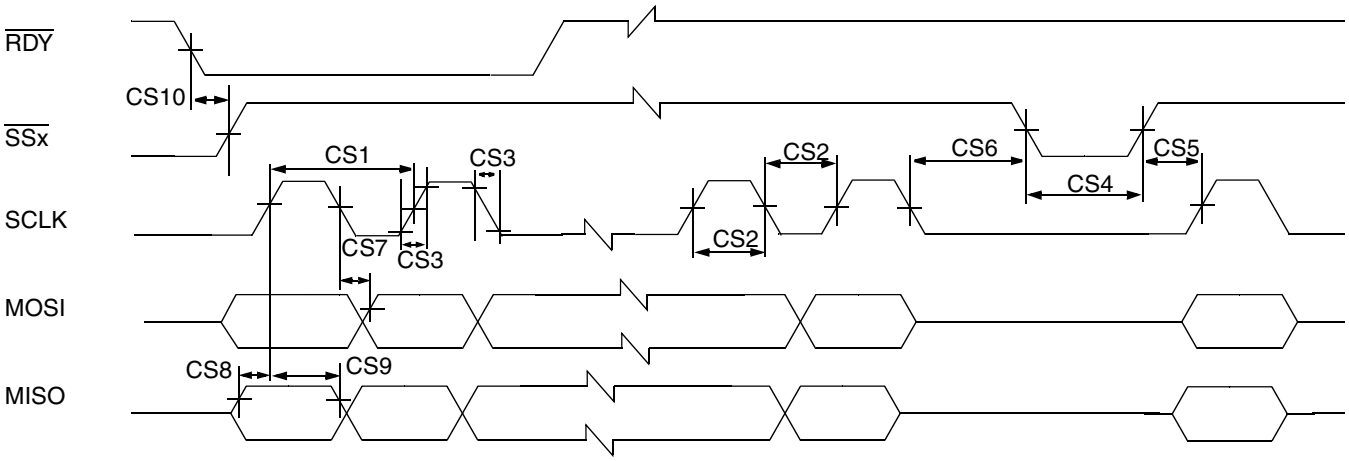

Figure 38. CSPI Master Mode Timing Diagram

Table 65. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns

Table 65. CSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	–1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, “I/O AC Parameters”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.1.2 CSPI Slave Mode Timing

Figure 39 depicts the timing of CSPI in Slave mode. Table 66 lists the CSPI Slave Mode timing characteristics.

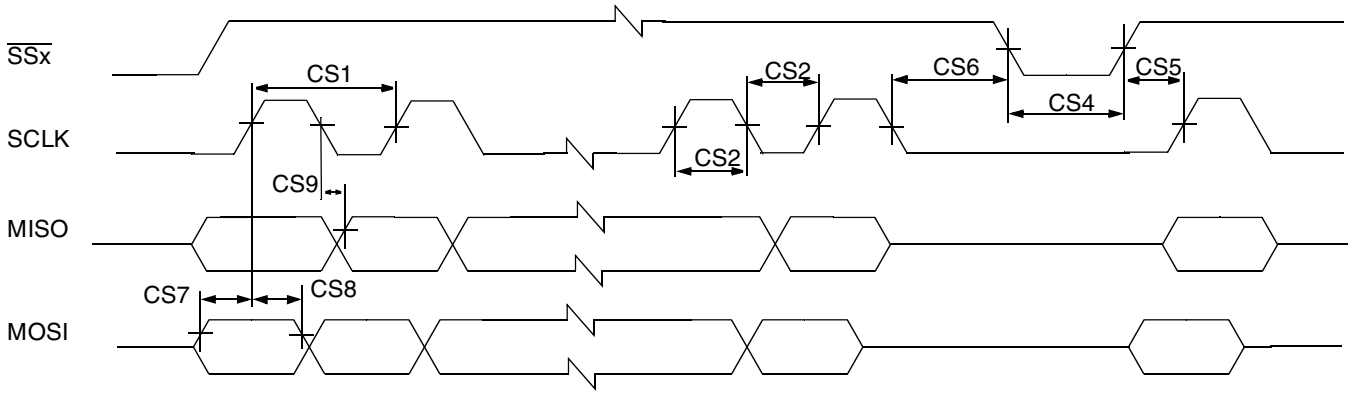

Figure 39. CSPI Slave Mode Timing Diagram

Table 66. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (SS setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Setup Time	t_{Smosi}	5	—	ns

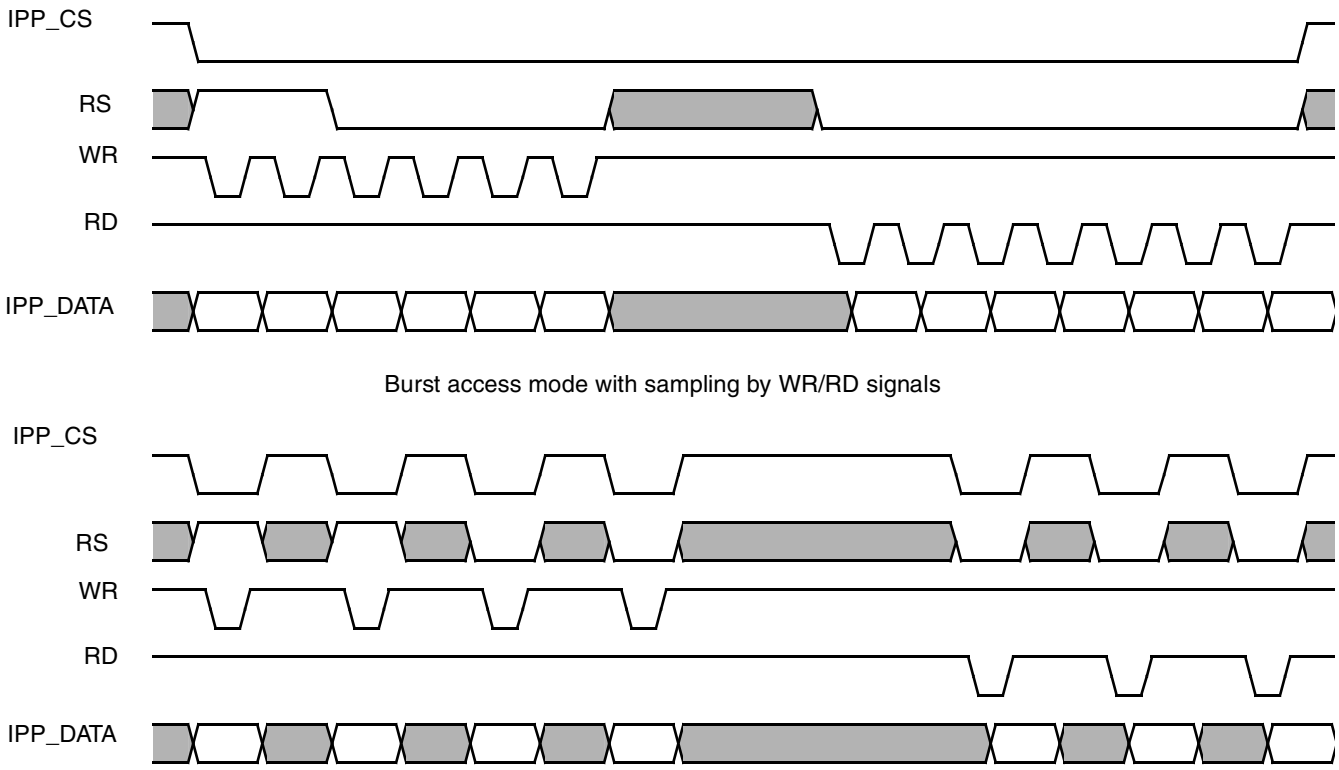

Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

4.7.8.7.2 Asynchronous Parallel Interface Timing Parameters

Figure 63 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 84 shows the timing characteristics at display access level. Table 83 shows the timing characteristics at the logical level—from configuration perspective. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

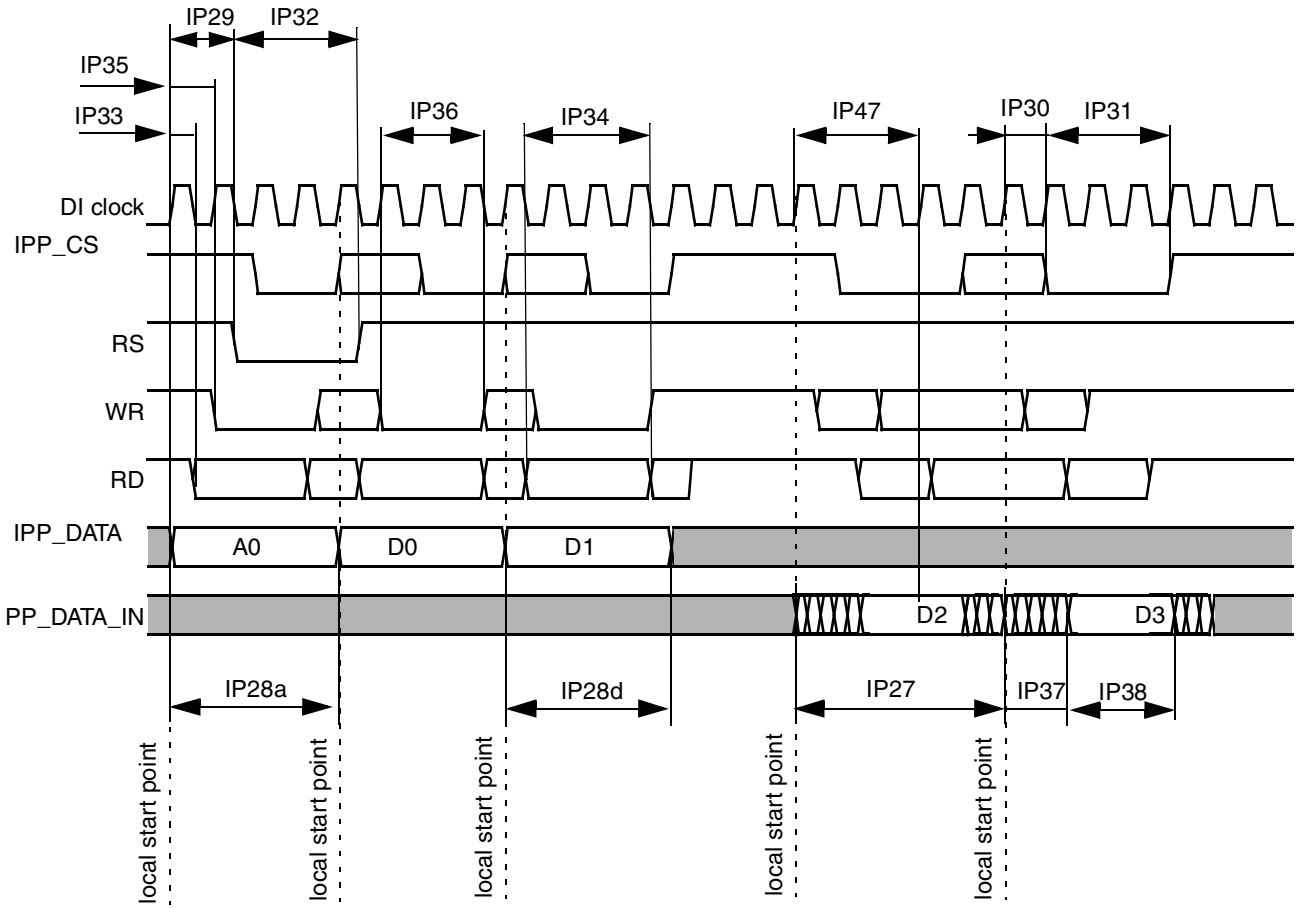

Figure 63. Asynchronous Parallel Interface Timing Diagram

Table 83. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP27	Read system cycle time	Tcycr	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns

Figure 83. UDMA Out Device Terminates Transfer Timing Diagram

Table 96. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 81, Figure 82, Figure 83	Value	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

Each of these steps is done in one CKIL period (usually 32 kHz). Power-down can be started because of a SIM Card removal detection or launched by the processor. Figure 87 and Table 98 shows the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

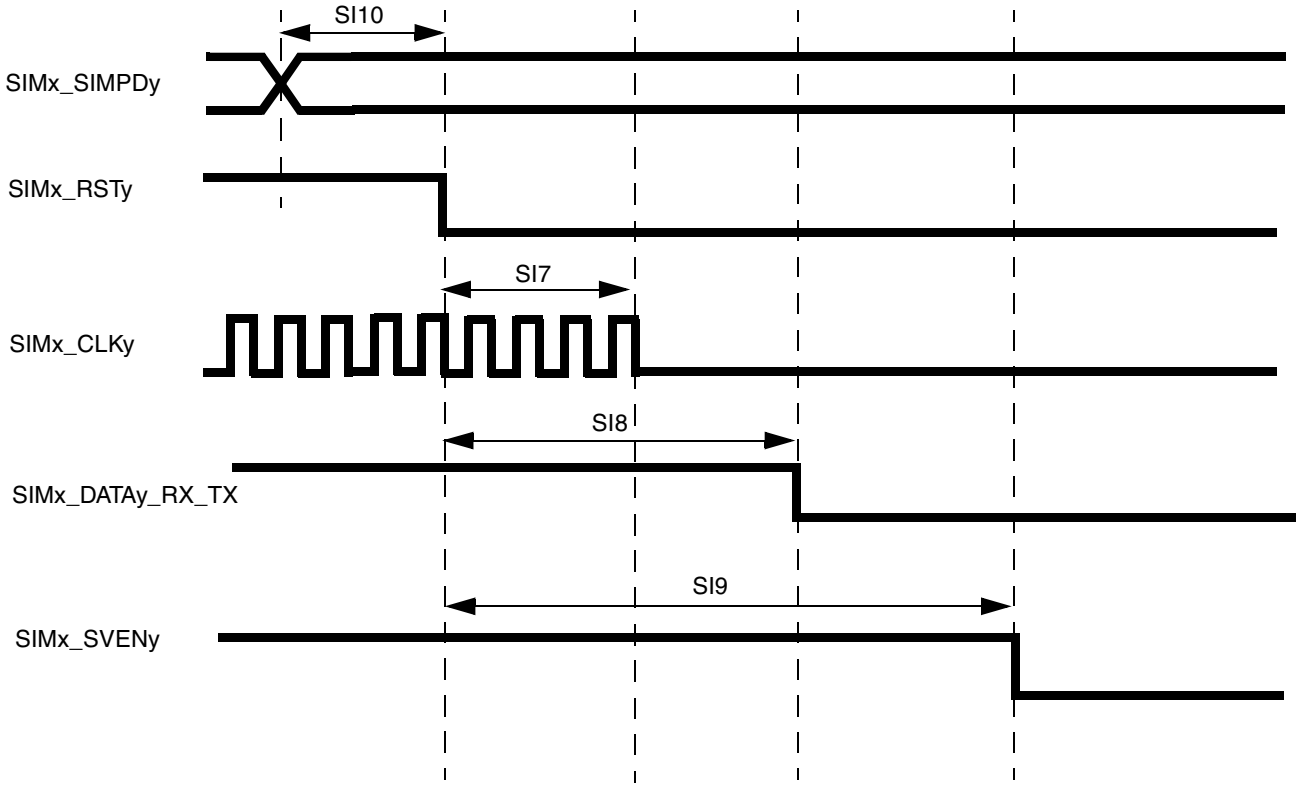

Figure 87. SmartCard Interface Power Down AC Timing

Table 98. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9×1/Fckil	1.1×1/Fckil	ns
SI8	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8×1/Fckil	2.2×1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7×1/Fckil	3.3×1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9×1/Fckil	1.1×1/Fckil	ns

Table 104. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16 UART

Table 106 shows the UART I/O configuration based on which mode is enabled.

Table 106. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.7.16.1 UART Electrical

This section describes the electrical information of the UART module.

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A21[1]	AD6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB9	NVCC_EMI	GPIO	Output	High
EIM_A23[1]	AE5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	Y9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AD5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AB7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AC6	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	V6	NVCC_EMI	GPIO	Output	High
EIM_CS0	Y17	NVCC_EMI	GPIO	Output	High
EIM_CS1	W6	NVCC_EMI	GPIO	Output	High
EIM_CS2	AE4	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	Y8	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AC7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AB12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	AE8	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AD9	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	AC10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AD10	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	AE10	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AE11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AE9	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	AC9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AD8	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	Y11	NVCC_EMI	GPIO	Input	Keeper
EIM_D29	AD7	NVCC_EMI	GPIO	Input	Keeper
EIM_D30	AC8	NVCC_EMI	GPIO	Input	Keeper
EIM_D31	AB8	NVCC_EMI	GPIO	Input	Keeper
EIM_DA0	AE15	NVCC_EMI	GPIO	Input	Keeper

Table 128. 13 x 13 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	H6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	D6	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	F6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	G6	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	E3	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	A15	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AC18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	AE18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AC19	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	AB18	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	Y24	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	AA25	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A18	NVCC_PER15	UHVIO	Output	—
SD1_CMD	C17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	B18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	D17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	D18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	C18	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	A19	NVCC_PER17	UHVIO	Output	—
SD2_CMD	F16	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	F18	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	A21	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	F17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down
STR	D14	NVCC_PER12	—	—	—

Table 131. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

Table 134. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_SDCKE0	DRAM_A7	DRAM_RAS	EIM_SDBA0	DRAM_A13	DRAM_D0	DRAM_D3	1
2	DRAM_A1	DRAM_A5	DRAM_A8	DRAM_A10	DRAM_A12	DRAM_A14	DRAM_D2	2
3	DRAM_A2	DRAM_CS1	DRAM_A6	DRAM_A9	EIM_SDBA1	DRAM_SDCLK	DRAM_D1	3
4	EIM_BCLK	DRAM_CS0	DRAM_A4	DRAM_CAS	DRAM_A11	DRAM_SDCLK_B	DRAM_D4	4
5	EIM_CS5	EIM_DTACK	DRAM_SDCKE1	DRAM_A3	DRAM_SDWE	GND	VREF	5
6	EIM_CS4	EIM_CS1	EIM_CS0	VDD_ANA_PLL_A	VDD_DIG_PLL_A	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	EIM_OE	EIM_CS2	EIM_D31	NVCC_EMI	GND_ANA_PLL_A	GND_DIG_PLL_A	VDD_FUSE	7
8	EIM_A19	EIM_D29	EIM_D27	EIM_D23	NVCC_EMI	VCC	GND	8
9	EIM_A16	EIM_D25	EIM_D21	EIM_EB3	NVCC_EMI	VCC	GND	9
10	EIM_D24	EIM_D19	EIM_D17	EIM_EB2	NVCC_EMI	VCC	GND	10
11	EIM_D18	EIM_DA15	EIM_DA13	EIM_DA11	NVCC_EMI	VCC	GND	11
12	EIM_DA12	EIM_DA9	EIM_EB1	EIM_EB0	NVCC_EMI	VCC	GND	12
13	EIM_DA6	EIM_DA5	EIM_DA7	EIM_DA1	NVCC_PER14	VDDA	GND	13
14	EIM_DA2	JTAG_TDI	JTAG_TRSTB	JTAG_MOD	NVCC_SRTC_POW	NVCC_I2C	GND	14
15	JTAG_TDO	PMIC_STBY_REQ	I2C1_CLK	JTAG_TCK	VREFOUT	NGND_TV_BACK	GND	15
16	PMIC_INT_REQ	CKIL	PMIC_ON_REQ	TVDAC_DHVDD	NVCC_TV_BACK	GND	GND	16
17	PMIC_RDY	COMP	NVCC_OSC	NGND_OSC	GND_ANA_PLL_B	VCC	VCC	17
18	AHVDDRGB	AHVDDRGB	VDD_DIG_PLL_B	GND_DIG_PLL_B	NVCC_PER3	NVCC_IPU2	NVCC_IPU9	18
19	AHVSSRGB	AHVSSRGB	VDD_ANA_PLL_B	CKIH1	DISPB2_SER_DIN	DISP2_DAT13	DISP2_DAT11	19
20	CKIH2	FASTR_DIG	FASTR_ANA	TEST_MODE	POR_B	DI1_PIN13	DISP2_DAT9	20
21	CLK_SS	RESET_IN_B	DISPB2_SER_RS	DISPB2_SER_DIO	DI1_D0_CS	DISP2_DAT15	DISP2_DAT0	21
22	DI1_PIN12	DI1_PIN11	DISP2_DAT10	DISP2_DAT4	DISP1_DAT2	DISP1_DAT4	CSI1_D10	22
23	DISP2_DAT14	DISP2_DAT12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	DISP1_DAT5	CSI1_D11	23
	AA	Y	W	V	U	T	R	

Table 135. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	05/2010	• Updated CaseTemperature Range column in Table 1, "Ordering Information," on page 3. • Changed the VREFOUT column in Table 3, "Special Signal Considerations," on page 12. • Added Section 3, “IOMUX Configuration for Boot Media”. • Updated Figure 2, "Power-Up Sequence," on page 24. • Updated the Minimum and Maximum columns in Table 13, "i.MX51 Operating Ranges," on page 19. • Added a note in Section 4.2.1, “Power-Up Sequence”. • Updated Section 4.2.1, “Power-Up Sequence.” • Changed the Input current (47 kΩ Pull-up) column in Table 21, "UHVIO DC Electrical Characteristics," on page 27 to Input current (75 kO Pull-up). • Added new table for parameters for DDR2 Pad output buffer Impedance. See Table 27, "DDR2 I/O Output Buffer Impedance HVE = 0," on page 32. • Added new section under Section 4.5, “I/O AC Parameters”. See Section 4.5.4, “AC Electrical Characteristics for DDR2”. • Updated Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48. In the VIH (for square wave input) parameter, the minimum frequency was changed to NVCC_PER3 - 0.25V and the maximum frequency was changed to NVCC_PER3. • Added a note in Section 4.6.6, “NAND Flash Controller (NFC) Parameters” after Table 49. • Updated Asymmetric Mode Min, Symmetric Mode Min, and Max columns of Table 50. • Removed Conditions parameters of the Full scale output voltage row in Table 82. • Updated Section 4.7.11, “P-ATA Timing Parameters”. Replaced ATA/ATAPI-6 specification with ATA/ATAPI-5 specification. • In Table 102, "SSI Transmitter Timing with Internal Clock," on page 135, under the Synchronous Internal Clock Operation sections for the ID SS42, minimum frequency was changed from 10.0 to 30. • In Table 103, "SSI Receiver Timing with Internal Clock," on page 136, under the Internal Clock Operation section for ID SS20, minimum frequency was changed from 10.0 to 30. • In Table 104, "SSI Transmitter Timing with External Clock," on page 138, under the External Clock Operation section for ID SS38, maximum frequency was changed from 15.0 to 30. • Added a new section Section 4.7.16.1, “UART Electrical”, under Section 4.7.16, “UART”. • In Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148, for IDs SS28 and SS29, direction was changed from out to in. • In Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150, for IDs US40 and US41, direction was changed from out to in and the reference signal was changed to USB_VM1 and USB_VP1 respectively. • In Table 122, "USB Timing Specification for ULPI Parallel Mode," on page 151, added an extra row for ID17. • Updated Signal and Direction columns in Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 150. • Updated Signal names in Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 148.
Rev. 1	10/2009	Initial public release.