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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

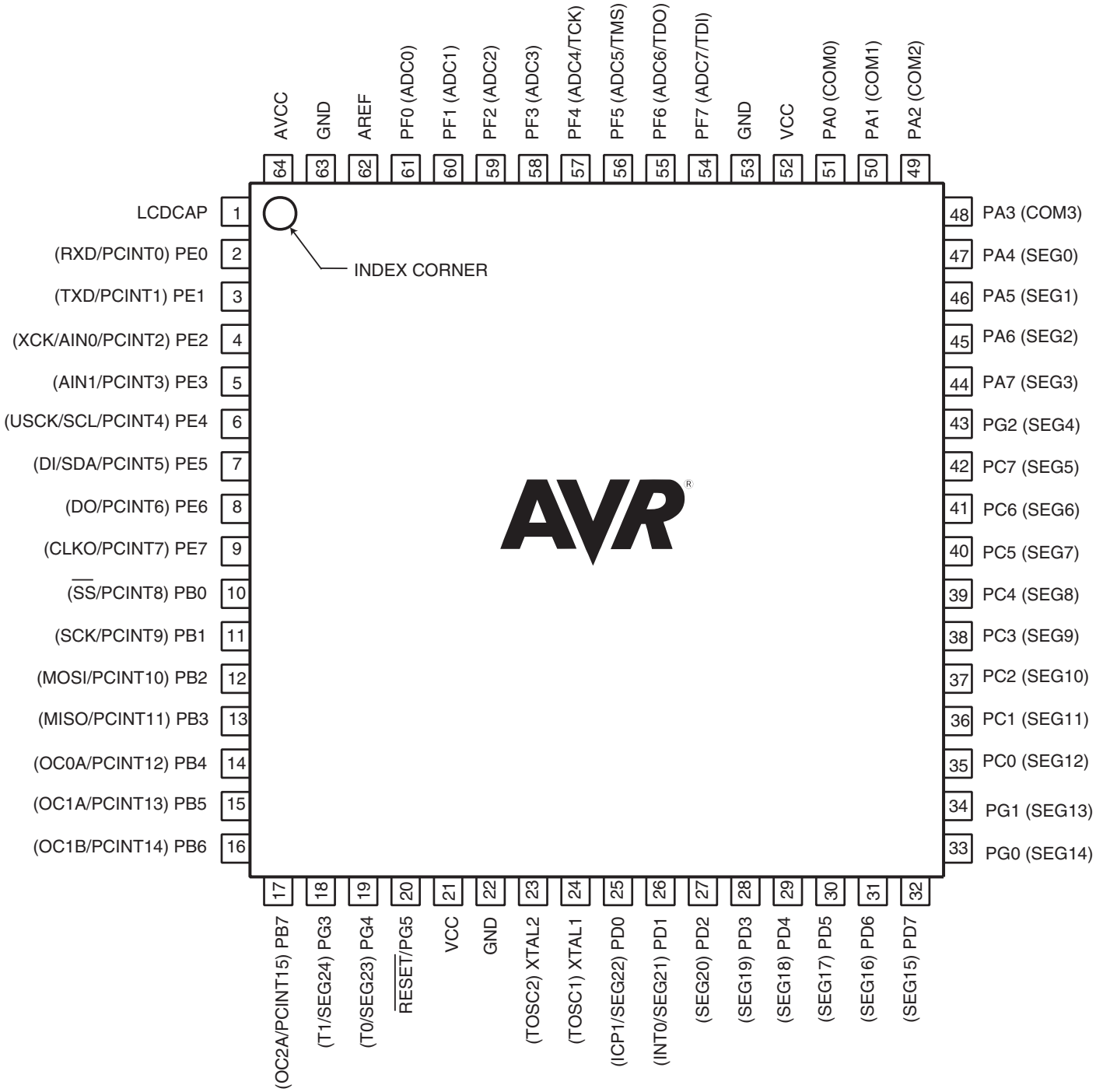
Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega169pa-aur

  - Real Time Counter with separate oscillator
  - Four PWM channels
  - 8-channel, 10-bit ADC
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Universal Serial Interface with Start Condition Detector
  - Programmable Watchdog Timer with Separate On-chip oscillator
  - On-chip analog comparator
  - Interrupt and Wake-up on pin change
- Special microcontroller features
  - Power-on reset and programmable Brown-out detection
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Five sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and packages
  - 54/69 programmable I/O lines
  - 64/100-lead TQFP, 64-pad QFN/MLF, and 64-pad DRQFN
- Speed Grade:
  - ATmega169A/169PA/649A/649P:
    - 0 - 16MHz @ 1.8 - 5.5V
  - ATmega3290A/3290PA/6490A/6490P:
    - 0 - 20MHz @ 1.8 - 5.5V
- Temperature range:
  - -40°C to 85°C industrial
- Ultra-low power consumption (picoPower® devices)
  - Active mode:
    - 1MHz, 1.8V: 215µA
    - 32kHz, 1.8V: 8µA (including oscillator)
    - 32kHz, 1.8V: 25µA (including oscillator and LCD)
  - Power-down mode:
    - 0.1µA at 1.8V
  - Power-save mode:
    - 0.6µA at 1.8V (Including 32kHz RTC)
    - 750nA at 1.8V

1. Pin configurations

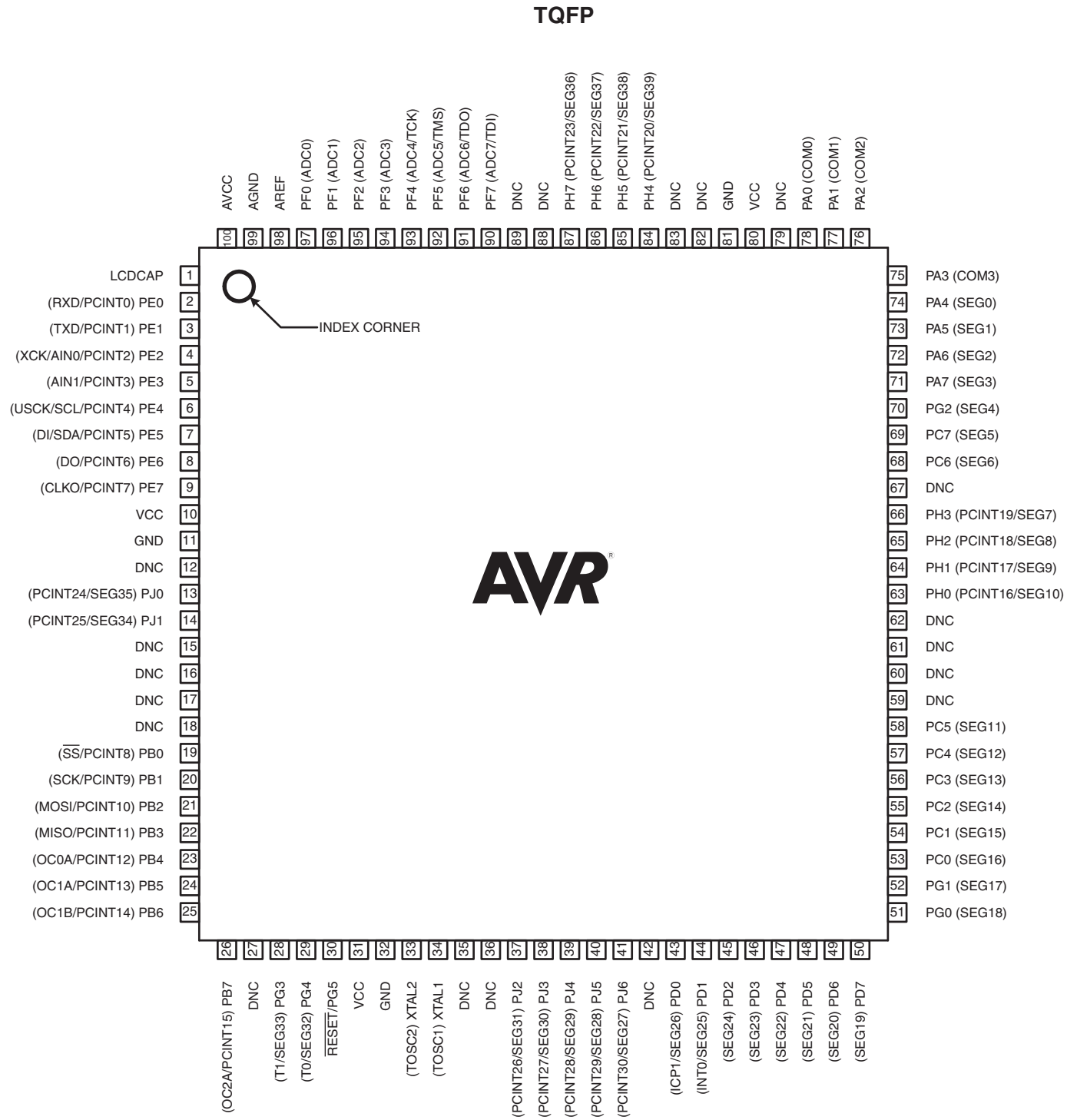
1.1 Pinout - 64A (TQFP) and 64M1 (QFN/MLF)

Figure 1-1. Pinout Atmel ATmega169A/ATmega169PA/ATmega329A/ATmega329PA/ATmega649A/ATmega649P.



1.2 Pinout - 100A (TQFP)

Figure 1-2. Pinout Atmel ATmega3290A/ATmega3290PA/ATmega6490A/ATmega6490P.



Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

1.3 Pinout - 64MC (DRQFN)

Figure 1-3. Pinout Atmel ATmega169A/ATmega169PA.

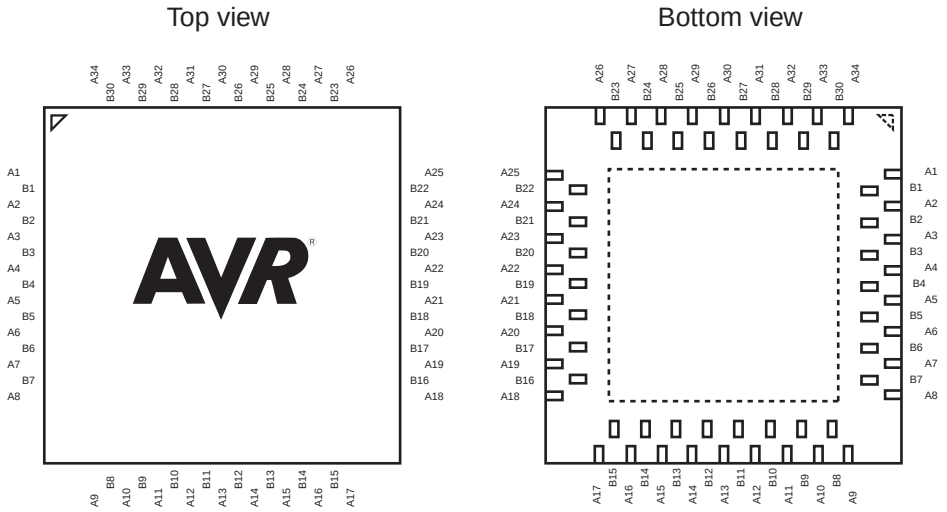


Table 1-1. DRQFN-64 Pinout ATmega169A/ATmega169PA.

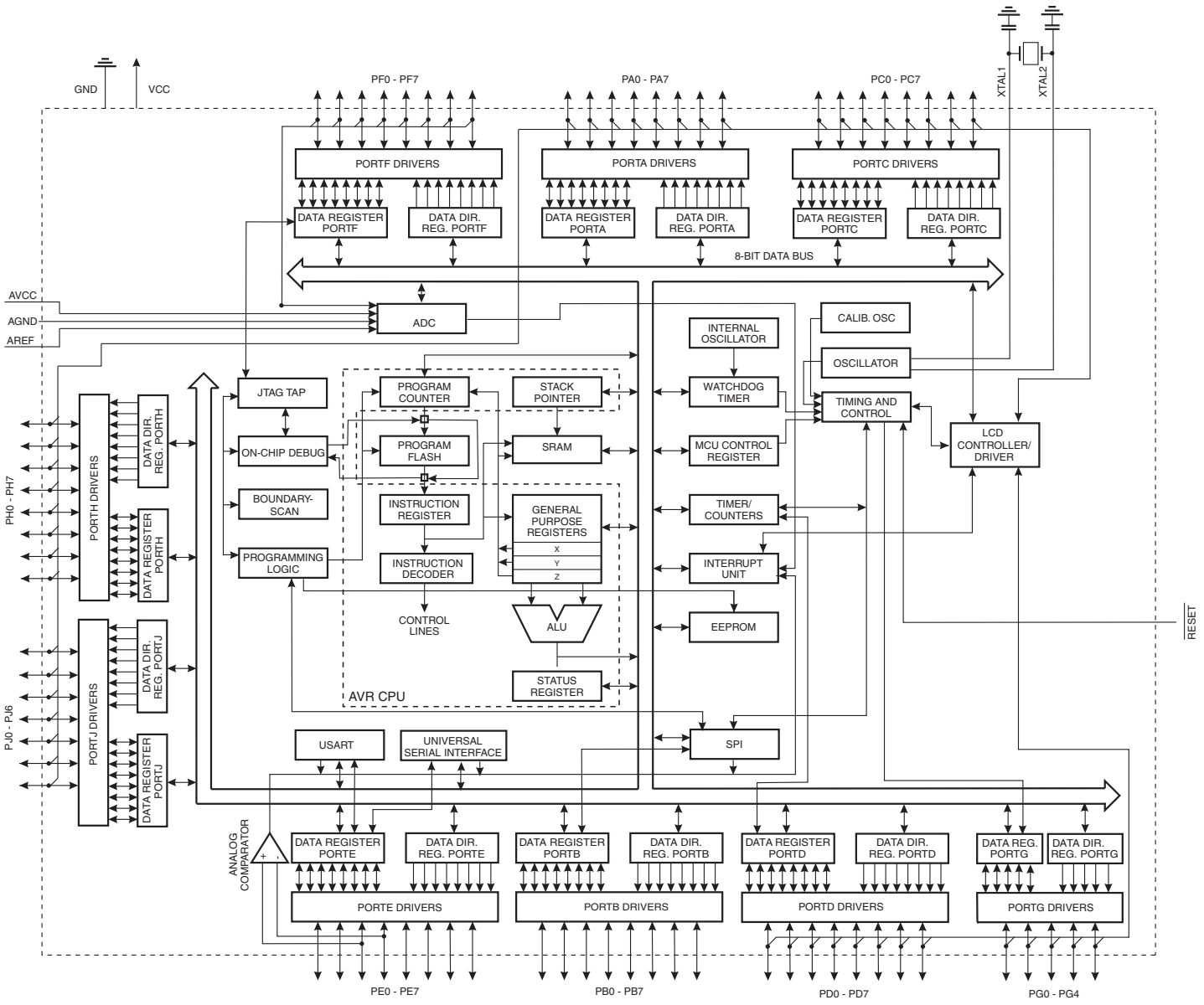
	PE0		PB7		PG1 (SEG13)		PA2 (COM2)
	VLCDCAP		PB6		PG0 (SEG14)		PA3 (COM3)
	PE1		PG3		PC0 (SEG12)		PA1 (COM1)
	PE2		PG4		PC1 (SEG11)		PA0 (COM0)
	PE3		$\overline{\text{RESET}}$		PC2 (SEG10)		VCC
	PE4		VCC		PC3 (SEG9)		GND
	PE5		GND		PC4 (SEG8)		PF7
	PE6		XTAL2 (TOSC2)		PC5 (SEG7)		PF6
	PE7		XTAL1 (TOSC1)		PC6 (SEG6)		PF5
	PB0		PD0 (SEG22)		PC7 (SEG5)		PF4
	PB1		PD1 (SEG21)		PG2 (SEG4)		PF3
	PB2		PD2 (SEG20)		PA7 (SEG3)		PF2
	PB3		PD3 (SEG19)		PA6 (SEG2)		PF1
	PB5		PD4 (SEG18)		PA4 (SEG0)		PF0
	PB4		PD5 (SEG17)		PA5 (SEG1)		AREF
			PD7 (SEG15)				AVCC
			PD6 (SEG16)				GND

2. Overview

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a low-power CMOS 8-bit microcontroller based on the Atmel®AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one

single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P provides the following features: 16K/32K/64K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K bytes EEPROM, 1K/2K/4K byte SRAM, 54/69 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, a complete On-chip LCD controller with internal contrast control, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, an 8-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer and the LCD controller continues to run, allowing the user to maintain a timer base and operate the LCD display while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, LCD controller and ADC, to minimize switching noise during ADC conversions. In Standby mode, the XTAL/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

Atmel offers the QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using the Atmel high density non-volatile memory technology. The On-chip In-System re-Programmable (ISP) Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation.

By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.2 Comparison between Atmel ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P

Table 2-1. Differences between: ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P.

ATmega169A	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega169PA	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega329A	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega329PA	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega3290A	32Kbytes	1Kbyte	2Kbyte	4 × 40
ATmega3290PA	32Kbyte	1Kbyte	2Kbyte	4 × 40
ATmega649A	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega649P	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega6490A	64Kbyte	2Kbyte	4Kbyte	4 × 40
ATmega6490P	64Kbyte	2Kbyte	4Kbyte	4 × 40

are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 79.

2.3.8 Port F (PF7...PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.3.9 Port G (PG5...PG0)

Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 83.

2.3.10 Port H (PH7...PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 85.

2.3.11 Port J (PJ6...PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 87.

2.3.12 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in ”System and reset characteristics” on page 332. Shorter pulses are not guaranteed to generate a reset.

2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.16 AREF

This is the analog reference pin for the A/D Converter.

2.3.17 LCDCAP

An external capacitor (typical > 470 nF) must be connected to the LCDCAP pin as shown in Figure 24-2, if the LCD module is enabled and configured to use internal power. This capacitor acts as a reservoir for LCD power (V_{LCD}). A large capacitance reduces ripple on V_{LCD} but increases the time until V_{LCD} reaches its target value.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

5. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

6. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the QTouch and QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API’s to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

7. Register summary

Note: Registers with bold type only available in Atmel ATmega3290A/3290PA/6490A/6490P.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	**LCDDR19**	**SEG339**	**SEG338**	**SEG337**	**SEG336**	**SEG335**	**SEG334**	**SEG333**	**SEG332**	236
(0xFE)	LCDDR18	**SEG331**	**SEG330**	**SEG329**	**SEG328**	**SEG327**	**SEG326**	**SEG325**	SEG324	236
(0xFD)	LCDDR17	SEG323	SEG322	SEG321	SEG320	SEG319	SEG318	SEG317	SEG316	236
(0xFC)	LCDDR16	SEG315	SEG314	SEG313	SEG312	SEG311	SEG310	SEG309	SEG308	236
(0xFB)	LCDDR15	SEG307	SEG306	SEG305	SEG304	SEG303	SEG302	SEG301	SEG300	236
(0xFA)	**LCDDR14**	**SEG239**	**SEG238**	**SEG237**	**SEG236**	**SEG235**	**SEG234**	**SEG233**	**SEG232**	236
(0xF9)	LCDDR13	**SEG231**	**SEG230**	**SEG229**	**SEG228**	**SEG227**	**SEG226**	**SEG225**	SEG224	236
(0xF8)	LCDDR12	SEG223	SEG222	SEG221	SEG220	SEG219	SEG218	SEG217	SEG216	236
(0xF7)	LCDDR11	SEG215	SEG214	SEG213	SEG212	SEG211	SEG210	SEG209	SEG208	236
(0xF6)	LCDDR10	SEG207	SEG206	SEG205	SEG204	SEG203	SEG202	SEG201	SEG200	236
(0xF5)	**LCDDR09**	**SEG139**	**SEG138**	**SEG137**	**SEG136**	**SEG135**	**SEG134**	**SEG133**	**SEG132**	236

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xF4)	LCDDR08	**SEG131**	**SEG130**	**SEG129**	**SEG128**	**SEG127**	**SEG126**	**SEG125**	SEG124	236
(0xF3)	LCDDR07	SEG123	SEG122	SEG121	SEG120	SEG119	SEG118	SEG117	SEG116	236
(0xF2)	LCDDR06	SEG115	SEG114	SEG113	SEG112	SEG111	SEG110	SEG109	SEG108	236
(0xF1)	LCDDR05	SEG107	SEG106	SEG105	SEG104	SEG103	SEG102	SEG101	SEG100	236
(0xF0)	**LCDDR04**	**SEG039**	**SEG038**	**SEG037**	**SEG036**	**SEG035**	**SEG034**	**SEG033**	**SEG032**	236
(0xEF)	LCDDR03	**SEG031**	**SEG030**	**SEG029**	**SEG028**	**SEG027**	**SEG026**	**SEG025**	SEG024	236
(0xEE)	LCDDR02	SEG023	SEG022	SEG021	SEG020	SEG019	SEG018	SEG017	SEG016	236
(0xED)	LCDDR01	SEG015	SEG014	SEG013	SEG012	SEG011	SEG010	SEG009	SEG008	236
(0xEC)	LCDDR00	SEG007	SEG006	SEG005	SEG004	SEG003	SEG002	SEG001	SEG000	236
(0xEB)	Reserved	-	-	-	-	-	-	-	-	
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	LCDCCR	LCDDC2	LCDDC1	LCDDC0	LCDMDT	LCDCC3	LCDCC2	LCDCC1	LCDCC0	234
(0xE6)	LCDFRR	-	LCDPS2	LCDPS1	LCDPS0	-	LCDCD2	LCDCD1	LCDCD0	233
(0xE5)	LCDCRB	LCDCS	LCD2B	LCDMUX1	LCDMUX0	**LCDPM3**	LCDPM2	LCDPM1	LCDPM0	232
(0xE4)	LCDCRA	LCDEN	LCDAB	-	LCDIF	LCDIE	LCDBD	LCDCCD	LCDBL	231
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	-	-	-	-	-	-	-	-	
(0xDD)	**PORTJ**	**-**	**PORTJ6**	**PORTJ5**	**PORTJ4**	**PORTJ3**	**PORTJ2**	**PORTJ1**	**PORTJ0**	93
(0xDC)	**DDRJ**	**-**	**DDJ6**	**DDJ5**	**DDJ4**	**DDJ3**	**DDJ2**	**DDJ1**	**DDJ0**	93
(0xDB)	**PINJ**	**-**	**PINJ6**	**PINJ5**	**PINJ4**	**PINJ3**	**PINJ2**	**PINJ1**	**PINJ0**	93
(0xDA)	**PORTH**	**PORTH7**	**PORTH6**	**PORTH5**	**PORTH4**	**PORTH3**	**PORTH2**	**PORTH1**	**PORTH0**	93
(0xD9)	**DDRH**	**DDH7**	**DDH6**	**DDH5**	**DDH4**	**DDH3**	**DDH2**	**DDH1**	**DDH0**	93
(0xD8)	**PINH**	**PINH7**	**PINH6**	**PINH5**	**PINH4**	**PINH3**	**PINH2**	**PINH1**	**PINH0**	93
(0xD7)	Reserved	-	-	-	-	-	-	-	-	
(0xD6)	Reserved	-	-	-	-	-	-	-	-	
(0xD5)	Reserved	-	-	-	-	-	-	-	-	
(0xD4)	Reserved	-	-	-	-	-	-	-	-	
(0xD3)	Reserved	-	-	-	-	-	-	-	-	
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	Reserved	-	-	-	-	-	-	-	-	
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	Reserved	-	-	-	-	-	-	-	-	
(0xCD)	Reserved	-	-	-	-	-	-	-	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	-	-	-	-	-	-	-	
(0xC8)	Reserved	-	-	-	-	-	-	-	-	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	UDR0	USART0 Data Register								186
(0xC5)	UBRR0H					USART0 Baud Rate Register High				190
(0xC4)	UBRR0L	USART0 Baud Rate Register Low								190
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	UCSR0C	-	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	189
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	188
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	187
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	Reserved	-	-	-	-	-	-	-	-	
(0xBC)	Reserved	-	-	-	-	-	-	-	-	
(0xBB)	Reserved	-	-	-	-	-	-	-	-	
(0xBA)	USIDR	USI Data Register								197
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	198
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	198
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	-	-	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB	153
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x72)	Reserved	-	-	-	-	-	-	-	-	
(0x71)	Reserved	-	-	-	-	-	-	-	-	
(0x70)	TIMSK2	-	-	-	-	-	-	OCIE2A	TOIE2	154
(0x6F)	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	131
(0x6E)	TIMSK0	-	-	-	-	-	-	OCIE0A	TOIE0	137
(0x6D)	**PCMSK2**	**PCINT23**	**PCINT22**	**PCINT21**	**PCINT20**	**PCINT19**	**PCINT18**	**PCINT17**	**PCINT16**	64
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	64
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	64
(0x6A)	Reserved	-	-	-	-	-	-	-	-	
(0x69)	EICRA	-	-	-	-	-	-	ISC01	ISC00	61
(0x68)	Reserved	-	-	-	-	-	-	-	-	
(0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x66)	OSCCAL	Oscillator Calibration Register [CAL7...0]								38
(0x65)	Reserved	-	-	-	-	-	-	-	-	
(0x64)	PRR	-	-	-	PRLCD	PRTIM1	PRSPI	PSUSART0	PRADC	46
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	38
(0x60)	WDTCR	-	-	-	WDCE	WDE	WDP2	WDP1	WDP0	53
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	15
0x3E (0x5E)	SPH	Stack Pointer High								17
0x3D (0x5D)	SPL	Stack Pointer Low								17
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	Reserved	-	-	-	-	-	-	-	-	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	-	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	289
0x36 (0x56)	Reserved									
0x35 (0x55)	MCUCR	JTD	BODS	BODSE	PUD	-	-	IVSEL	IVCE	59/90/275
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	53
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	45
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0x31 (0x51)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	242
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	202
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR	SPI Data Register								165
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	164
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	163
0x2B (0x4B)	GPIOR2	General Purpose I/O Register								29
0x2A (0x4A)	GPIOR1	General Purpose I/O Register								29
0x29 (0x49)	Reserved	-	-	-	-	-	-	-	-	
0x28 (0x48)	Reserved	-	-	-	-	-	-	-	-	
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare A								138
0x26 (0x46)	TCNT0	Timer/Counter0								137
0x25 (0x45)	Reserved	-	-	-	-	-	-	-	-	
0x24 (0x44)	TCCR0A	FOC0A	WGM00	COM0A1	COM0A0	WGM01	CS02	CS01	CS00	135
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSR2	PSR10	138/155
0x22 (0x42)	EEARH	-	-	-	-	-	EEPROM Address Register High			28
0x21 (0x41)	EEARL	EEPROM Address Register Low								28
0x20 (0x40)	EEDR	EEPROM Data Register								28
0x1F (0x3F)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	28
0x1E (0x3E)	GPIOR0	General Purpose I/O Register								29
0x1D (0x3D)	EIMSK	PCIE	PCIE2	PCIE1	PCIE0	-	-	-	INT0	62
0x1C (0x3C)	EIFR	PCIF3	PCIF2	PCIF1	PCIF0	-	-	-	INTF0	63
0x1B (0x3B)	Reserved	-	-	-	-	-	-	-	-	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	
0x18 (0x38)	Reserved	-	-	-	-	-	-	-	-	
0x17 (0x37)	TIFR2	-	-	-	-	-	-	OCF2A	TOV2	154
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	131
0x15 (0x35)	TIFR0	-	-	-	-	-	-	OCF0A	TOV0	138
0x14 (0x34)	PORTG	-	-	-	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	92
0x13 (0x33)	DDRG	-	-	-	DDG4	DDG3	DDG2	DDG1	DDG0	92
0x12 (0x32)	PING	-	-	PING5	PING4	PING3	PING2	PING1	PING0	92

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2

9. Ordering information

9.1 Atmel ATmega169A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5V	ATmega169A-AU ATmega169A-AUR (4) ATmega169A-MU ATmega169A-MUR (4) ATmega169A-MCH ATmega169A-MCHR (4)	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169A-AN ATmega169A-ANR (4) ATmega169A-MN ATmega169A-MNR (4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 29-1 on page 330.
4. Tape & Reel.

Package type	
	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

9.6 Atmel ATmega3290PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega3290PA-AU ATmega3290PA-AUR(4)	100A 100A	Industrial (-40°C to 85°C)
		ATmega3290PA-AN ATmega3290PA-ANR(4)	100A 100A	Industrial (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 330.
4. Tape & Reel.
5. See characterization specification at 105°C.

	Package type
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.7 Atmel ATmega649A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5V	ATmega649A-AU ATmega649A-AUR (4) ATmega649A-MU ATmega649A-MUR (4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-1 on page 330.
4. Tape & Reel.

Package type	
	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

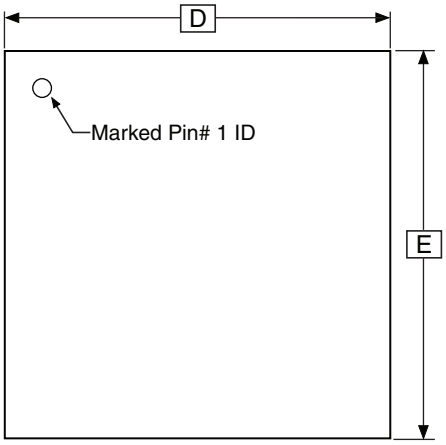
9.9 Atmel ATmega6490A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega6490A-AU ATmega6490A-AUR (4)	100A 100A	Industrial (-40°C to 85°C)

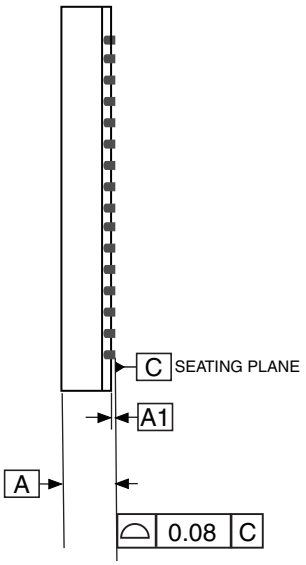
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 330.
4. Tape & Reel.

Package type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

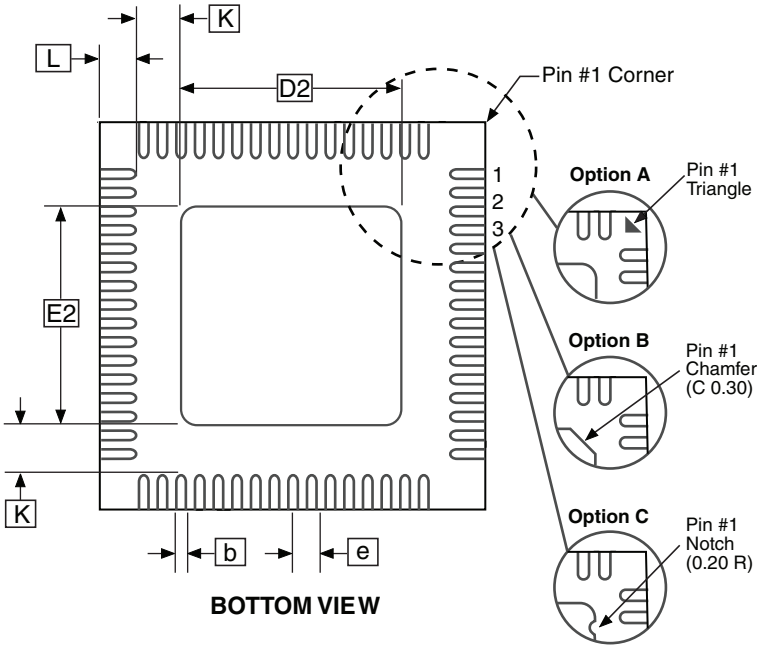
10.2 64M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	

Notes:
1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2010-10-19

Atmel 2325 Orchard Parkway San Jose, CA 95131	**TITLE** **64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	**DRAWING NO.** 64M1	**REV.** H

11.6 Atmel ATmega329A/329PA rev. C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

11.7 Atmel ATmega3290A/3290PA rev. A

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Using BOD disable will make the chip reset**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. **Using BOD disable will make the chip reset**

   If the part enters sleep with the BOD turned off with the BOD disable option

   enabled, a BOD reset will be generated at wakeup and the chip will reset.

   Problem Fix/Workaround

   Do not use BOD disable

11.8 Atmel ATmega3290A/3290PA rev. B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

12. Datasheet revision history

Please note that the referring page numbers in this section are referring to this document.The referring revision in this section are referring to the document revision.

12.1 Rev. 8284F - 08/2014

1. New back page
2. Changed chip references in the text in Section 9.6 ”Low-frequency XTAL oscillator” on page 34.

12.2 Rev. 8284E - 02/2013

1. New template
2. Countless, small corrections made throughout the whole document
3. In Section ”System and reset characteristics” on page 332 the sentence “The following chara apply only to...” has been deleted
4. Former Section 29.6 on page 332 (“Power-on reset”), subsection 29.6.1 (“ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490PA revision C and later”) and subsection 29.6.2 (“ATmega329A/329PA/3290A/3290PA/649A/649P/6490A/6490PA revision A and B”) have been deleted
5. The maximum limits for “Power Supply Current” in Table 29-9 on page 328 have been corrected
6. The maximum limits for “Power Supply Current” in Table 29-11 on page 329 have been corrected
7. Added ”Electrical Characteristics – TA = -40°C to 105°C” on page 337.
8. Added ”Typical Characteristics – TA = -40°C to 105°C” on page 658.
9. Updated ”Ordering information” on page 20

12.3 Rev. 8284D - 06/11

1. Removed “Preliminary” from the front page
2. Updated the Table 29-16 on page 344. V_{POT} falling / Min. is 0.05V, not 0.5V

12.4 Rev. 8284C - 06/11

1. Updated ”Signature Bytes” on page 294. A, P, and PA devices have different signature (0x002) bytes.
2. Updated all ”DC Characteristics” on page 323.