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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega3290pa-au

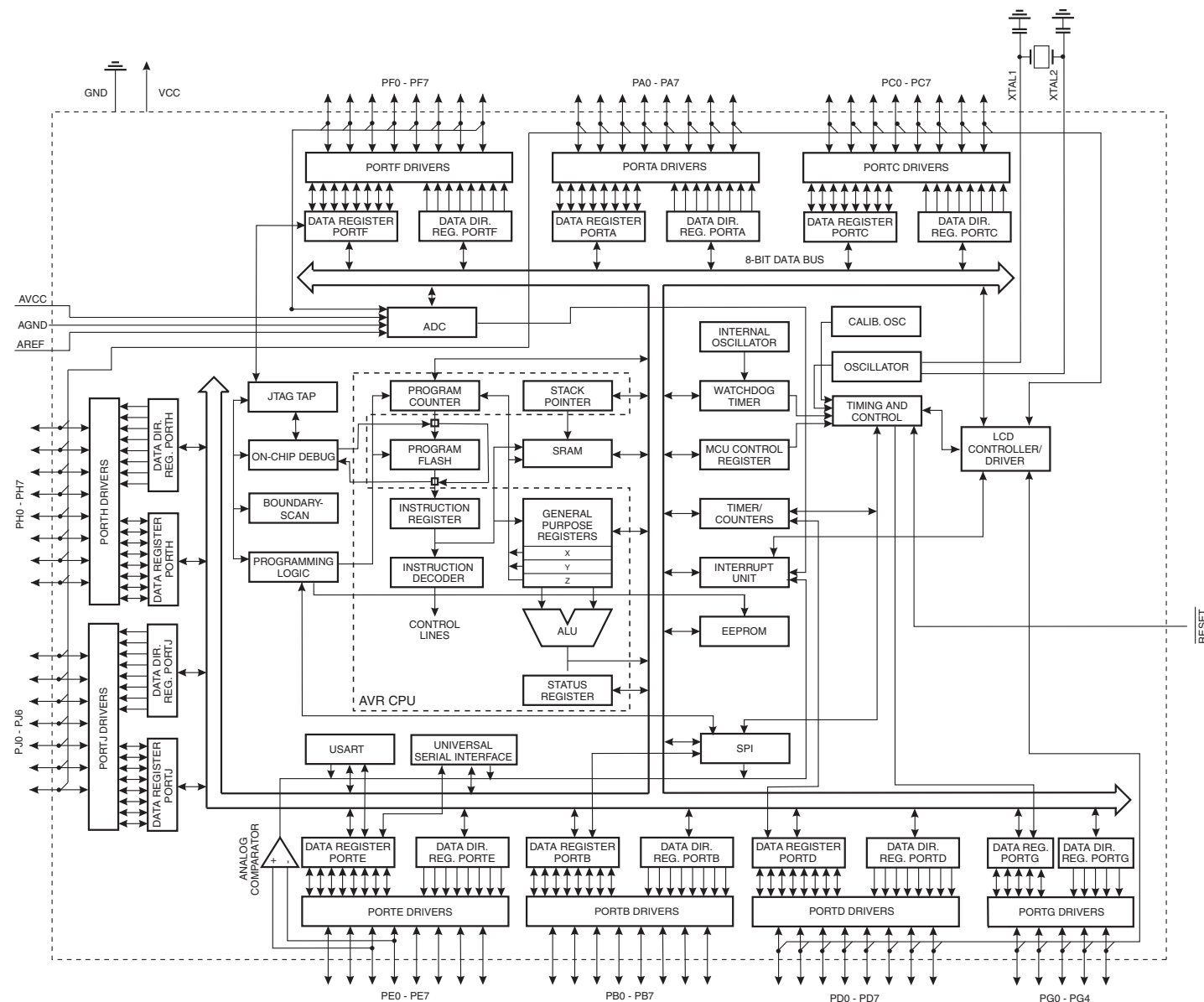
- Real Time Counter with separate oscillator
- Four PWM channels
- 8-channel, 10-bit ADC
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Universal Serial Interface with Start Condition Detector
- Programmable Watchdog Timer with Separate On-chip oscillator
- On-chip analog comparator
- Interrupt and Wake-up on pin change
- Special microcontroller features
 - Power-on reset and programmable Brown-out detection
 - Internal calibrated oscillator
 - External and internal interrupt sources
 - Five sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and packages
 - 54/69 programmable I/O lines
 - 64/100-lead TQFP, 64-pad QFN/MLF, and 64-pad DRQFN
- Speed Grade:
 - ATmega169A/169PA/649A/649P:
 - 0 - 16MHz @ 1.8 - 5.5V
 - ATmega3290A/3290PA/6490A/6490P:
 - 0 - 20MHz @ 1.8 - 5.5V
- Temperature range:
 - -40°C to 85°C industrial
- Ultra-low power consumption (picoPower® devices)
 - Active mode:
 - 1MHz, 1.8V: 215µA
 - 32kHz, 1.8V: 8µA (including oscillator)
 - 32kHz, 1.8V: 25µA (including oscillator and LCD)
 - Power-down mode:
 - 0.1µA at 1.8V
 - Power-save mode:
 - 0.6µA at 1.8V (Including 32kHz RTC)
 - 750nA at 1.8V

2. Overview

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a low-power CMOS 8-bit microcontroller based on the Atmel®AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one

2.3 Pin descriptions

The following section describes the I/O-pin special functions.

2.3.1 V_{CC}

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7...PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 72](#).

2.3.4 Port B (PB7...PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 73](#).

2.3.5 Port C (PC7...PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 76](#).

2.3.6 Port D (PD7...PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 77](#).

2.3.7 Port E (PE7...PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that

are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 79](#).

2.3.8 Port F (PF7...PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.3.9 Port G (PG5...PG0)

Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 83](#).

2.3.10 Port H (PH7...PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega3290PA/6490P as listed on [page 85](#).

2.3.11 Port J (PJ6...PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the ATmega3290PA/6490P as listed on [page 87](#).

2.3.12 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in "[System and reset characteristics](#)" on [page 332](#). Shorter pulses are not guaranteed to generate a reset.

2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.16 AREF

This is the analog reference pin for the A/D Converter.

2.3.17 LCDCAP

An external capacitor (typical > 470 nF) must be connected to the LCDCAP pin as shown in [Figure 24-2](#), if the LCD module is enabled and configured to use internal power. This capacitor acts as a reservoir for LCD power (V_{LCD}). A large capacitance reduces ripple on V_{LCD} but increases the time until V_{LCD} reaches its target value.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xB3)	OCR2A	Timer/Counter 2 Output Compare Register A								153
(0xB2)	TCNT2	Timer/Counter2								153
(0xB1)	Reserved	-	-	-	-	-	-	-	-	
(0xB0)	TCCR2A	FOC2A	WGM20	COM2A1	COM2A0	WGM21	CS22	CS21	CS20	151
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	-	-	
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	Reserved	-	-	-	-	-	-	-	-	
(0x9C)	Reserved	-	-	-	-	-	-	-	-	
(0x9B)	Reserved	-	-	-	-	-	-	-	-	
(0x9A)	Reserved	-	-	-	-	-	-	-	-	
(0x99)	Reserved	-	-	-	-	-	-	-	-	
(0x98)	Reserved	-	-	-	-	-	-	-	-	
(0x97)	Reserved	-	-	-	-	-	-	-	-	
(0x96)	Reserved	-	-	-	-	-	-	-	-	
(0x95)	Reserved	-	-	-	-	-	-	-	-	
(0x94)	Reserved	-	-	-	-	-	-	-	-	
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	Reserved	-	-	-	-	-	-	-	-	
(0x91)	Reserved	-	-	-	-	-	-	-	-	
(0x90)	Reserved	-	-	-	-	-	-	-	-	
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	Reserved	-	-	-	-	-	-	-	-	
(0x8C)	Reserved	-	-	-	-	-	-	-	-	
(0x8B)	OCR1BH	Timer/Counter1 Output Compare Register B High								130
(0x8A)	OCR1BL	Timer/Counter1 Output Compare Register B Low								130
(0x89)	OCR1AH	Timer/Counter1 Output Compare Register A High								130
(0x88)	OCR1AL	Timer/Counter1 Output Compare Register A Low								130
(0x87)	ICR1H	Timer/Counter1 Input Capture Register High								131
(0x86)	ICR1L	Timer/Counter1 Input Capture Register Low								131
(0x85)	TCNT1H	Timer/Counter1 High								130
(0x84)	TCNT1L	Timer/Counter1 Low								130
(0x83)	Reserved	-	-	-	-	-	-	-	-	
(0x82)	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-	129
(0x81)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	128
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10	126
(0x7F)	DIDR1	-	-	-	-	-	-	AIN1D	AIN0D	203
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	220
(0x7D)	Reserved	-	-	-	-	-	-	-	-	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	216
(0x7B)	ADCSRB	-	ACME	-	-	-	ADTS2	ADTS1	ADTS0	202/219
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	218
(0x79)	ADCH	ADC Data Register High								219
(0x78)	ADCL	ADC Data Register Low								219
(0x77)	Reserved	-	-	-	-	-	-	-	-	
(0x76)	Reserved	-	-	-	-	-	-	-	-	
(0x75)	Reserved	-	-	-	-	-	-	-	-	
(0x74)	Reserved	-	-	-	-	-	-	-	-	
(0x73)	PCMSK3	-	PCINT30	PCINT29	PCINT28	PCINT27	PCINT26	PCINT25	PCINT24	64

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x72)	Reserved	-	-	-	-	-	-	-	-	
(0x71)	Reserved	-	-	-	-	-	-	-	-	
(0x70)	TIMSK2	-	-	-	-	-	-	OCIE2A	TOIE2	154
(0x6F)	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1	131
(0x6E)	TIMSK0	-	-	-	-	-	-	OCIE0A	TOIE0	137
(0x6D)	PCMSK2	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	64
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	64
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	64
(0x6A)	Reserved	-	-	-	-	-	-	-	-	
(0x69)	EICRA	-	-	-	-	-	-	ISC01	ISC00	61
(0x68)	Reserved	-	-	-	-	-	-	-	-	
(0x67)	Reserved	-	-	-	-	-	-	-	-	
(0x66)	OSCCAL	Oscillator Calibration Register [CAL7...0]								38
(0x65)	Reserved	-	-	-	-	-	-	-	-	
(0x64)	PRR	-	-	-	PRLCD	PRTIM1	PRSPI	PSUSART0	PRADC	46
(0x63)	Reserved	-	-	-	-	-	-	-	-	
(0x62)	Reserved	-	-	-	-	-	-	-	-	
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0	38
(0x60)	WDTCR	-	-	-	WDCE	WDE	WDP2	WDP1	WDP0	53
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	15
0x3E (0x5E)	SPH	Stack Pointer High								17
0x3D (0x5D)	SPL	Stack Pointer Low								17
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-	
0x3B (0x5B)	Reserved	-	-	-	-	-	-	-	-	
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-	
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-	
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-	
0x37 (0x57)	SPMCSR	SPMIE	RWWWSB	-	RWWWSRE	BLBSET	PGWRT	PGERS	SPMEN	289
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-	
0x35 (0x55)	MCUCR	JTD	BODS	BODSE	PUD	-	-	IVSEL	IVCE	59/90/275
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF	53
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE	45
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-	
0x31 (0x51)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	242
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	202
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-	
0x2E (0x4E)	SPDR	SPI Data Register								165
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	164
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	163
0x2B (0x4B)	GPIOR2	General Purpose I/O Register								29
0x2A (0x4A)	GPIOR1	General Purpose I/O Register								29
0x29 (0x49)	Reserved	-	-	-	-	-	-	-	-	
0x28 (0x48)	Reserved	-	-	-	-	-	-	-	-	
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare A								138
0x26 (0x46)	TCNT0	Timer/Counter0								137
0x25 (0x45)	Reserved	-	-	-	-	-	-	-	-	
0x24 (0x44)	TCCR0A	FOC0A	WGM00	COM0A1	COM0A0	WGM01	CS02	CS01	CS00	135
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSR2	PSR10	138/155
0x22 (0x42)	EEARH	-	-	-	-	-	EEPROM Address Register High			28
0x21 (0x41)	EEARL	EEPROM Address Register Low								28
0x20 (0x40)	EEDR	EEPROM Data Register								28
0x1F (0x3F)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	28
0x1E (0x3E)	GPIOR0	General Purpose I/O Register								29
0x1D (0x3D)	EIMSK	PCIE	PCIE2	PCIE1	PCIE0	-	-	-	INT0	62
0x1C (0x3C)	EIFR	PCIF3	PCIF2	PCIF1	PCIF0	-	-	-	INTF0	63
0x1B (0x3B)	Reserved	-	-	-	-	-	-	-	-	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	
0x18 (0x38)	Reserved	-	-	-	-	-	-	-	-	
0x17 (0x37)	TIFR2	-	-	-	-	-	-	OCF2A	TOV2	154
0x16 (0x36)	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1	131
0x15 (0x35)	TIFR0	-	-	-	-	-	-	OCF0A	TOV0	138
0x14 (0x34)	PORTG	-	-	-	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	92
0x13 (0x33)	DDRG	-	-	-	DDG4	DDG3	DDG2	DDG1	DDG0	92
0x12 (0x32)	PING	-	-	PING5	PING4	PING3	PING2	PING1	PING0	92

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	92
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	92
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	92
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	91
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	92
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	92
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	91
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	91
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	91
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	91
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	91
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	91
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	90
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	90
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	91
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	90
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	90
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	90

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
JMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRs	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2

9.2 Atmel ATmega169PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
16	1.8 - 5.5V	ATmega169PA-AU ATmega169PA-AUR ⁽⁴⁾ ATmega169PA-MU ATmega169PA-MUR ⁽⁴⁾ ATmega169PA-MCH ATmega169PA-MCHR ⁽⁴⁾	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169PA-AN ATmega169PA-ANR ⁽⁴⁾ ATmega169PA-MN ATmega169PA-MNR ⁽⁴⁾	64A 64A 64M1 64M1	Extended (-40°C to 105°C) ⁽⁵⁾

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} , see [Figure 29-1 on page 330](#).
 4. Tape & Reel.
 5. See characterization specification at 105°C.

Package type	
	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0mm Exposed Pad, Quad Flat No-Lead Package (QFN)

9.5 Atmel ATmega3290A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega3290A-AU ATmega3290A-AUR ⁽⁴⁾	100A 100A	Industrial (-40°C to 85°C)
		ATmega3290A-AN ATmega3290A-ANR ⁽⁴⁾	100A 100A	Extended (-40°C to 105°C) ⁽⁵⁾

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-2 on page 330](#).
 4. Tape & Reel.
 5. See characterization specification at 105°C.

Package type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.6 Atmel ATmega3290PA

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega3290PA-AU ATmega3290PA-AUR ⁽⁴⁾	100A 100A	Industrial (-40°C to 85°C)
		ATmega3290PA-AN ATmega3290PA-ANR ⁽⁴⁾	100A 100A	Industrial (-40°C to 105°C) ⁽⁵⁾

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-2 on page 330](#).
 4. Tape & Reel.
 5. See characterization specification at 105°C.

Package type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.7 Atmel ATmega649A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
16	1.8 - 5.5V	ATmega649A-AU ATmega649A-AUR ⁽⁴⁾ ATmega649A-MU ATmega649A-MUR ⁽⁴⁾	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-1 on page 330](#).
 4. Tape & Reel.

Package type	
	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.8 Atmel ATmega649P

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
16	1.8 - 5.5 V	ATmega649P-AU ATmega649P-AUR ⁽⁴⁾ ATmega649P-MU ATmega649P-MUR ⁽⁴⁾	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-1 on page 330](#).
 4. Tape & Reel.

Package type	
	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.9 Atmel ATmega6490A

Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega6490A-AU ATmega6490A-AUR ⁽⁴⁾	100A 100A	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-2 on page 330](#).
 4. Tape & Reel.

Package type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.10 Atmel ATmega6490P

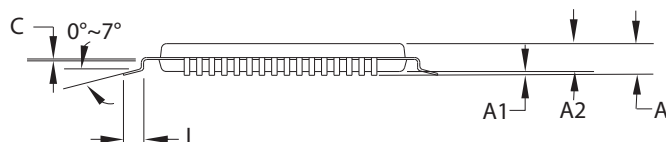
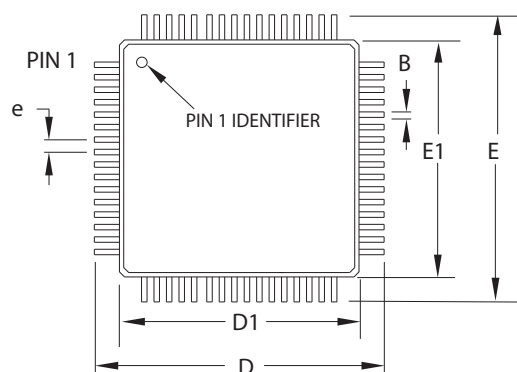
Speed [MHz] ⁽³⁾	Power supply	Ordering code ⁽²⁾	Package type ⁽¹⁾	Operational range
20	1.8 - 5.5V	ATmega6490P-AU ATmega6490P-AUR ⁽⁴⁾	100A 100A	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
 3. For Speed vs. V_{CC} see [Figure 29-2 on page 330](#).
 4. Tape & Reel.

Package Type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

10. Packaging Information

10.1 64A



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30–	0.45		
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20



2325 Orchard Parkway
San Jose, CA 95131

TITLE

64A, 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness,
0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

64A

REV.

C

11. Errata

11.1 Atmel ATmega169A

No known errata

11.2 Atmel ATmega169A/169PA Rev. A to F

Not sampled.

11.3 Atmel ATmega169PA Rev. G

No known errata.

11.4 Atmel ATmega329A/329PA rev. A

- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Using BOD disable will make the chip reset

1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. Using BOD disable will make the chip reset

If the part enters sleep with the BOD turned off with the BOD disable option enabled, a BOD reset will be generated at wakeup and the chip will reset.

Problem Fix/Workaround

Do not use BOD disable

11.5 Atmel ATmega329A/329PA rev. B

- Interrupts may be lost when writing the timer registers in the asynchronous timer

1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

12.5 Rev. 8284B - 03/11

1. Updated the datasheet according to the Atmel new Brand Style Guide.
2. Updated all ["Ordering information" on page 20](#).
3. Updated ["Packaging Information" on page 30](#).

12.6 Rev. 8284A - 10/10

1. Initial revision



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