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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

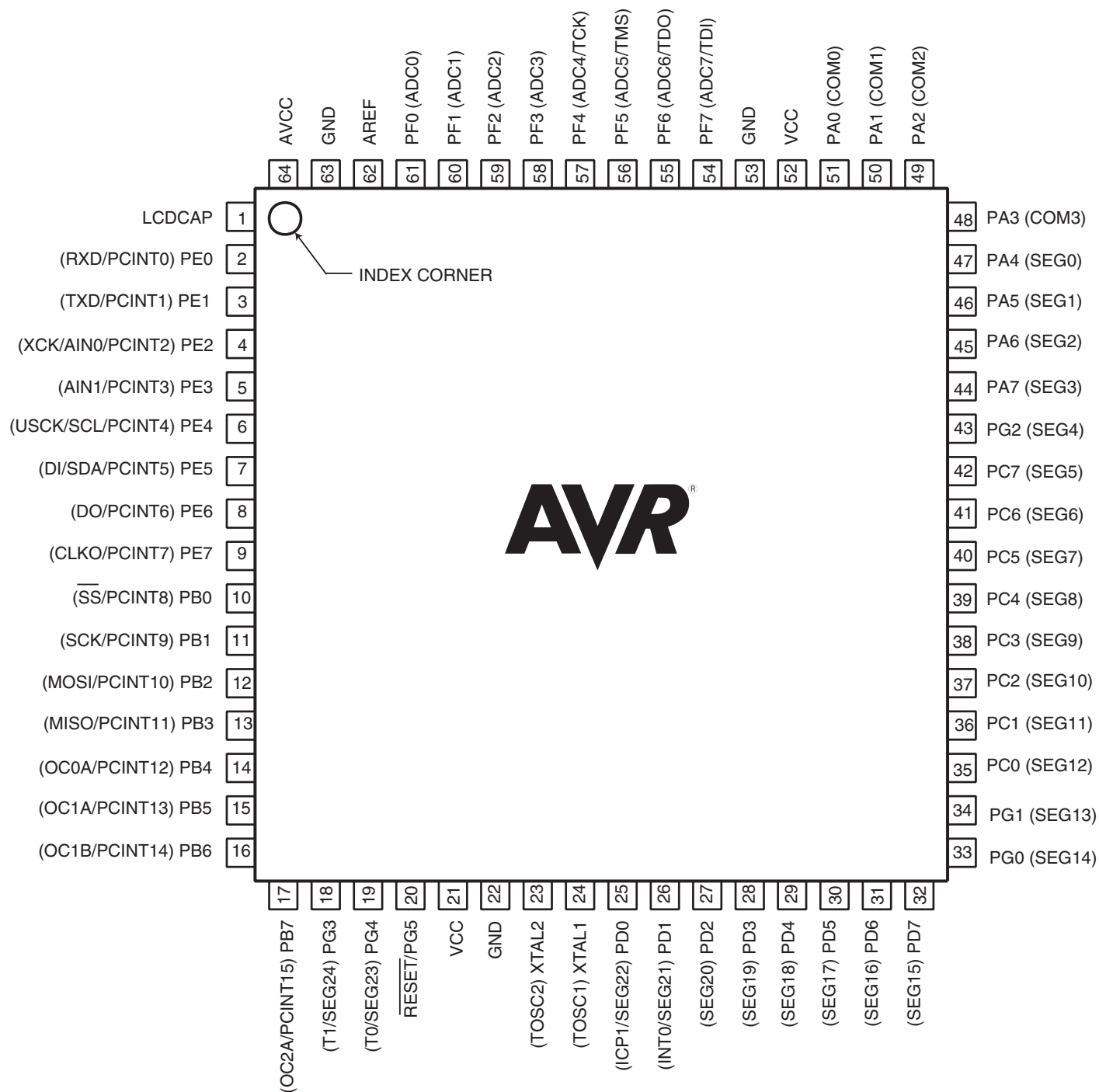
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atmega649a-mu">https://www.e-xfl.com/product-detail/microchip-technology/atmega649a-mu</a>

- Real Time Counter with separate oscillator
- Four PWM channels
- 8-channel, 10-bit ADC
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Universal Serial Interface with Start Condition Detector
- Programmable Watchdog Timer with Separate On-chip oscillator
- On-chip analog comparator
- Interrupt and Wake-up on pin change
- Special microcontroller features
  - Power-on reset and programmable Brown-out detection
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Five sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and packages
  - 54/69 programmable I/O lines
  - 64/100-lead TQFP, 64-pad QFN/MLF, and 64-pad DRQFN
- Speed Grade:
  - ATmega169A/169PA/649A/649P:
    - 0 - 16MHz @ 1.8 - 5.5V
  - ATmega3290A/3290PA/6490A/6490P:
    - 0 - 20MHz @ 1.8 - 5.5V
- Temperature range:
  - -40°C to 85°C industrial
- Ultra-low power consumption (picoPower® devices)
  - Active mode:
    - 1MHz, 1.8V: 215µA
    - 32kHz, 1.8V: 8µA (including oscillator)
    - 32kHz, 1.8V: 25µA (including oscillator and LCD)
  - Power-down mode:
    - 0.1µA at 1.8V
  - Power-save mode:
    - 0.6µA at 1.8V (Including 32kHz RTC)
    - 750nA at 1.8V

# 1. Pin configurations

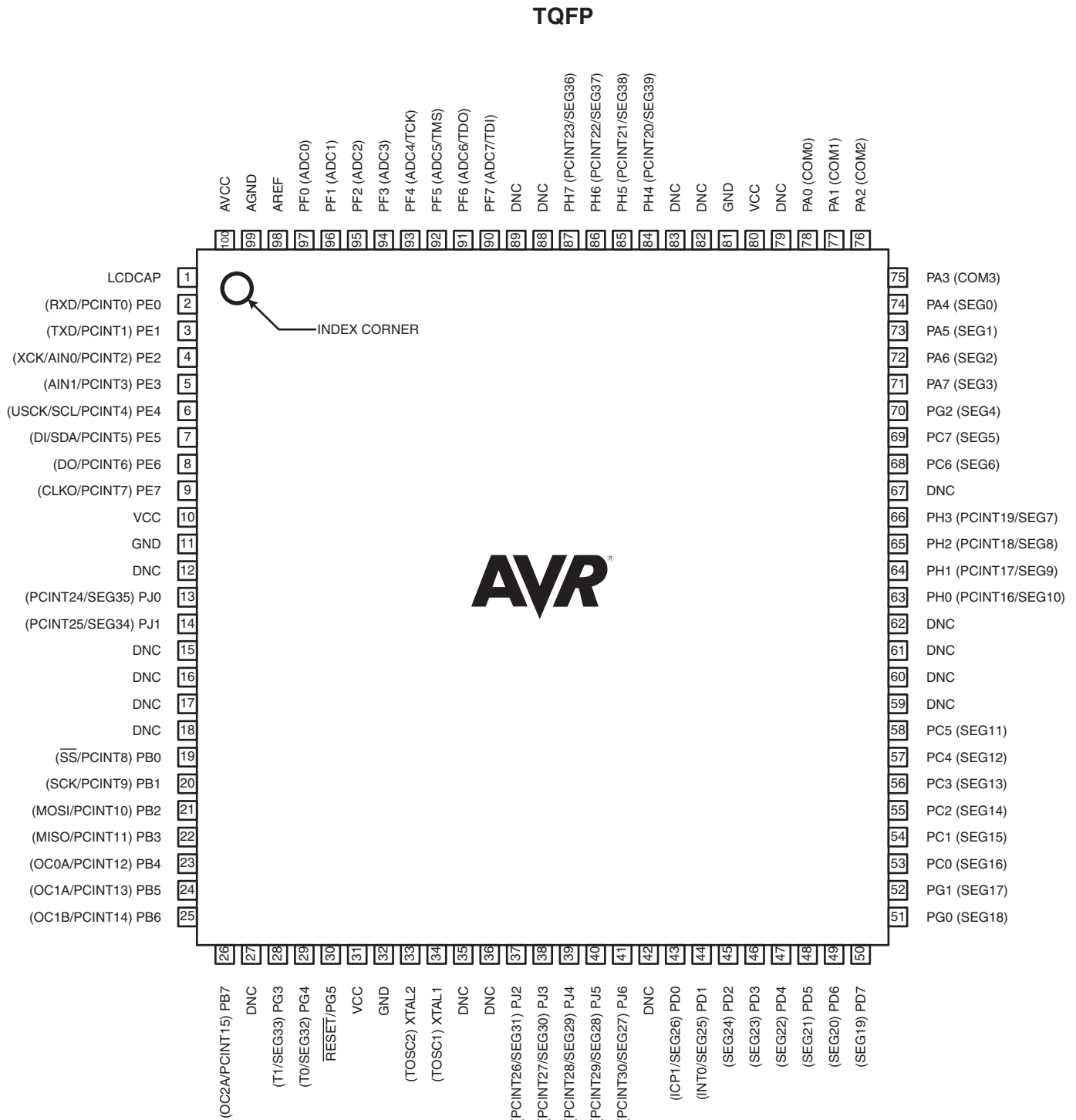
## 1.1 Pinout - 64A (TQFP) and 64M1 (QFN/MLF)

Figure 1-1. Pinout Atmel ATmega169A/ATmega169PA/ATmega329A/ATmega329PA/ATmega649A/ATmega649P.



## 1.2 Pinout - 100A (TQFP)

Figure 1-2. Pinout Atmel ATmega3290A/ATmega3290PA/ATmega6490A/ATmega6490P.



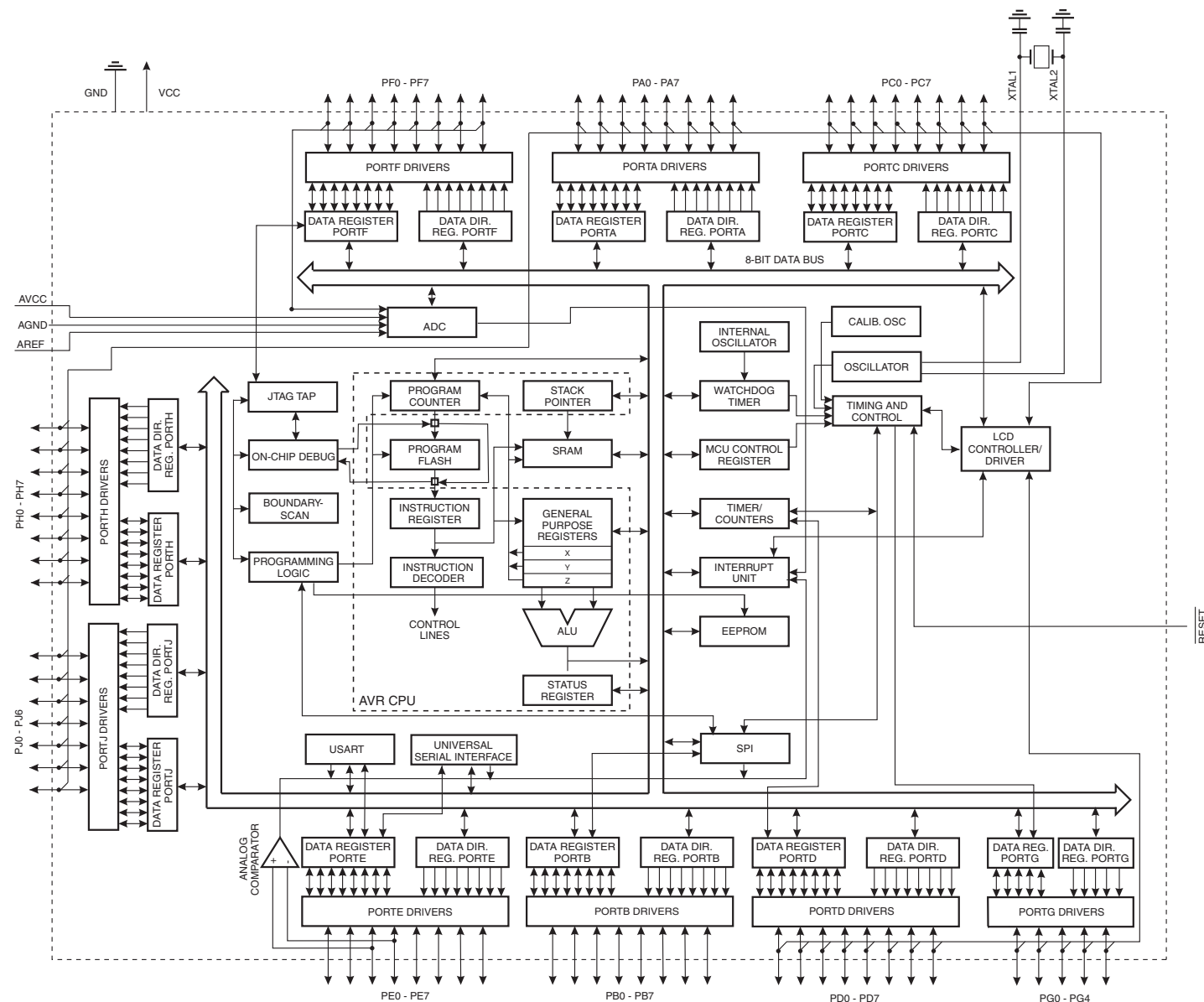
Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

## 2. Overview

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a low-power CMOS 8-bit microcontroller based on the Atmel®AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

### 2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one

## 2.2 Comparison between Atmel

### ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P

Table 2-1. Differences between: ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P.

ATmega169A	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega169PA	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega329A	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega329PA	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega3290A	32Kbytes	1Kbyte	2Kbyte	4 × 40
ATmega3290PA	32Kbyte	1Kbyte	2Kbyte	4 × 40
ATmega649A	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega649P	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega6490A	64Kbyte	2Kbyte	4Kbyte	4 × 40
ATmega6490P	64Kbyte	2Kbyte	4Kbyte	4 × 40

## 2.3 Pin descriptions

The following section describes the I/O-pin special functions.

### 2.3.1 $V_{CC}$

Digital supply voltage.

### 2.3.2 GND

Ground.

### 2.3.3 Port A (PA7...PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 72](#).

### 2.3.4 Port B (PB7...PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 73](#).

### 2.3.5 Port C (PC7...PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 76](#).

### 2.3.6 Port D (PD7...PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on [page 77](#).

### 2.3.7 Port E (PE7...PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that

### 2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to  $V_{CC}$ , even if the ADC is not used. If the ADC is used, it should be connected to  $V_{CC}$  through a low-pass filter.

### 2.3.16 AREF

This is the analog reference pin for the A/D Converter.

### 2.3.17 LCDCAP

An external capacitor (typical > 470 nF) must be connected to the LCDCAP pin as shown in [Figure 24-2](#), if the LCD module is enabled and configured to use internal power. This capacitor acts as a reservoir for LCD power ( $V_{LCD}$ ). A large capacitance reduces ripple on  $V_{LCD}$  but increases the time until  $V_{LCD}$  reaches its target value.



### 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

### 4. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

### 5. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBR”, “SBRC”, “SBR”, and “CBR”.

### 6. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the QTouch and QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: [www.atmel.com/qtouchlibrary](http://www.atmel.com/qtouchlibrary). For implementation details and other information, refer to the [Atmel QTouch Library User Guide](#) - also available for download from the Atmel website.

### 7. Register summary

Note: Registers with bold type only available in Atmel ATmega3290A/3290PA/6490A/6490P.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	<b>LCDDR19</b>	<b>SEG339</b>	<b>SEG338</b>	<b>SEG337</b>	<b>SEG336</b>	<b>SEG335</b>	<b>SEG334</b>	<b>SEG333</b>	<b>SEG332</b>	<a href="#">236</a>
(0xFE)	LCDDR18	<b>SEG331</b>	<b>SEG330</b>	<b>SEG329</b>	<b>SEG328</b>	<b>SEG327</b>	<b>SEG326</b>	<b>SEG325</b>	SEG324	<a href="#">236</a>
(0xFD)	LCDDR17	SEG323	SEG322	SEG321	SEG320	SEG319	SEG318	SEG317	SEG316	<a href="#">236</a>
(0xFC)	LCDDR16	SEG315	SEG314	SEG313	SEG312	SEG311	SEG310	SEG309	SEG308	<a href="#">236</a>
(0xFB)	LCDDR15	SEG307	SEG306	SEG305	SEG304	SEG303	SEG302	SEG301	SEG300	<a href="#">236</a>
(0xFA)	<b>LCDDR14</b>	<b>SEG239</b>	<b>SEG238</b>	<b>SEG237</b>	<b>SEG236</b>	<b>SEG235</b>	<b>SEG234</b>	<b>SEG233</b>	<b>SEG232</b>	<a href="#">236</a>
(0xF9)	LCDDR13	<b>SEG231</b>	<b>SEG230</b>	<b>SEG229</b>	<b>SEG228</b>	<b>SEG227</b>	<b>SEG226</b>	<b>SEG225</b>	SEG224	<a href="#">236</a>
(0xF8)	LCDDR12	SEG223	SEG222	SEG221	SEG220	SEG219	SEG218	SEG217	SEG216	<a href="#">236</a>
(0xF7)	LCDDR11	SEG215	SEG214	SEG213	SEG212	SEG211	SEG210	SEG209	SEG208	<a href="#">236</a>
(0xF6)	LCDDR10	SEG207	SEG206	SEG205	SEG204	SEG203	SEG202	SEG201	SEG200	<a href="#">236</a>
(0xF5)	<b>LCDDR09</b>	<b>SEG139</b>	<b>SEG138</b>	<b>SEG137</b>	<b>SEG136</b>	<b>SEG135</b>	<b>SEG134</b>	<b>SEG133</b>	<b>SEG132</b>	<a href="#">236</a>

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xF4)	LCDDR08	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125	SEG124	236
(0xF3)	LCDDR07	SEG123	SEG122	SEG121	SEG120	SEG119	SEG118	SEG117	SEG116	236
(0xF2)	LCDDR06	SEG115	SEG114	SEG113	SEG112	SEG111	SEG110	SEG109	SEG108	236
(0xF1)	LCDDR05	SEG107	SEG106	SEG105	SEG104	SEG103	SEG102	SEG101	SEG100	236
(0xF0)	LCDDR04	SEG039	SEG038	SEG037	SEG036	SEG035	SEG034	SEG033	SEG032	236
(0xEF)	LCDDR03	SEG031	SEG030	SEG029	SEG028	SEG027	SEG026	SEG025	SEG024	236
(0xEE)	LCDDR02	SEG023	SEG022	SEG021	SEG020	SEG019	SEG018	SEG017	SEG016	236
(0xED)	LCDDR01	SEG015	SEG014	SEG013	SEG012	SEG011	SEG010	SEG009	SEG008	236
(0xEC)	LCDDR00	SEG007	SEG006	SEG005	SEG004	SEG003	SEG002	SEG001	SEG000	236
(0xEB)	Reserved	-	-	-	-	-	-	-	-	
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	LCDDCR	LCDDC2	LCDDC1	LCDDC0	LCDMDT	LCDCC3	LCDCC2	LCDCC1	LCDCC0	234
(0xE6)	LCDFRR	-	LCDPS2	LCDPS1	LCDPS0	-	LCDCCD2	LCDCCD1	LCDCCD0	233
(0xE5)	LCDCRB	LCDCS	LCD2B	LCDMUX1	LCDMUX0	LCDPM3	LCDPM2	LCDPM1	LCDPM0	232
(0xE4)	LCD CRA	LCDEN	LCDAB	-	LCDIF	LCDIE	LCD BD	LCDCCD	LCD BL	231
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	-	-	-	-	-	-	-	-	
(0xDD)	PORTJ	-	PORTJ6	PORTJ5	PORTJ4	PORTJ3	PORTJ2	PORTJ1	PORTJ0	93
(0xDC)	DDRJ	-	DDJ6	DDJ5	DDJ4	DDJ3	DDJ2	DDJ1	DDJ0	93
(0xDB)	PINJ	-	PINJ6	PINJ5	PINJ4	PINJ3	PINJ2	PINJ1	PINJ0	93
(0xDA)	PORTH	PORTH7	PORTH6	PORTH5	PORTH4	PORTH3	PORTH2	PORTH1	PORTH0	93
(0xD9)	DDRH	DDH7	DDH6	DDH5	DDH4	DDH3	DDH2	DDH1	DDH0	93
(0xD8)	PINH	PINH7	PINH6	PINH5	PINH4	PINH3	PINH2	PINH1	PINH0	93
(0xD7)	Reserved	-	-	-	-	-	-	-	-	
(0xD6)	Reserved	-	-	-	-	-	-	-	-	
(0xD5)	Reserved	-	-	-	-	-	-	-	-	
(0xD4)	Reserved	-	-	-	-	-	-	-	-	
(0xD3)	Reserved	-	-	-	-	-	-	-	-	
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	Reserved	-	-	-	-	-	-	-	-	
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	Reserved	-	-	-	-	-	-	-	-	
(0xCD)	Reserved	-	-	-	-	-	-	-	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	-	-	-	-	-	-	-	
(0xC8)	Reserved	-	-	-	-	-	-	-	-	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	UDR0	USART0 Data Register								186
(0xC5)	UBRR0H	USART0 Baud Rate Register High								190
(0xC4)	UBRR0L	USART0 Baud Rate Register Low								190
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	UCSR0C	-	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	189
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	188
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	187
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	Reserved	-	-	-	-	-	-	-	-	
(0xBC)	Reserved	-	-	-	-	-	-	-	-	
(0xBB)	Reserved	-	-	-	-	-	-	-	-	
(0xBA)	USIDR	USI Data Register								197
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	198
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	198
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	-	-	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB	153
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	Reserved	-	-	-	-	-	-	-	-	

## 8. Instruction set summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>ARITHMETIC AND LOGIC INSTRUCTIONS</b>					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	RdI,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	RdI,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) \ll 1$	Z,C	2
<b>BRANCH INSTRUCTIONS</b>					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
JMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	4
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRs	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2

## 9.2 Atmel ATmega169PA

Speed [MHz] <sup>(3)</sup>	Power supply	Ordering code <sup>(2)</sup>	Package type <sup>(1)</sup>	Operational range
16	1.8 - 5.5V	ATmega169PA-AU ATmega169PA-AUR <sup>(4)</sup> ATmega169PA-MU ATmega169PA-MUR <sup>(4)</sup> ATmega169PA-MCH ATmega169PA-MCHR <sup>(4)</sup>	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169PA-AN ATmega169PA-ANR <sup>(4)</sup> ATmega169PA-MN ATmega169PA-MNR <sup>(4)</sup>	64A 64A 64M1 64M1	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 29-1 on page 330](#).
  4. Tape & Reel.
  5. See characterization specification at 105°C.

Package type	
	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0mm Exposed Pad, Quad Flat No-Lead Package (QFN)

## 9.8 Atmel ATmega649P

Speed [MHz] <sup>(3)</sup>	Power supply	Ordering code <sup>(2)</sup>	Package type <sup>(1)</sup>	Operational range
16	1.8 - 5.5 V	ATmega649P-AU ATmega649P-AUR <sup>(4)</sup> ATmega649P-MU ATmega649P-MUR <sup>(4)</sup>	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$  see [Figure 29-1 on page 330](#).
  4. Tape & Reel.

Package type	
	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

## 9.10 Atmel ATmega6490P

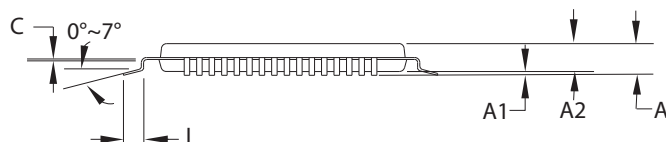
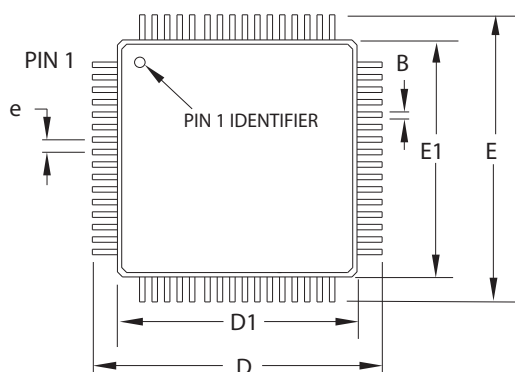
Speed [MHz] <sup>(3)</sup>	Power supply	Ordering code <sup>(2)</sup>	Package type <sup>(1)</sup>	Operational range
20	1.8 - 5.5V	ATmega6490P-AU ATmega6490P-AUR <sup>(4)</sup>	100A 100A	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$  see [Figure 29-2 on page 330](#).
  4. Tape & Reel.

Package Type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

## 10. Packaging Information

### 10.1 64A



COMMON DIMENSIONS  
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30–	0.45		
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:

1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20



2325 Orchard Parkway  
San Jose, CA 95131

TITLE

64A, 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness,  
0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

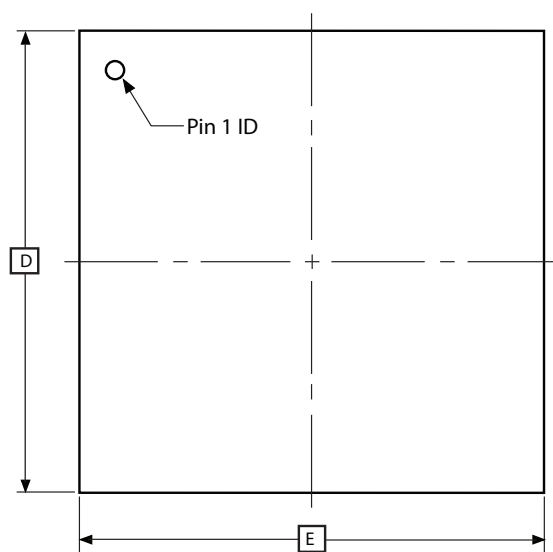
DRAWING NO.

64A

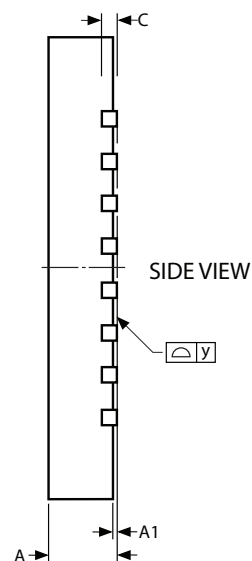
REV.

C

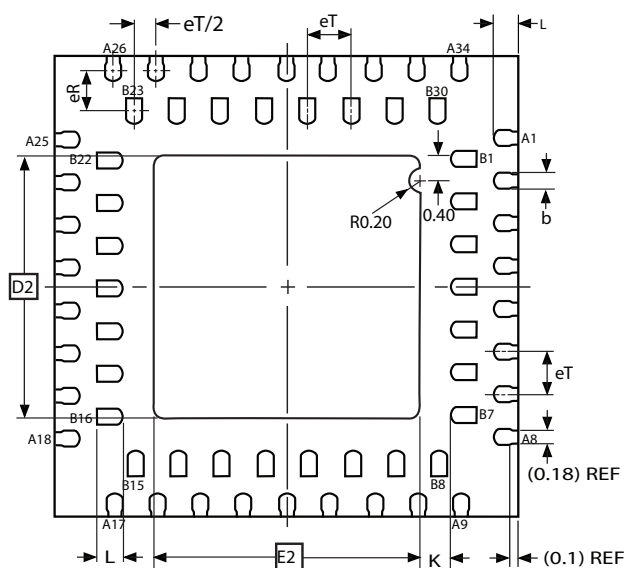
### 10.3 64MC



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: 1. The terminal #1 ID is a Laser-marked Feature.

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.28	
C	0.20 REF			
D	6.90	7.00	7.10	
D2	3.95	4.00	4.05	
E	6.90	7.00	7.10	
E2	3.95	4.00	4.05	
eT	–	0.65	–	
eR	–	0.65	–	
K	0.20	–	–	(REF)
L	0.35	0.40	0.45	
y	0.00	–	0.075	

10/3/07



Package Drawing Contact:  
packagedrawings@atmel.com

TITLE
64MC, 64QFN (2-Row Staggered), 7 x 7 x 1.00 mm Body, 4.0 x 4.0 mm Exposed Pad, Quad Flat No Lead Package

GPC
-----

ZXC

DRAWING NO.
-------------

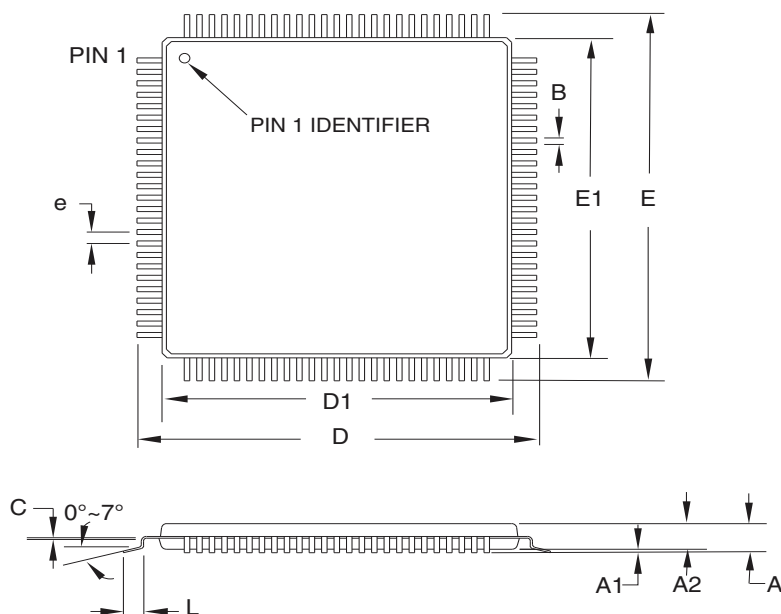
64MC

REV.

A



## 10.4 100A



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	—	0.27	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.50 TYP			

**Notes:**

1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08mm maximum.

2014-02-05

TITLE		DRAWING NO.	REV.
<b>Atmel</b> Package Drawing Contact: <a href="mailto:packagedrawings@atmel.com">packagedrawings@atmel.com</a>		100A	E
<b>100A</b> , 100-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)			

## 11. Errata

### 11.1 Atmel ATmega169A

No known errata

### 11.2 Atmel ATmega169A/169PA Rev. A to F

Not sampled.

### 11.3 Atmel ATmega169PA Rev. G

No known errata.

### 11.4 Atmel ATmega329A/329PA rev. A

- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Using BOD disable will make the chip reset

#### 1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

##### Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCR<sub>x</sub>), asynchronous Timer Counter Register (TCNT<sub>x</sub>), or asynchronous Output Compare Register (OCR<sub>x</sub>).

#### 2. Using BOD disable will make the chip reset

If the part enters sleep with the BOD turned off with the BOD disable option enabled, a BOD reset will be generated at wakeup and the chip will reset.

##### Problem Fix/Workaround

Do not use BOD disable

### 11.5 Atmel ATmega329A/329PA rev. B

- Interrupts may be lost when writing the timer registers in the asynchronous timer

#### 1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNT<sub>x</sub>) is 0x00.

##### Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCR<sub>x</sub>), asynchronous Timer Counter Register (TCNT<sub>x</sub>), or asynchronous Output Compare Register (OCR<sub>x</sub>).

## 11.6 Atmel ATmega329A/329PA rev. C

- Interrupts may be lost when writing the timer registers in the asynchronous timer

### 1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

#### Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

## 11.7 Atmel ATmega3290A/3290PA rev. A

- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Using BOD disable will make the chip reset

### 1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

#### Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

### 2. Using BOD disable will make the chip reset

If the part enters sleep with the BOD turned off with the BOD disable option enabled, a BOD reset will be generated at wakeup and the chip will reset.

#### Problem Fix/Workaround

Do not use BOD disable

## 11.8 Atmel ATmega3290A/3290PA rev. B

- Interrupts may be lost when writing the timer registers in the asynchronous timer

### 1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

#### Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

## 12.5 Rev. 8284B - 03/11

1. Updated the datasheet according to the Atmel new Brand Style Guide.
2. Updated all ["Ordering information" on page 20](#).
3. Updated ["Packaging Information" on page 30](#).

## 12.6 Rev. 8284A - 10/10

1. Initial revision



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