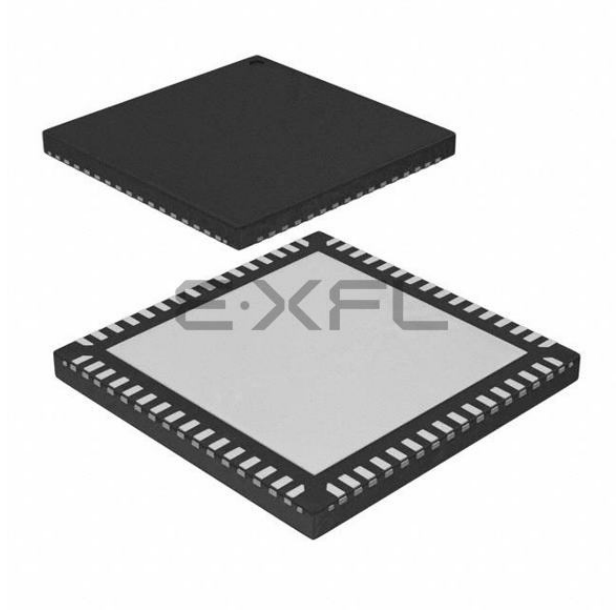

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

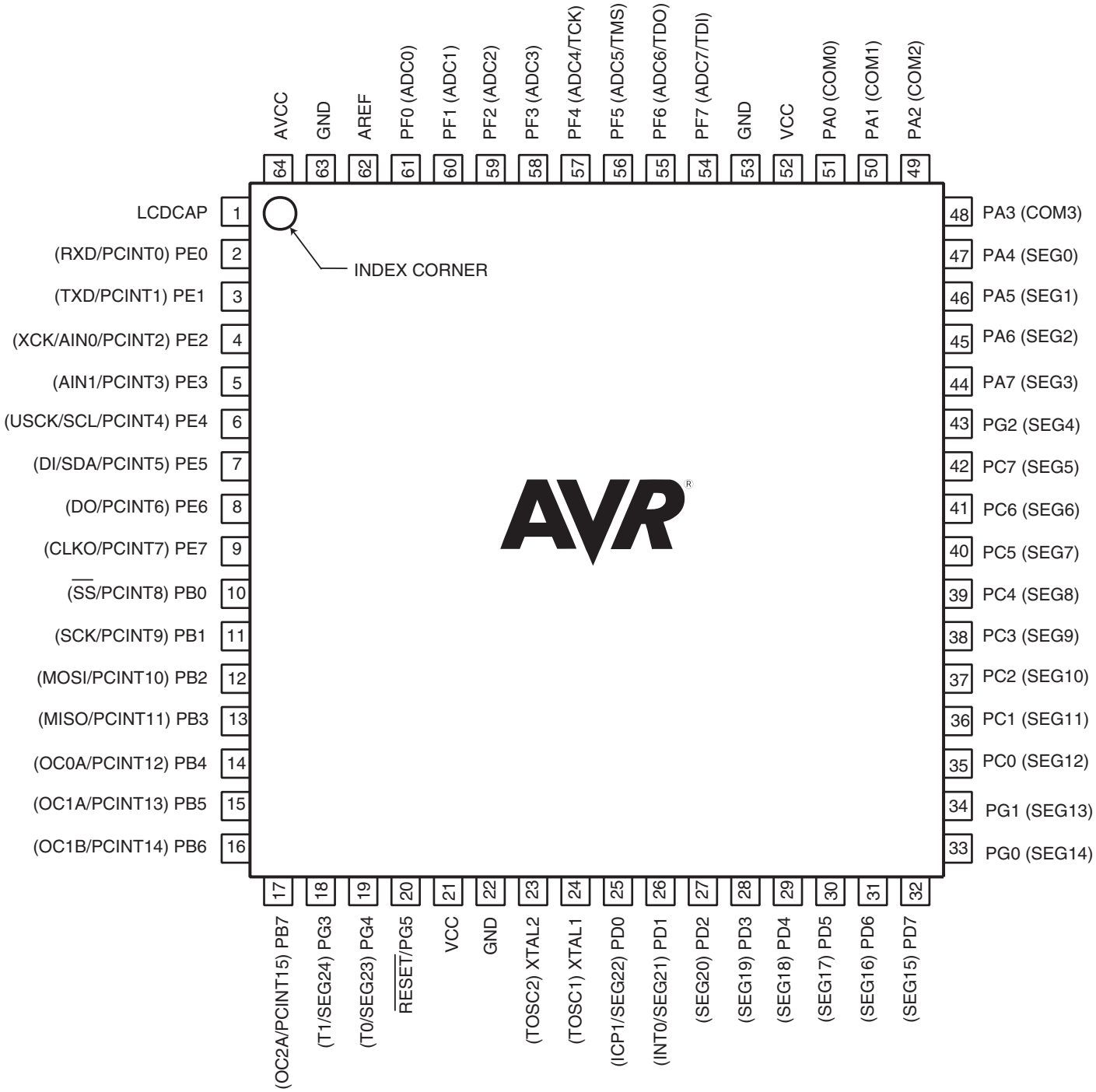
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega649p-mur

1. Pin configurations

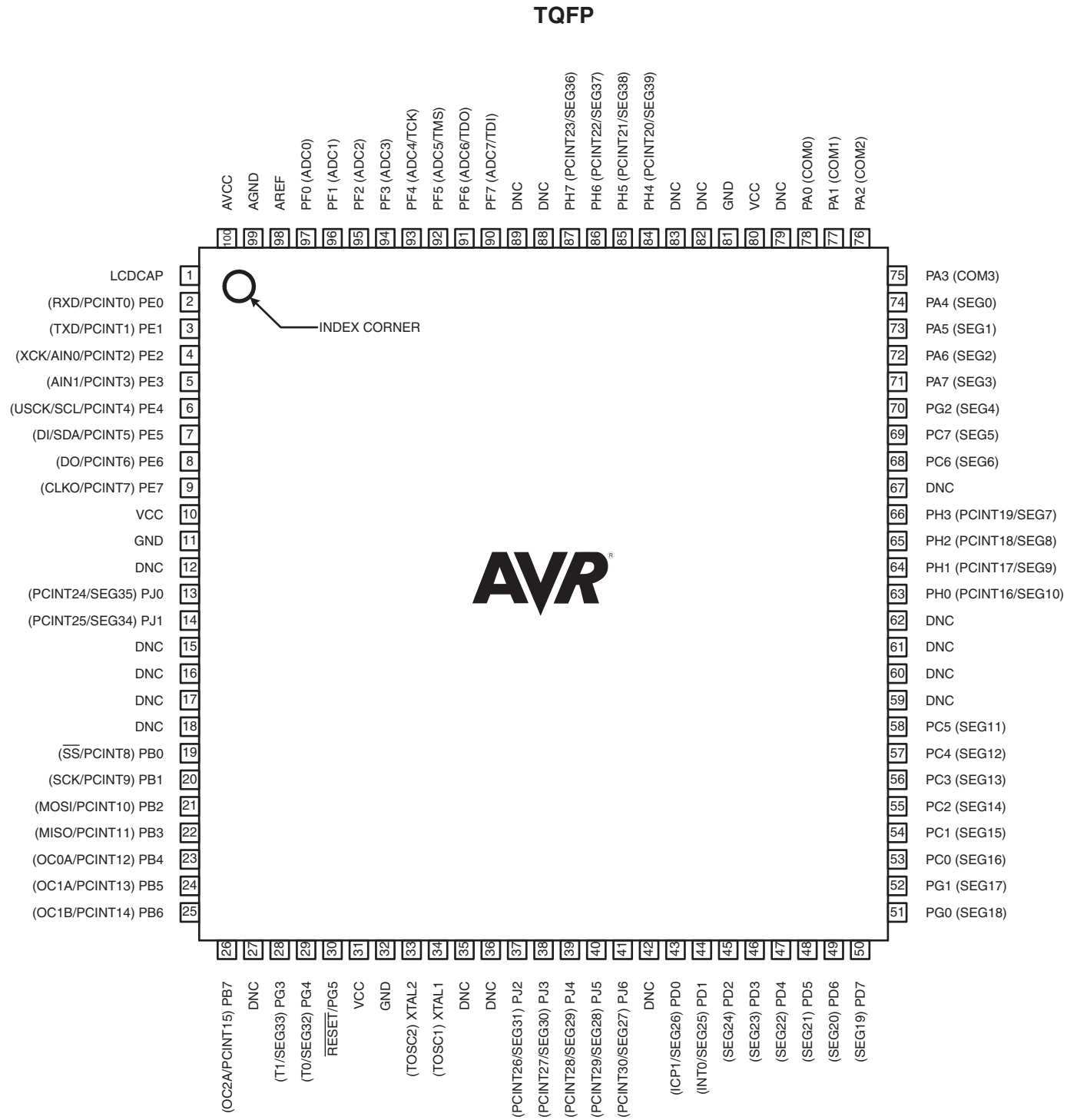
1.1 Pinout - 64A (TQFP) and 64M1 (QFN/MLF)

Figure 1-1. Pinout Atmel ATmega169A/ATmega169PA/ATmega329A/ATmega329PA/ATmega649A/ATmega649P.



1.2 Pinout - 100A (TQFP)

Figure 1-2. Pinout Atmel ATmega3290A/ATmega3290PA/ATmega6490A/ATmega6490P.



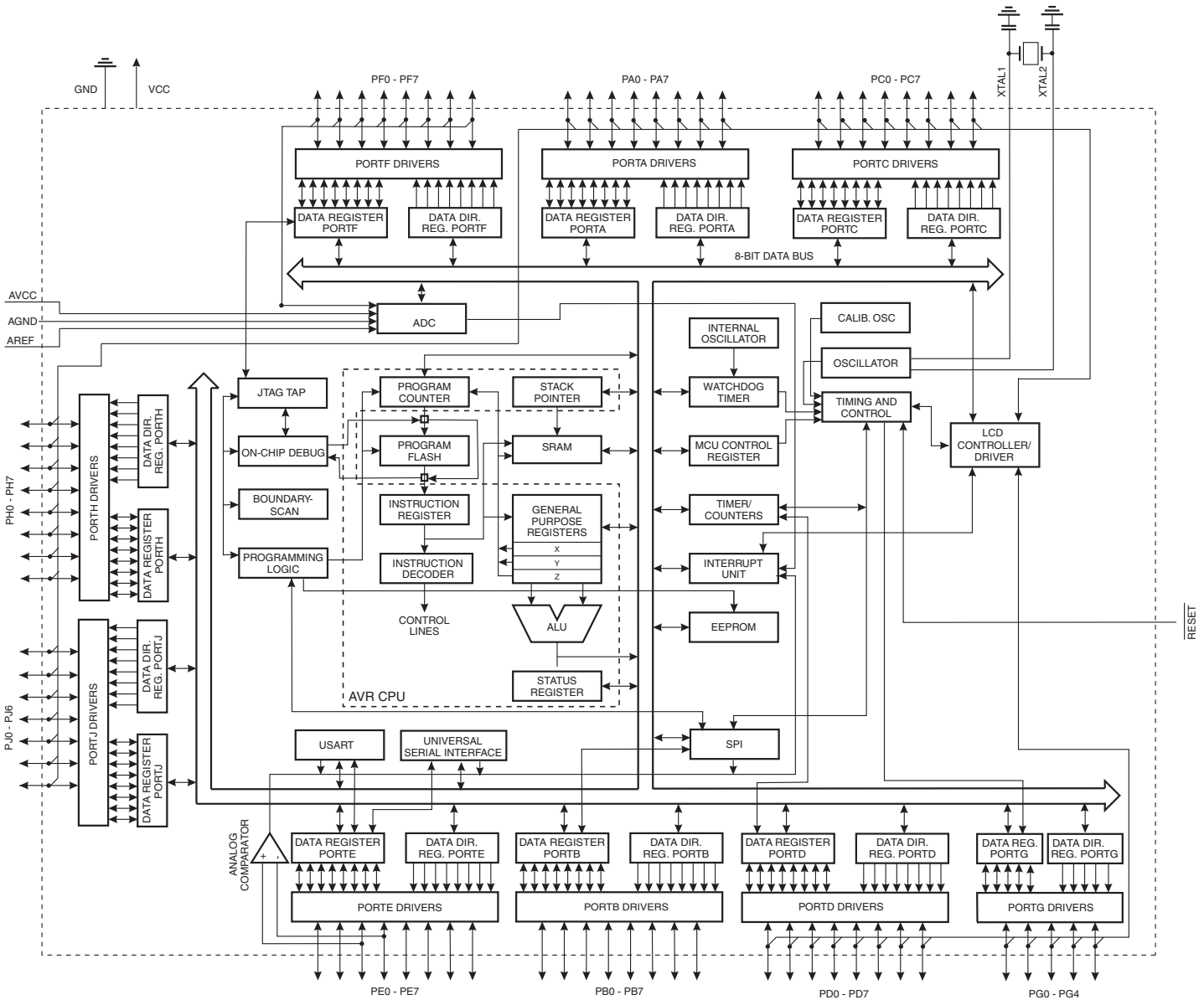
Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

2. Overview

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a low-power CMOS 8-bit microcontroller based on the Atmel®AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one

2.2 Comparison between Atmel ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P

Table 2-1. Differences between: ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P.

ATmega169A	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega169PA	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega329A	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega329PA	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega3290A	32Kbytes	1Kbyte	2Kbyte	4 × 40
ATmega3290PA	32Kbyte	1Kbyte	2Kbyte	4 × 40
ATmega649A	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega649P	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega6490A	64Kbyte	2Kbyte	4Kbyte	4 × 40
ATmega6490P	64Kbyte	2Kbyte	4Kbyte	4 × 40

are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 79.

2.3.8 Port F (PF7...PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.3.9 Port G (PG5...PG0)

Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 83.

2.3.10 Port H (PH7...PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 85.

2.3.11 Port J (PJ6...PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 87.

2.3.12 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in ”System and reset characteristics” on page 332. Shorter pulses are not guaranteed to generate a reset.

2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.16 AREF

This is the analog reference pin for the A/D Converter.

2.3.17 LCDCAP

An external capacitor (typical > 470 nF) must be connected to the LCDCAP pin as shown in Figure 24-2, if the LCD module is enabled and configured to use internal power. This capacitor acts as a reservoir for LCD power (V_{LCD}). A large capacitance reduces ripple on V_{LCD} but increases the time until V_{LCD} reaches its target value.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xF4)	LCDDR08	**SEG131**	**SEG130**	**SEG129**	**SEG128**	**SEG127**	**SEG126**	**SEG125**	SEG124	236
(0xF3)	LCDDR07	SEG123	SEG122	SEG121	SEG120	SEG119	SEG118	SEG117	SEG116	236
(0xF2)	LCDDR06	SEG115	SEG114	SEG113	SEG112	SEG111	SEG110	SEG109	SEG108	236
(0xF1)	LCDDR05	SEG107	SEG106	SEG105	SEG104	SEG103	SEG102	SEG101	SEG100	236
(0xF0)	**LCDDR04**	**SEG039**	**SEG038**	**SEG037**	**SEG036**	**SEG035**	**SEG034**	**SEG033**	**SEG032**	236
(0xEF)	LCDDR03	**SEG031**	**SEG030**	**SEG029**	**SEG028**	**SEG027**	**SEG026**	**SEG025**	SEG024	236
(0xEE)	LCDDR02	SEG023	SEG022	SEG021	SEG020	SEG019	SEG018	SEG017	SEG016	236
(0xED)	LCDDR01	SEG015	SEG014	SEG013	SEG012	SEG011	SEG010	SEG009	SEG008	236
(0xEC)	LCDDR00	SEG007	SEG006	SEG005	SEG004	SEG003	SEG002	SEG001	SEG000	236
(0xEB)	Reserved	-	-	-	-	-	-	-	-	
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	LCDCCR	LCDDC2	LCDDC1	LCDDC0	LCDMDT	LCDCC3	LCDCC2	LCDCC1	LCDCC0	234
(0xE6)	LCDFRR	-	LCDPS2	LCDPS1	LCDPS0	-	LCDCD2	LCDCD1	LCDCD0	233
(0xE5)	LCDCRB	LCDCS	LCD2B	LCDMUX1	LCDMUX0	**LCDPM3**	LCDPM2	LCDPM1	LCDPM0	232
(0xE4)	LCDCRA	LCDEN	LCDAB	-	LCDIF	LCDIE	LCDBD	LCDCCD	LCDBL	231
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	-	-	-	-	-	-	-	-	
(0xDD)	**PORTJ**	**-**	**PORTJ6**	**PORTJ5**	**PORTJ4**	**PORTJ3**	**PORTJ2**	**PORTJ1**	**PORTJ0**	93
(0xDC)	**DDRJ**	**-**	**DDJ6**	**DDJ5**	**DDJ4**	**DDJ3**	**DDJ2**	**DDJ1**	**DDJ0**	93
(0xDB)	**PINJ**	**-**	**PINJ6**	**PINJ5**	**PINJ4**	**PINJ3**	**PINJ2**	**PINJ1**	**PINJ0**	93
(0xDA)	**PORTH**	**PORTH7**	**PORTH6**	**PORTH5**	**PORTH4**	**PORTH3**	**PORTH2**	**PORTH1**	**PORTH0**	93
(0xD9)	**DDRH**	**DDH7**	**DDH6**	**DDH5**	**DDH4**	**DDH3**	**DDH2**	**DDH1**	**DDH0**	93
(0xD8)	**PINH**	**PINH7**	**PINH6**	**PINH5**	**PINH4**	**PINH3**	**PINH2**	**PINH1**	**PINH0**	93
(0xD7)	Reserved	-	-	-	-	-	-	-	-	
(0xD6)	Reserved	-	-	-	-	-	-	-	-	
(0xD5)	Reserved	-	-	-	-	-	-	-	-	
(0xD4)	Reserved	-	-	-	-	-	-	-	-	
(0xD3)	Reserved	-	-	-	-	-	-	-	-	
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	Reserved	-	-	-	-	-	-	-	-	
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	Reserved	-	-	-	-	-	-	-	-	
(0xCD)	Reserved	-	-	-	-	-	-	-	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	-	-	-	-	-	-	-	
(0xC8)	Reserved	-	-	-	-	-	-	-	-	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	UDR0	USART0 Data Register								186
(0xC5)	UBRR0H					USART0 Baud Rate Register High				190
(0xC4)	UBRR0L	USART0 Baud Rate Register Low								190
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	UCSR0C	-	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	189
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	188
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	187
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	Reserved	-	-	-	-	-	-	-	-	
(0xBC)	Reserved	-	-	-	-	-	-	-	-	
(0xBB)	Reserved	-	-	-	-	-	-	-	-	
(0xBA)	USIDR	USI Data Register								197
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	198
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	198
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	-	-	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB	153
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	Reserved	-	-	-	-	-	-	-	-	

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	92
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	92
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	92
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	91
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	92
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	92
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	91
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	91
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	91
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	91
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	91
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	91
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	90
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	90
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	91
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	90
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	90
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	90

Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

9. Ordering information

9.1 Atmel ATmega169A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5V	ATmega169A-AU ATmega169A-AUR (4) ATmega169A-MU ATmega169A-MUR (4) ATmega169A-MCH ATmega169A-MCHR (4)	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169A-AN ATmega169A-ANR (4) ATmega169A-MN ATmega169A-MNR (4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 29-1 on page 330.
4. Tape & Reel.

Package type	
	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

9.2 Atmel ATmega169PA

Speed [MHz] [3]	Power supply	Ordering code [2]	Package type[1]	Operational range
16	1.8 - 5.5V	ATmega169PA-AU ATmega169PA-AUR[4] ATmega169PA-MU ATmega169PA-MUR[4] ATmega169PA-MCH ATmega169PA-MCHR[4]	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169PA-AN ATmega169PA-ANR[4] ATmega169PA-MN ATmega169PA-MNR[4]	64A 64A 64M1 64M1	Extended (-40°C to 105°C)[5]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 29-1 on page 330.
4. Tape & Reel.
5. See characterization specification at 105°C.

Package type	
	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0mm Exposed Pad, Quad Flat No-Lead Package (QFN)

9.4 Atmel ATmega329PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega329PA-AU ATmega329PA-AUR(4) ATmega329PA-MU ATmega329PA-MUR(4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega329PA-AN ATmega329PA-ANR(4) ATmega329PA-MN ATmega329PA-MNR(4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 330.
4. Tape &Reel.
5. See characterization specification at 105°C.

Package type	
	64-lead, 14 × 14 × 1.0mm, thin profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.8 Atmel ATmega649P

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5 V	ATmega649P-AU ATmega649P-AUR (4) ATmega649P-MU ATmega649P-MUR (4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-1 on page 330.
4. Tape & Reel.

Package type	
	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

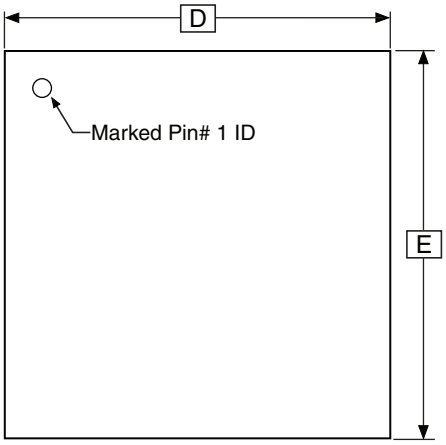
9.10 Atmel ATmega6490P

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega6490P-AU ATmega6490P-AUR (4)	100A 100A	Industrial (-40°C to 85°C)

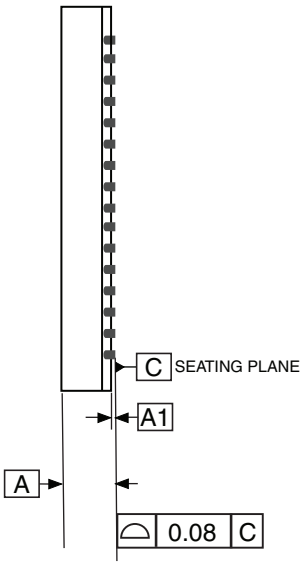
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 330.
4. Tape & Reel.

Package Type	
	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

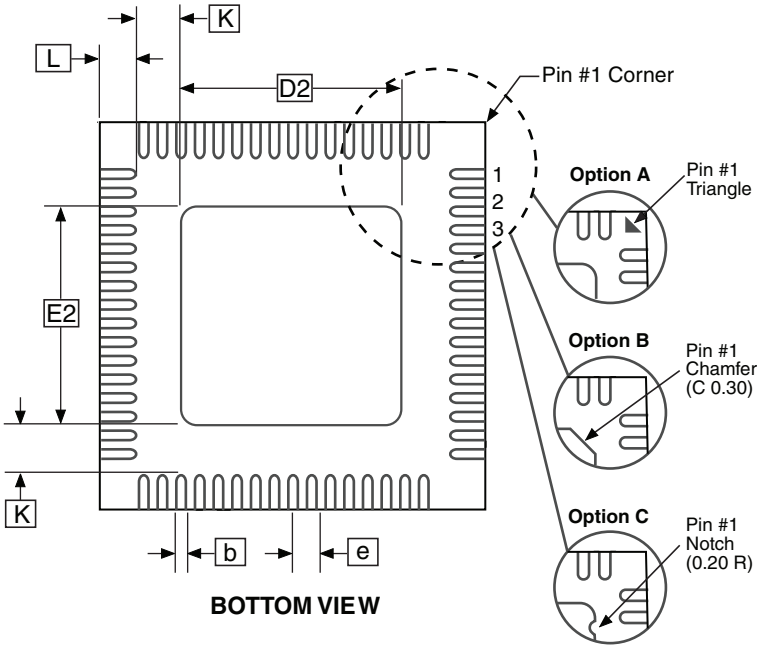
10.2 64M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

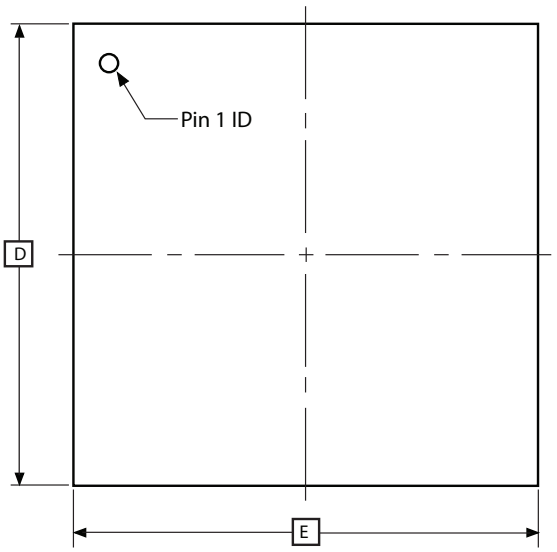
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	

Notes:
1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

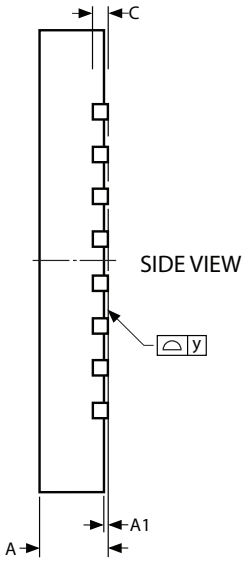
2010-10-19

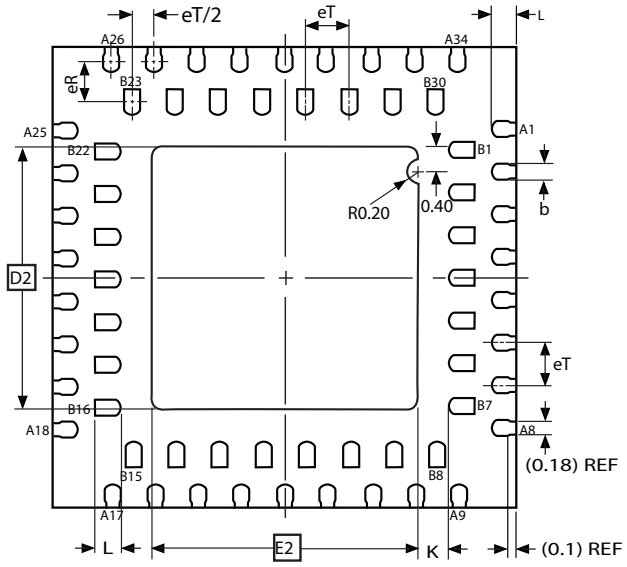
Atmel 2325 Orchard Parkway San Jose, CA 95131	TITLE	DRAWING NO.	REV.
	64M1, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M1	H

10.3 64MC



TOP VIEW





BOTTOM VIEW

Note: 1. The terminal #1 ID is a Laser-marked Feature.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.28	
C		0.20 REF		
D	6.90	7.00	7.10	
D2	3.95	4.00	4.05	
E	6.90	7.00	7.10	
E2	3.95	4.00	4.05	
eT	–	0.65	–	
eR	–	0.65	–	
K	0.20	–	–	(REF)
L	0.35	0.40	0.45	
y	0.00	–	0.075	

10/3/07

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 64MC, 64QFN (2-Row Staggered), 7 x 7 x 1.00 mm Body, 4.0 x 4.0 mm Exposed Pad, Quad Flat No Lead Package	GPC ZXC	DRAWING NO. 64MC	REV. A

11. Errata

11.1 Atmel ATmega169A

No known errata

11.2 Atmel ATmega169A/169PA Rev. A to F

Not sampled.

11.3 Atmel ATmega169PA Rev. G

No known errata.

11.4 Atmel ATmega329A/329PA rev. A

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Using BOD disable will make the chip reset**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. **Using BOD disable will make the chip reset**

   If the part enters sleep with the BOD turned off with the BOD disable option

   enabled, a BOD reset will be generated at wakeup and the chip will reset.

   Problem Fix/Workaround

   Do not use BOD disable

11.5 Atmel ATmega329A/329PA rev. B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

11.6 Atmel ATmega329A/329PA rev. C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

11.7 Atmel ATmega3290A/3290PA rev. A

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Using BOD disable will make the chip reset**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. **Using BOD disable will make the chip reset**

   If the part enters sleep with the BOD turned off with the BOD disable option

   enabled, a BOD reset will be generated at wakeup and the chip will reset.

   Problem Fix/Workaround

   Do not use BOD disable

11.8 Atmel ATmega3290A/3290PA rev. B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

11.9 Atmel ATmega3290A/3290PA rev. C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

11.10 Atmel ATmega649A/649P/ATmega6490A/6490P

No known errata.

12. Datasheet revision history

Please note that the referring page numbers in this section are referring to this document.The referring revision in this section are referring to the document revision.

12.1 Rev. 8284F - 08/2014

1. New back page
2. Changed chip references in the text in Section 9.6 ”Low-frequency XTAL oscillator” on page 34.

12.2 Rev. 8284E - 02/2013

1. New template
2. Countless, small corrections made throughout the whole document
3. In Section ”System and reset characteristics” on page 332 the sentence “The following chara apply only to...” has been deleted
4. Former Section 29.6 on page 332 (“Power-on reset”), subsection 29.6.1 (“ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490PA revision C and later”) and subsection 29.6.2 (“ATmega329A/329PA/3290A/3290PA/649A/649P/6490A/6490PA revision A and B”) have been deleted
5. The maximum limits for “Power Supply Current” in Table 29-9 on page 328 have been corrected
6. The maximum limits for “Power Supply Current” in Table 29-11 on page 329 have been corrected
7. Added ”Electrical Characteristics – TA = -40°C to 105°C” on page 337.
8. Added ”Typical Characteristics – TA = -40°C to 105°C” on page 658.
9. Updated ”Ordering information” on page 20

12.3 Rev. 8284D - 06/11

1. Removed “Preliminary” from the front page
2. Updated the Table 29-16 on page 344. V_{POT} falling / Min. is 0.05V, not 0.5V

12.4 Rev. 8284C - 06/11

1. Updated ”Signature Bytes” on page 294. A, P, and PA devices have different signature (0x002) bytes.
2. Updated all ”DC Characteristics” on page 323.

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