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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4024lqi-s401

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The PSoC 4000S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4000S reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a $\pm 5\%$ reference.

Analog Blocks

Low-power Comparators (LPC)

The PSoC 4000S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The PSoC 4000S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The PSoC 4000S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4000S.

Serial Communication Block (SCB)

The PSoC 4000S has two serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000S and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000S is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Coders), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

GPIO

The PSoC 4000S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4000S).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

LCD Segment Drive

The PSoC 4000S has an LCD controller, which can drive up to 8 commons and up to 28 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Table 1. PSoC 4000S Pin List (continued)

48-TQFP		32-QFN		24-QFN		25-CSP		40-QFN	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
17	P3.4							14	P3.4
18	P3.5							15	P3.5
19	P3.6							16	P3.6
20	P3.7							17	P3.7
21	VDDD								
22	P4.0	13	P4.0	9	P4.0	E3	P4.0	18	P4.0
23	P4.1	14	P4.1	10	P4.1	D2	P4.1	19	P4.1
24	P4.2	15	P4.2	11	P4.2	E2	P4.2	20	P4.2
25	P4.3	16	P4.3	12	P4.3	E1	P4.3	21	P4.3

Descriptions of the Pin functions are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V \pm 5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

Alternate Pin Functions

Each port pin can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

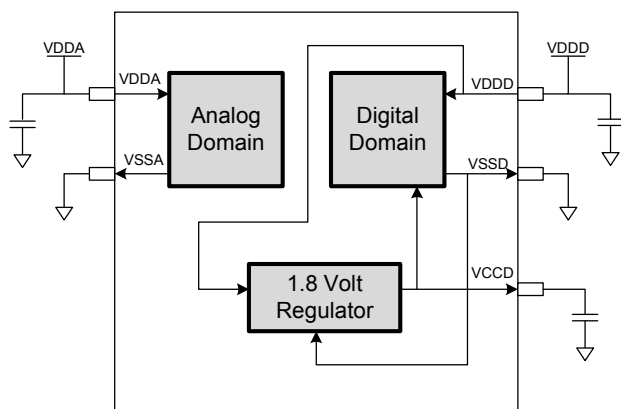
Port/ Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]		scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]		scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						
P0.4	wco.wco_in			scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7				scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0			tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1			tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2			tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]		scb[0].spi_clk:1
P1.3			tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]		scb[0].spi_select0:1
P1.4							scb[0].spi_select1:1
P1.5							scb[0].spi_select2:1

Port/ Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P1.6							scb[0].spi_select3:1
P1.7							
P2.0		prgio[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1		prgio[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2		prgio[0].io[2]					scb[1].spi_clk:2
P2.3		prgio[0].io[3]					scb[1].spi_select0:2
P2.4		prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5		prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6		prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7		prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		prgio[1].io[5]	tcpwm.line_compl[2]:0		tcpwm.tr_in[7]		scb[1].spi_select2:0
P3.6		prgio[1].io[6]	tcpwm.line[3]:0		tcpwm.tr_in[8]		scb[1].spi_select3:0
P3.7		prgio[1].io[7]	tcpwm.line_compl[3]:0		tcpwm.tr_in[9]	lpcomp.comp[1]:1	
P4.0	csd.vref_ext			scb[0].uart_rx:0	tcpwm.tr_in[10]	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0	tcpwm.tr_in[11]	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4000S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 3. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is $1.8 \text{ V} \pm 5\%$ (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4000S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000S supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μF ; X5R ceramic or better) and must not be connected to anything else.

Mode 2: $1.8 \text{ V} \pm 5\%$ External Supply

In this mode, the PSoC 4000S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μF range, in parallel with a smaller capacitor (0.1 μF , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 4. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active

Power supply bypass connections example

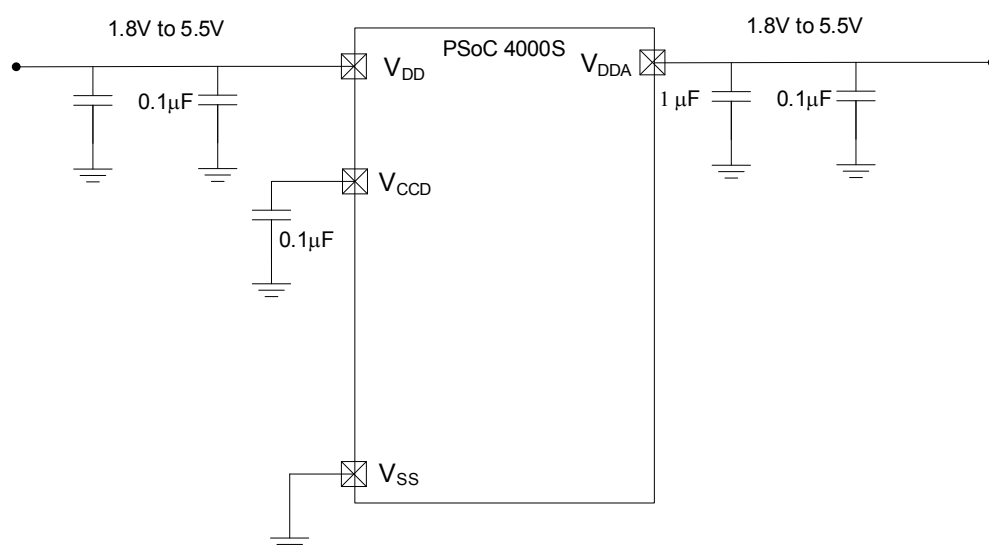


Table 3. DC Specifications (continued)

 Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, $V_{DD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed)							
SID28	I_{DD23}	I ² C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHz
SID28A	I_{DD23A}	I ² C wakeup, WDT, and Comparators on	–	0.9	1.1	mA	12 MHz
Deep Sleep Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ (Regulator on)							
SID31	I_{DD26}	I ² C wakeup and WDT on	–	2.5	60	μA	–
Deep Sleep Mode, $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ (Regulator on)							
SID34	I_{DD29}	I ² C wakeup and WDT on	–	2.5	60	μA	–
Deep Sleep Mode, $V_{DD} = V_{CCD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed)							
SID37	I_{DD32}	I ² C wakeup and WDT on	–	2.5	60	μA	–
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 ^[3]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	μs	
SID50 ^[3]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

Note

2. Guaranteed by characterization.

GPIO

Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DD}$	—	—	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	—	—	$0.3 \times V_{DD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	—	—		—
SID242	V_{IL}	LVTTL input, $V_{DD} < 2.7$ V	—	—	$0.3 \times V_{DD}$		—
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	—	—		—
SID244	V_{IL}	LVTTL input, $V_{DD} \geq 2.7$ V	—	—	0.8		—
SID59	V_{OH}	Output voltage high level	$V_{DD} - 0.6$	—	—		$I_{OH} = 4$ mA at 3 V V_{DD}
SID60	V_{OH}	Output voltage high level	$V_{DD} - 0.5$	—	—		$I_{OH} = 1$ mA at 3 V V_{DD}
SID61	V_{OL}	Output voltage low level	—	—	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DD}
SID62	V_{OL}	Output voltage low level	—	—	0.6		$I_{OL} = 10$ mA at 3 V V_{DD}
SID62A	V_{OL}	Output voltage low level	—	—	0.4		$I_{OL} = 3$ mA at 3 V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	—
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		—
SID65	I_{IL}	Input leakage current (absolute value)	—	—	2	nA	25 °C, $V_{DD} = 3.0$ V
SID66	C_{IN}	Input capacitance	—	—	7	pF	—
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	—	mV	$V_{DD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	—	—		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	—	—		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	—	—	100	μ A	—
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	—	—	200	mA	—

Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	—	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	—	12		3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	—	60	—	3.3 V V_{DD} , Load = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	—	60	—	3.3 V V_{DD} , Load = 25 pF

Notes

3. V_{IH} must not exceed $V_{DD} + 0.2$ V.
4. Guaranteed by characterization.

CSD
Table 11. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	$V_{DD} > 2\text{ V}$ (with ripple), 25°C T_A , Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	$V_{DD} > 1.75\text{V}$ (with ripple), 25°C T_A , Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V _{REF}	Voltage reference for CSD and Comparator	0.6	1.2	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	$V_{DDA} - 0.6$	V	$V_{DDA} - 0.06$ or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	μA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	μA	LSB = 2.4-μA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8-μA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	μA	LSB = 37.5-nA typ.

Table 12. 10-bit CapSense ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	kHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V _{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 13. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[6]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

Note

6. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

Table 18. UART DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	–

Table 19. UART AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 20. LCD Direct Drive DC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current $V_{bias} = 5\text{ V}$	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	I_{LCDOP2}	LCD system operating current $V_{bias} = 3.3\text{ V}$	–	2	–		32 × 4 segments. 50 Hz. 25 °C

Table 21. LCD Direct Drive AC Specifications^[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note

8. Guaranteed by characterization.

Memory

Table 22. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 23. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[9]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE} ^[9]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[9]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[9]	Bulk erase time (32 KB)	–	–	35		–
SID180 ^[10]	T _{DEVPROG} ^[9]	Total device program time	–	–	7	Seconds	–
SID181 ^[10]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[10]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[10]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 24. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[10]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[10]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 25. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[10]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[10]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

9. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

10. Guaranteed by characterization.

Ordering Information

The PSoC 4000S part numbers and features are listed in the following table.

Table 35. PSoC 4000S Ordering Information

Category	MPN	Features												Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CapSense	10-bit CSD ADC	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	WLCSP (0.35-mm pitch)	24-Pin QFN	32-Pin QFN	40-Pin QFN	48-Pin TQFP
4024	CY8C4024FNI-S402	24	16	2	0	0	1	0	2	5	2	8	21	✓				
	CY8C4024LQI-S401	24	16	2	0	0	1	0	2	5	2	8	19		✓			
	CY8C4024LQI-S402	24	16	2	0	0	1	0	2	5	2	16	27			✓		
	CY8C4024LQI-S403	24	16	2	0	0	1	0	2	5	2	16	34				✓	
	CY8C4024AZI-S403	24	16	2	0	0	1	0	2	5	2	16	36					✓
	CY8C4024FNI-S412	24	16	2	0	1	1	0	2	5	2	8	21	✓				
	CY8C4024LQI-S411	24	16	2	0	1	1	0	2	5	2	8	19		✓			
	CY8C4024LQI-S412	24	16	2	0	1	1	0	2	5	2	16	27			✓		
	CY8C4024LQI-S413	24	16	2	0	1	1	0	2	5	2	16	34				✓	
	CY8C4024AZI-S413	24	16	2	0	1	1	0	2	5	2	16	36					✓
4025	CY8C4025FNI-S402	24	32	4	0	0	1	0	2	5	2	8	21	✓				
	CY8C4025LQI-S401	24	32	4	0	0	1	0	2	5	2	8	19		✓			
	CY8C4025LQI-S402	24	32	4	0	0	1	0	2	5	2	16	27			✓		
	CY8C4025AZI-S403	24	32	4	0	0	1	0	2	5	2	16	36					✓
	CY8C4025FNI-S412	24	32	4	0	1	1	0	2	5	2	8	21	✓				
	CY8C4025LQI-S411	24	32	4	0	1	1	0	2	5	2	8	19		✓			
	CY8C4025LQI-S412	24	32	4	0	1	1	0	2	5	2	16	27			✓		
	CY8C4025AZI-S413	24	32	4	0	1	1	0	2	5	2	16	36					✓
4045	CY8C4045FNI-S412	48	32	4	0	1	1	0	2	5	2	8	21	✓				
	CY8C4045LQI-S411	48	32	4	0	1	1	0	2	5	2	8	19		✓			
	CY8C4045LQI-S412	48	32	4	0	1	1	0	2	5	2	16	27			✓		
	CY8C4045AZI-S413	48	32	4	0	1	1	0	2	5	2	16	36					✓

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU Speed	2	24 MHz
		4	48 MHz

Packaging

The PSoC 4000S will be offered in 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, and 25-ball WLCSP packages.

Package dimensions and Cypress drawing numbers are in the following table.

Table 36. Package List

Spec ID#	Package	Description	Package Dwg
BID20	48-pin TQFP	7 × 7 × 1.4 mm height with 0.5-mm pitch	51-85135
BID27	40-pin QFN	6 × 6 × 0.6 mm height with 0.5-mm pitch	001-80659
BID34A	32-pin QFN	5 × 5 × 0.6 mm height with 0.5-mm pitch	001-42168
BID34	24-pin QFN	4 × 4 × 0.6 mm height with 0.5-mm pitch	001-13937
BID34F	25-ball WLCSP	2.02 × 1.93 × 0.48 mm height with 0.35-mm pitch	002-09957

Table 37. Package Thermal Characteristics

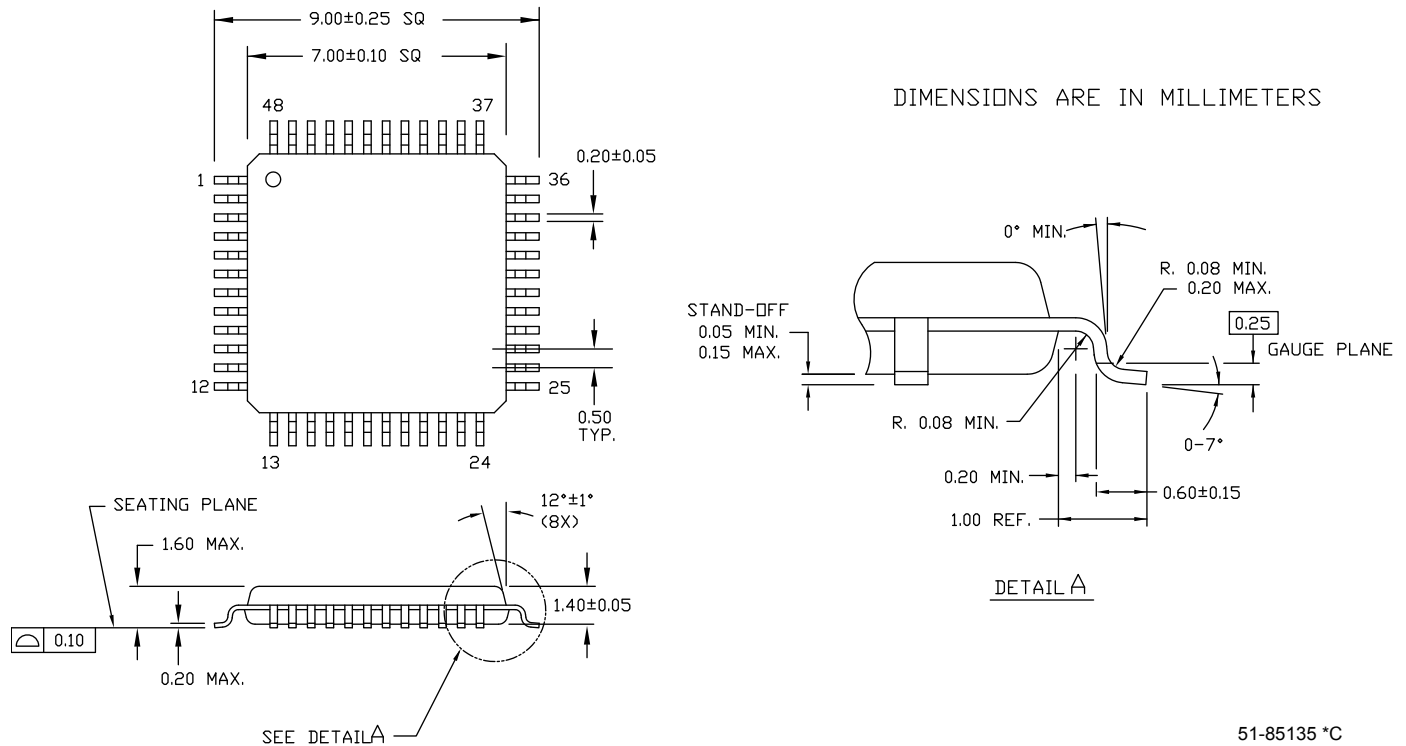
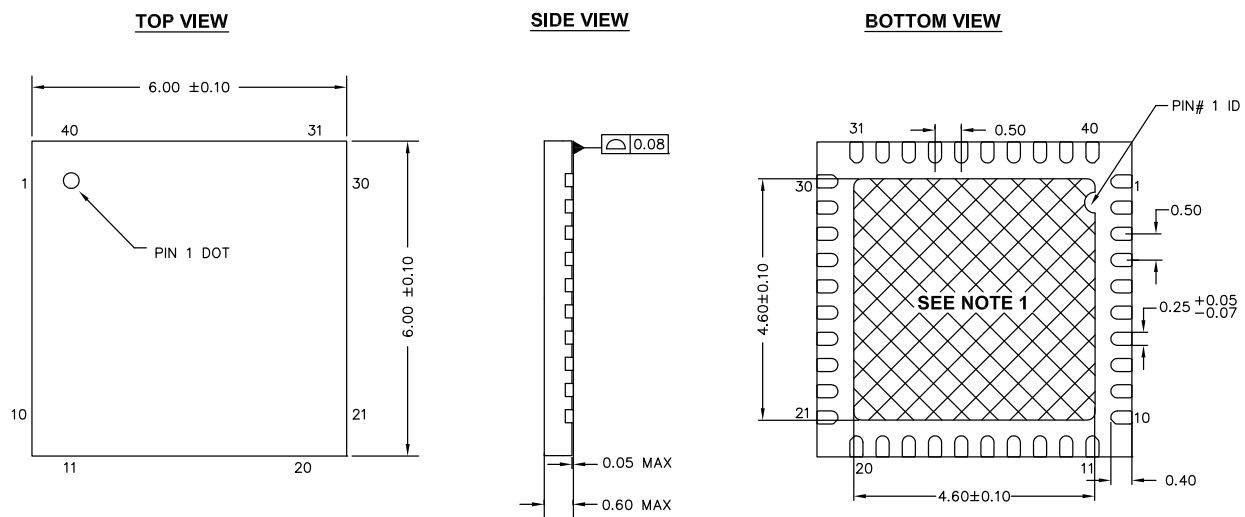
Parameter	Description	Package	Min	Typ	Max	Units
T _A	Operating ambient temperature		−40	25	85	°C
T _J	Operating junction temperature		−40	—	100	°C
T _{JA}	Package θ _{JA}	48-pin TQFP	—	73.5	—	°C/Watt
T _{JC}	Package θ _{JC}	48-pin TQFP	—	33.5	—	°C/Watt
T _{JA}	Package θ _{JA}	40-pin QFN	—	17.8	—	°C/Watt
T _{JC}	Package θ _{JC}	40-pin QFN	—	2.8	—	°C/Watt
T _{JA}	Package θ _{JA}	32-pin QFN	—	20.8	—	°C/Watt
T _{JC}	Package θ _{JC}	32-pin QFN	—	5.9	—	°C/Watt
T _{JA}	Package θ _{JA}	24-pin QFN	—	21.7	—	°C/Watt
T _{JC}	Package θ _{JC}	24-pin QFN	—	5.6	—	°C/Watt
T _{JA}	Package θ _{JA}	25-ball WLCSP	—	54.6	—	°C/Watt
T _{JC}	Package θ _{JC}	25-ball WLCSP	—	0.5	—	°C/Watt


Table 38. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

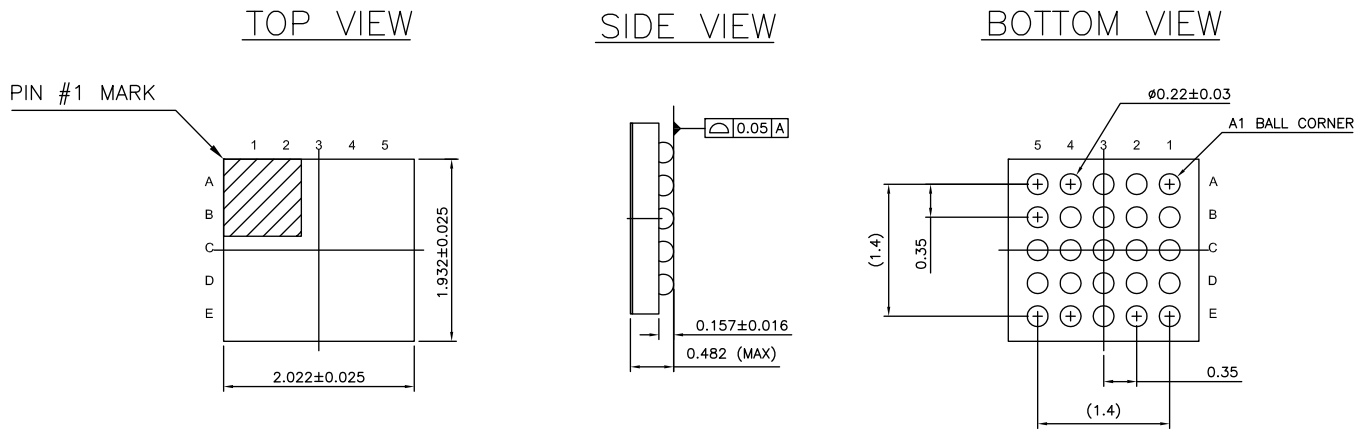
Table 39. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All except WLCSP	MSL 3
25-ball WLCSP	MSL 1

Package Diagrams
Figure 5. 48-pin TQFP Package Outline

Figure 6. 40-pin QFN Package Outline

NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 9. 25-Ball WLCSP


ALL DIMENSIONS ARE IN MM
 JEDEC Publication 95; Design Guide 4.18

002-09957 **

Acronyms

Table 40. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM [®]	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 40. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 40. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 40. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 41. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC [®] 4: PSoC 4000S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00123				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4883809	WKA	08/28/2015	New datasheet
*A	4992376	WKA	10/30/2015	Updated Pinouts . Added $V_{DD} \geq 2.2V$ at $-40^{\circ}C$ under Conditions for specs SID247A, SID90, SID92. Updated Table 12 . Updated Ordering Information .
*B	5037826	SLAN	12/08/2015	Changed datasheet status to Preliminary
*C	5104369	WKA	01/27/2016	Added Errata. Added 25 WLCSP package details. Updated theta J_A and J_C values for all packages.
*D	5139206	WKA	02/16/2016	Updated copyright information at the end of the document.
*E	5173961	WKA	03/15/2016	Updated Pinouts . Updated values for SID79, BID194, SID175, and SID176. Updated CSD and IDAC Specifications . Updated 10-bit CapSense ADC Specifications .
*F	5268662	WKA	05/12/2016	Updated Alternate Pin Functions . Updated the following specs: SID310, SID312, SID313, SID314, SID314C, SID314D, SID314E, SID315, SID315C, SID315D, SID315E, SID322A, SID322B, SIDA109. Removed Errata section. Updated the Cypress logo and copyright information based on the template.
*G	5330930	WKA	07/27/2016	Updated LCD Segment Drive . Updated SID60 conditions. Updated IDD specs. Corrected package dimensions for WLCSP package and added WLCSP MSL condition. Moved datasheet status to Final.
*H	5415365	WKA	09/14/2016	Added 40-pin QFN pin and package details. Updated IDD spec values in DC Specifications .
*I	5561833	WKA	01/09/2017	Changed PRGIO references to Smart I/O.
*J	5704046	GNKK	04/26/2017	Updated the Cypress logo and copyright information.

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