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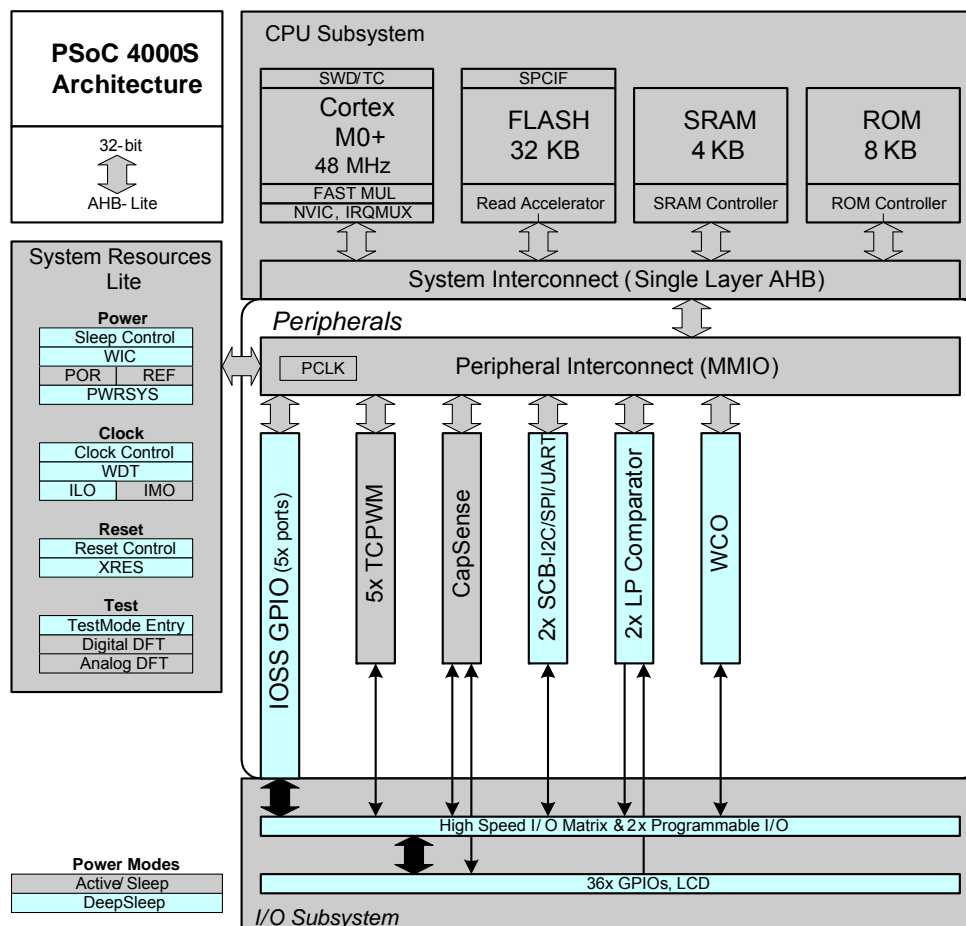
What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4024lqi-s402t |

Figure 1. Block Diagram


PSoC 4000S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000S allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4000S has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4000S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power on page 10](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000S operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

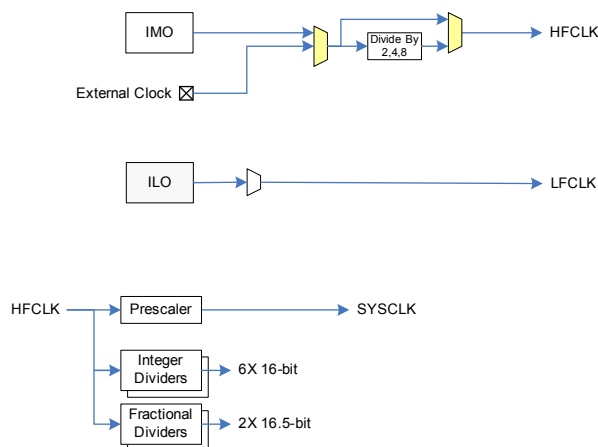
Clock System

The PSoC 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC Creator.

Figure 2. PSoC 4000S MCU Clocking Architecture



IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2%.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

GPIO

The PSoC 4000S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4000S).

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4000S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

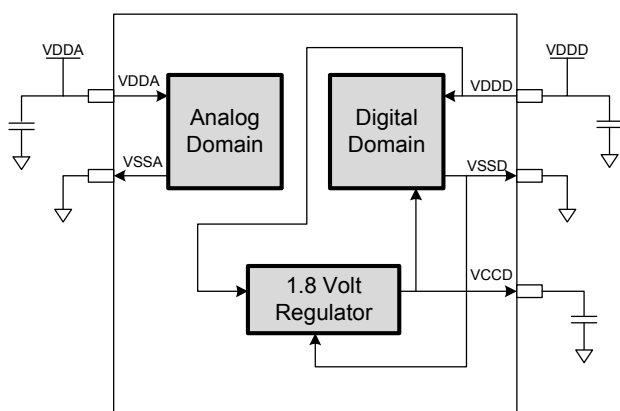
LCD Segment Drive

The PSoC 4000S has an LCD controller, which can drive up to 8 commons and up to 28 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4000S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 3. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is $1.8 \text{ V} \pm 5\%$ (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4000S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000S supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μF ; X5R ceramic or better) and must not be connected to anything else.

Mode 2: 1.8 V $\pm 5\%$ External Supply

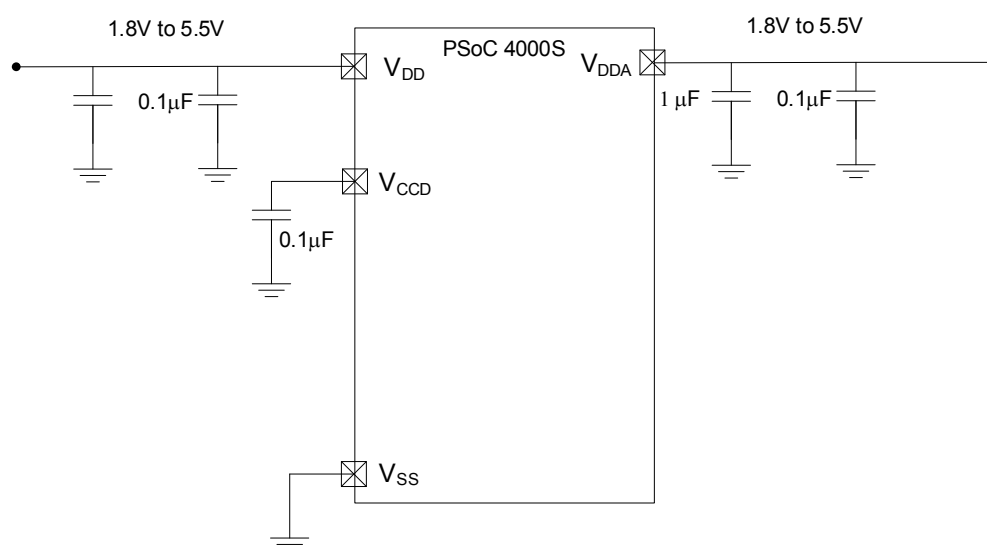
In this mode, the PSoC 4000S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DD} and V_{CCD} pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μF range, in parallel with a smaller capacitor (0.1 μF , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 4. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active

Power supply bypass connections example



Development Support

The PSoC 4000S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4000S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings^[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------|-----------------------------|---|------|-----|----------------------|-------|--------------------------|
| SID1 | V _{DDD_ABS} | Digital supply relative to V _{SS} | -0.5 | – | 6 | V | – |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SS} | -0.5 | – | 1.95 | | – |
| SID3 | V _{GPIO_ABS} | GPIO voltage | -0.5 | – | V _{DD} +0.5 | | – |
| SID4 | I _{GPIO_ABS} | Maximum current per GPIO | -25 | – | 25 | mA | – |
| SID5 | I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DD} , and Min for V _{IL} < V _{SS} | -0.5 | – | 0.5 | | Current injected per pin |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | – |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | | – |
| BID46 | LU | Pin current for latch-up | -140 | – | 140 | mA | – |

Device Level Specifications

All specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 3. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|--|-------------------|---|------|-----|------|-------|-------------------------------|
| SID53 | V _{DD} | Power supply input voltage | 1.8 | – | 5.5 | V | Internally regulated supply |
| SID255 | V _{DD} | Power supply input voltage (V _{CCD} = V _{DD} = V _{DDA}) | 1.71 | – | 1.89 | | Internally unregulated supply |
| SID54 | V _{CCD} | Output voltage (for core logic) | – | 1.8 | – | | – |
| SID55 | C _{EFC} | External regulator voltage bypass | – | 0.1 | – | μF | X5R ceramic or better |
| SID56 | C _{EXC} | Power supply bypass capacitor | – | 1 | – | | X5R ceramic or better |
| Active Mode, V _{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C. | | | | | | | |
| SID10 | I _{DD5} | Execute from flash; CPU at 6 MHz | – | 1.2 | 2.0 | mA | – |
| SID16 | I _{DD8} | Execute from flash; CPU at 24 MHz | – | 2.4 | 4.0 | | – |
| SID19 | I _{DD11} | Execute from flash; CPU at 48 MHz | – | 4.6 | 5.9 | | – |
| Sleep Mode, V _{DDD} = 1.8 V to 5.5 V (Regulator on) | | | | | | | |
| SID22 | I _{DD17} | I ² C wakeup WDT, and Comparators on | – | 1.1 | 1.6 | mA | 6 MHz |
| SID25 | I _{DD20} | I ² C wakeup, WDT, and Comparators on | – | 1.4 | 1.9 | | 12 MHz |

Note

- Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 3. DC Specifications (continued)

 Typical values measured at $V_{DD} = 3.3\text{ V}$ and $25\text{ }^{\circ}\text{C}$.

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|--------------|--|-----|-----|-----|-------|------------------------|
| Sleep Mode, $V_{DD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed) | | | | | | | |
| SID28 | I_{DD23} | I ² C wakeup, WDT, and Comparators on | – | 0.7 | 0.9 | mA | 6 MHz |
| SID28A | I_{DD23A} | I ² C wakeup, WDT, and Comparators on | – | 0.9 | 1.1 | mA | 12 MHz |
| Deep Sleep Mode, $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ (Regulator on) | | | | | | | |
| SID31 | I_{DD26} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
| Deep Sleep Mode, $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ (Regulator on) | | | | | | | |
| SID34 | I_{DD29} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
| Deep Sleep Mode, $V_{DD} = V_{CCD} = 1.71\text{ V to }1.89\text{ V}$ (Regulator bypassed) | | | | | | | |
| SID37 | I_{DD32} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
| XRES Current | | | | | | | |
| SID307 | I_{DD_XR} | Supply current while XRES asserted | – | 2 | 5 | mA | – |

Table 4. AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|----------------------|-----------------|-----------------------------|-----|-----|-----|-------|-----------------------------|
| SID48 | F_{CPU} | CPU frequency | DC | – | 48 | MHz | $1.71 \leq V_{DD} \leq 5.5$ |
| SID49 ^[3] | T_{SLEEP} | Wakeup from Sleep mode | – | 0 | – | μs | |
| SID50 ^[3] | $T_{DEEPSLEEP}$ | Wakeup from Deep Sleep mode | – | 35 | – | | |

Note

2. Guaranteed by characterization.

ρ_C
Table 14. Fixed I²C DC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---|-----|-----|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 50 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | | |

Table 15. Fixed I²C AC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Msps | – |

Table 16. SPI DC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID163 | ISPI1 | Block current consumption at 1 Mbps | – | – | 360 | μA | – |
| SID164 | ISPI2 | Block current consumption at 4 Mbps | – | – | 560 | | – |
| SID165 | ISPI3 | Block current consumption at 8 Mbps | – | – | 600 | | – |

Table 17. SPI AC Specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|-----------|---|-----|-----|-------------|-------|---------------------------------------|
| SID166 | FSPI | SPI operating frequency (Master; 6X Oversampling) | – | – | 8 | MHz | |
| Fixed SPI Master Mode AC Specifications | | | | | | | |
| SID167 | TDMO | MOSI Valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | TDSI | MISO Valid before SClock capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | THMO | Previous MOSI data hold time | 0 | – | – | | Referred to Slave capturing edge |
| Fixed SPI Slave Mode AC Specifications | | | | | | | |
| SID170 | TDMI | MOSI Valid before Sclock Capturing edge | 40 | – | – | ns | – |
| SID171 | TDSO | MISO Valid after Sclock driving edge | – | – | 42 + 3*Tcpu | | T _{CPU} = 1/F _{CPU} |
| SID171A | TDSO_EXT | MISO Valid after Sclock driving edge in Ext. Clk mode | – | – | 48 | | – |
| SID172 | THSO | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | TSSELSSCK | SSEL Valid to first SCK Valid edge | – | – | 100 | ns | – |

Note

7. Guaranteed by characterization.

Memory

Table 22. Flash DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------|---------------------------|------|-----|-----|-------|--------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | – |

Table 23. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|--|---|-------|-----|-----|---------|--------------------------|
| SID174 | T _{ROWWRITE} ^[9] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | T _{ROWERASE} ^[9] | Row erase time | – | – | 16 | | – |
| SID176 | T _{ROWPROGRAM} ^[9] | Row program time after erase | – | – | 4 | | – |
| SID178 | T _{BULKERASE} ^[9] | Bulk erase time (32 KB) | – | – | 35 | | – |
| SID180 ^[10] | T _{DEVPROG} ^[9] | Total device program time | – | – | 7 | Seconds | – |
| SID181 ^[10] | F _{END} | Flash endurance | 100 K | – | – | Cycles | – |
| SID182 ^[10] | F _{RET} | Flash retention. T _A ≤ 55 °C, 100 K P/E cycles | 20 | – | – | Years | – |
| SID182A ^[10] | – | Flash retention. T _A ≤ 85 °C, 10 K P/E cycles | 10 | – | – | | – |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |

System Resources

Power-on Reset (POR)

Table 24. Power On Reset (PRES)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|-----------------------|------------------------|------|-----|-----|-------|--------------------|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185 ^[10] | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186 ^[10] | V _{FALLIPOR} | Falling trip voltage | 0.70 | – | 1.4 | | – |

Table 25. Brown-out Detect (BOD) for V_{CCD}

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|--|------|-----|------|-------|--------------------|
| SID190 ^[10] | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192 ^[10] | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

Notes

9. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

10. Guaranteed by characterization.

SWD Interface

Table 26. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|--------------|---|----------------|-----|---------------|-------|--|
| SID213 | F_SWDCCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWDCCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | | SWDCCLK \leq 1/3 CPU clock frequency |
| SID215 ^[11] | T_SWDI_SETUP | $T = 1/f_{\text{SWDCCLK}}$ | $0.25 \cdot T$ | – | – | ns | – |
| SID216 ^[11] | T_SWDI_HOLD | $T = 1/f_{\text{SWDCCLK}}$ | $0.25 \cdot T$ | – | – | | – |
| SID217 ^[11] | T_SWDO_VALID | $T = 1/f_{\text{SWDCCLK}}$ | – | – | $0.5 \cdot T$ | | – |
| SID217A ^[11] | T_SWDO_HOLD | $T = 1/f_{\text{SWDCCLK}}$ | 1 | – | – | | – |

Internal Main Oscillator

Table 27. IMO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|-----|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | – | – | 250 | μA | – |
| SID219 | I _{IMO2} | IMO operating current at 24 MHz | – | – | 180 | μA | – |

Table 28. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------------|---|-----|-----|-----|-------|--------------------|
| SID223 | F _{IMOTOL1} | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2 | % | |
| SID226 | T _{STARTIMO} | IMO startup time | – | – | 7 | μs | – |
| SID228 | T _{JITRMSIMO2} | RMS jitter at 24 MHz | – | 145 | – | ps | – |

Internal Low-Speed Oscillator

Table 29. ILO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|-------------------|-----------------------|-----|-----|------|-------|--------------------|
| SID231 ^[11] | I _{ILO1} | ILO operating current | – | 0.3 | 1.05 | μA | – |

Table 30. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|---------------------|-----|-----|-----|-------|--------------------|
| SID234 ^[11] | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | – |
| SID236 ^[11] | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | F _{ILOTRIM1} | ILO frequency range | 20 | 40 | 80 | kHz | – |

Note

11. Guaranteed by characterization.

Table 31. Watch Crystal Oscillator (WCO) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|-----------|-------------------------------------|-----|--------|------|-------|----------------------|
| SID398 | FWCO | Crystal Frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | μW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal Load Capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal Shunt Capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating Current (high power mode) | – | – | 8 | uA | |
| SID406 | IWCO2 | Operating Current (low power mode) | – | – | 1 | uA | |

Table 32. External Clock Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------|---|-----|-----|-----|-------|--------------------|
| SID305 ^[12] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306 ^[12] | ExtClkDuty | Duty cycle; measured at V _{DD/2} | 45 | – | 55 | % | – |

Table 33. Block Specs

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------------|------------------------|------------------------------------|-----|-----|-----|---------|--------------------|
| SID262 ^[12] | T _{CLKSWITCH} | System clock source switching time | 3 | – | 4 | Periods | – |

Table 34. Smart I/O Pass-through Time (Delay in Bypass Mode)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|----------|------------|---|-----|-----|-----|-------|----------------------|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

Note

12. Guaranteed by characterization.

Packaging

The PSoC 4000S will be offered in 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, and 25-ball WLCSP packages.

Package dimensions and Cypress drawing numbers are in the following table.

Table 36. Package List

| Spec ID# | Package | Description | Package Dwg |
|----------|---------------|---|-------------|
| BID20 | 48-pin TQFP | 7 × 7 × 1.4 mm height with 0.5-mm pitch | 51-85135 |
| BID27 | 40-pin QFN | 6 × 6 × 0.6 mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32-pin QFN | 5 × 5 × 0.6 mm height with 0.5-mm pitch | 001-42168 |
| BID34 | 24-pin QFN | 4 × 4 × 0.6 mm height with 0.5-mm pitch | 001-13937 |
| BID34F | 25-ball WLCSP | 2.02 × 1.93 × 0.48 mm height with 0.35-mm pitch | 002-09957 |

Table 37. Package Thermal Characteristics

| Parameter | Description | Package | Min | Typ | Max | Units |
|-----------------|--------------------------------|---------------|-----|------|-----|---------|
| T _A | Operating ambient temperature | | −40 | 25 | 85 | °C |
| T _J | Operating junction temperature | | −40 | — | 100 | °C |
| T _{JA} | Package θ _{JA} | 48-pin TQFP | — | 73.5 | — | °C/Watt |
| T _{JC} | Package θ _{JC} | 48-pin TQFP | — | 33.5 | — | °C/Watt |
| T _{JA} | Package θ _{JA} | 40-pin QFN | — | 17.8 | — | °C/Watt |
| T _{JC} | Package θ _{JC} | 40-pin QFN | — | 2.8 | — | °C/Watt |
| T _{JA} | Package θ _{JA} | 32-pin QFN | — | 20.8 | — | °C/Watt |
| T _{JC} | Package θ _{JC} | 32-pin QFN | — | 5.9 | — | °C/Watt |
| T _{JA} | Package θ _{JA} | 24-pin QFN | — | 21.7 | — | °C/Watt |
| T _{JC} | Package θ _{JC} | 24-pin QFN | — | 5.6 | — | °C/Watt |
| T _{JA} | Package θ _{JA} | 25-ball WLCSP | — | 54.6 | — | °C/Watt |
| T _{JC} | Package θ _{JC} | 25-ball WLCSP | — | 0.5 | — | °C/Watt |

Table 38. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------|--------------------------|----------------------------------|
| All | 260 °C | 30 seconds |

Table 39. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

| Package | MSL |
|------------------|-------|
| All except WLCSP | MSL 3 |
| 25-ball WLCSP | MSL 1 |

Package Diagrams

Figure 5. 48-pin TQFP Package Outline

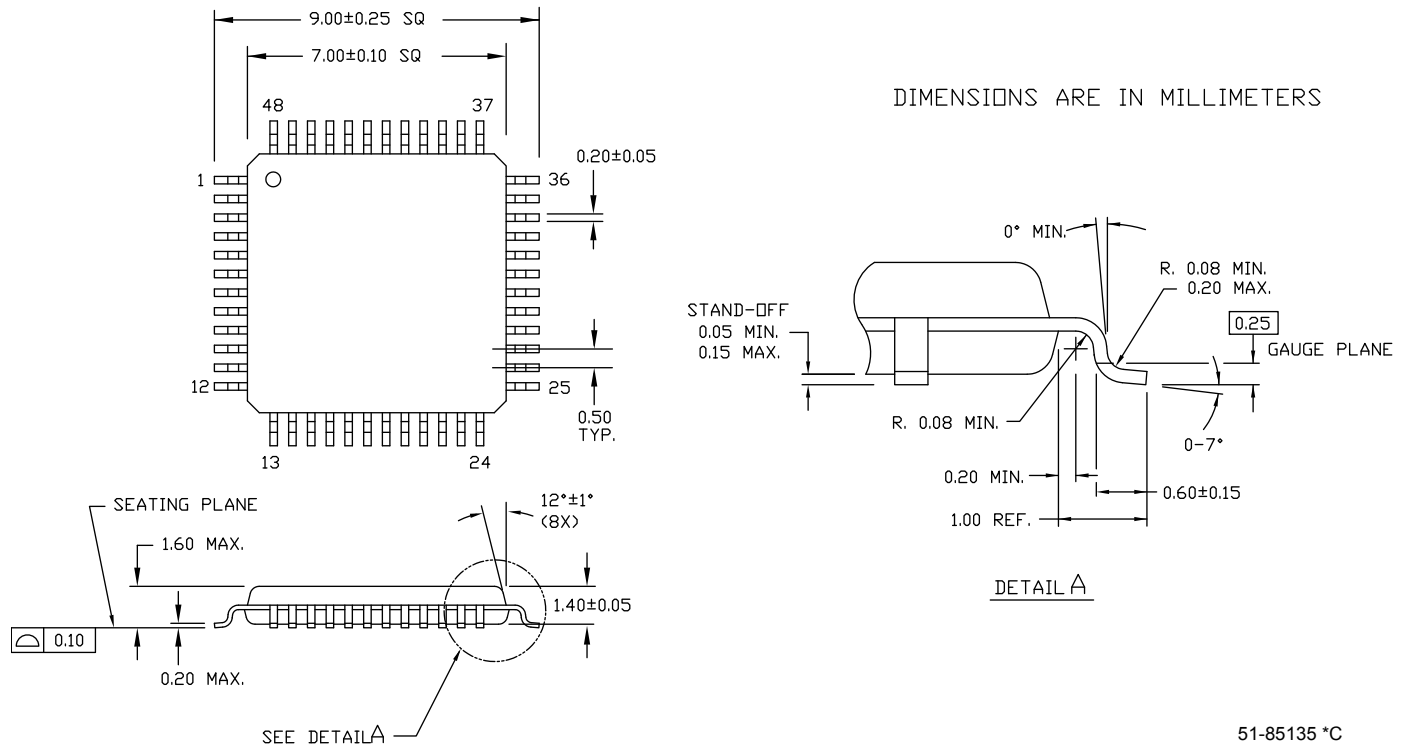
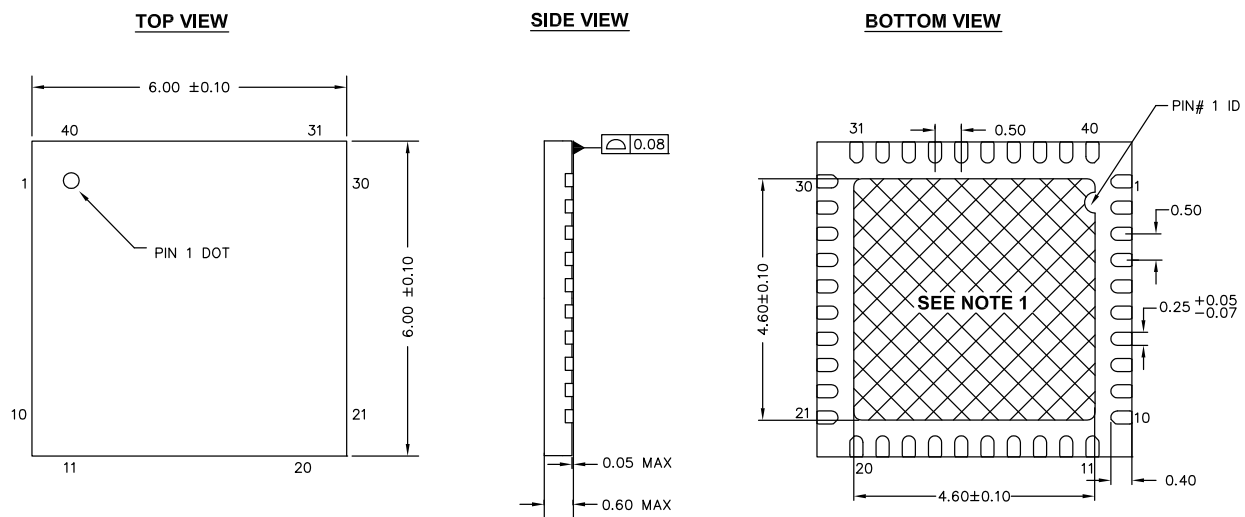



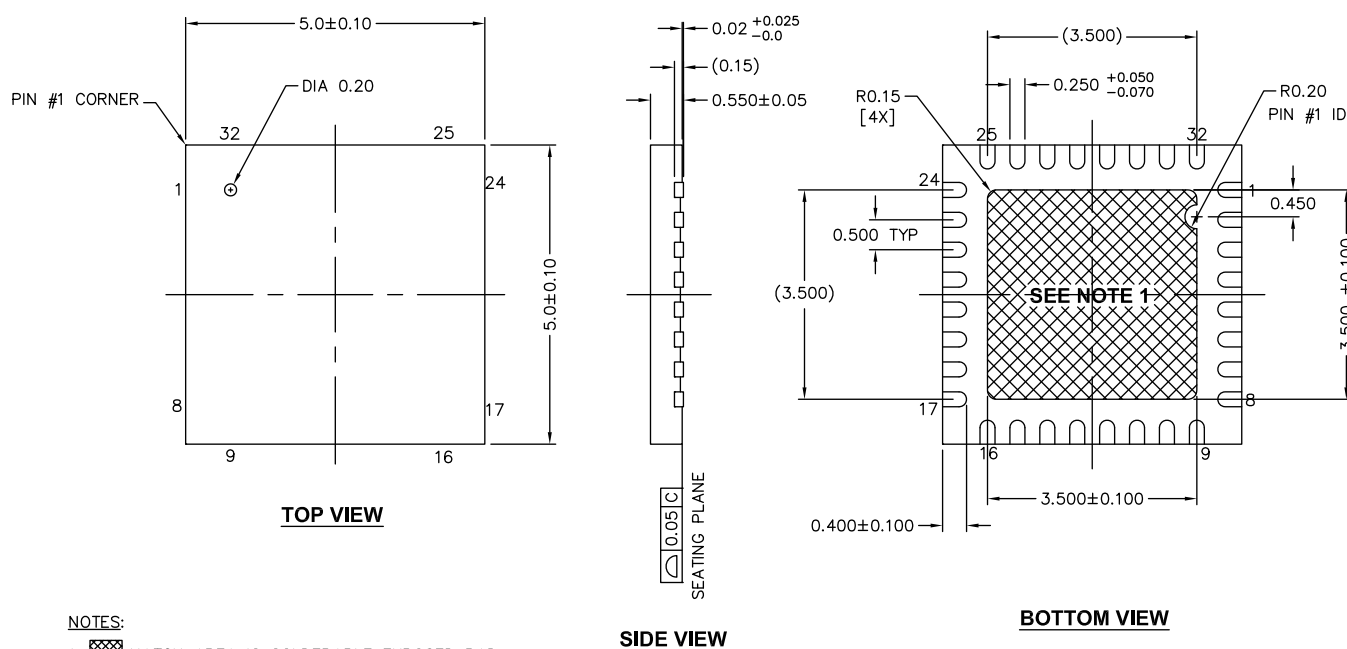
Figure 6. 40-pin QFN Package Outline



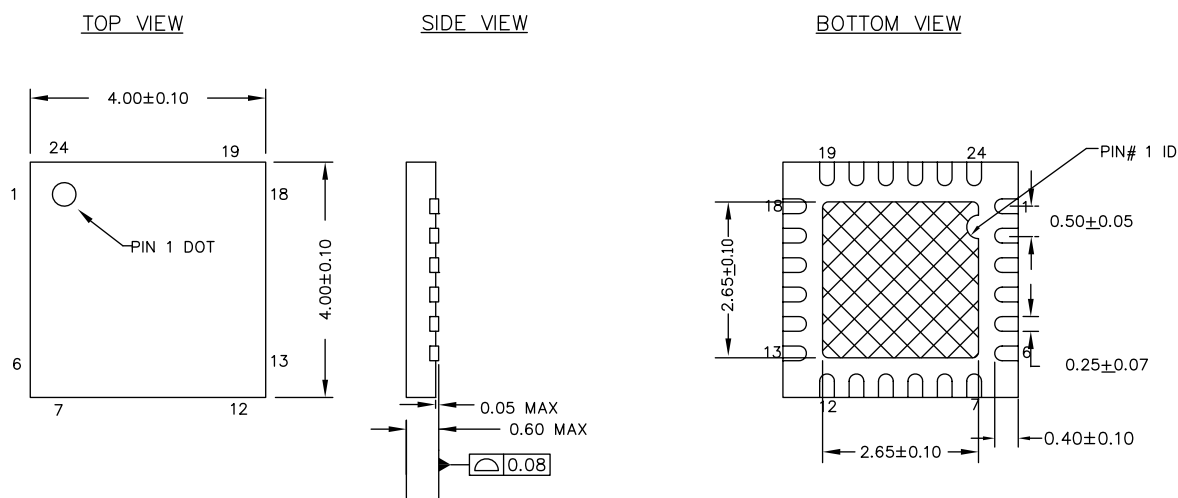
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

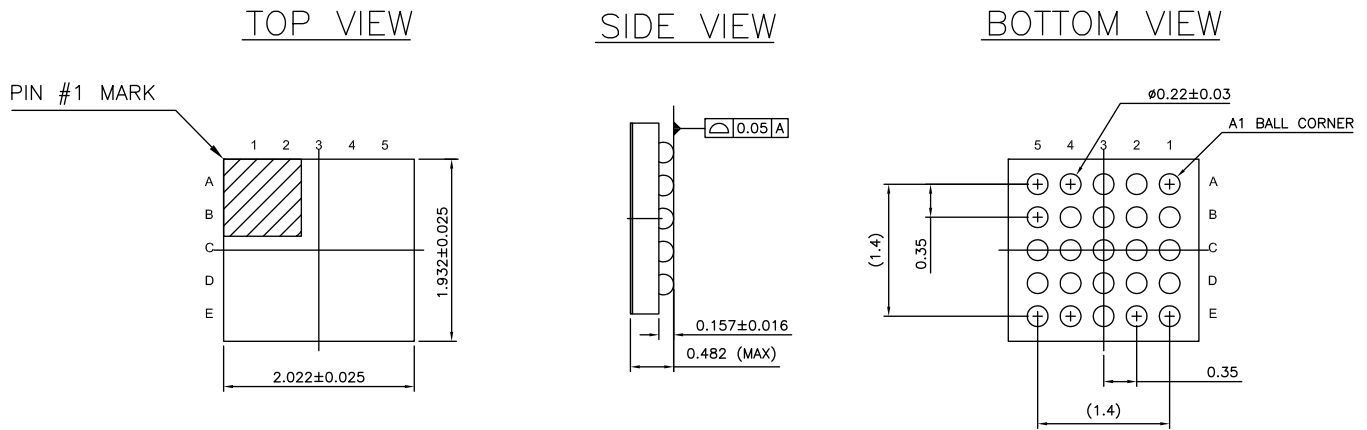
Figure 7. 32-pin QFN Package Outline


001-42168 *E

Figure 8. 24-pin QFN Package Outline


001-13937 *F

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 9. 25-Ball WLCSP


ALL DIMENSIONS ARE IN MM
 JEDEC Publication 95; Design Guide 4.18

002-09957 **

Acronyms

Table 40. Acronyms Used in this Document

| Acronym | Description |
|------------------|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM [®] | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

Table 40. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|--------------------------|--|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

Table 40. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|-------------------|--|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC [®] | Programmable System-on-Chip [™] |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

Table 40. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

Document Conventions

Units of Measure

Table 41. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Revision History

| Description Title: PSoC® 4: PSoC 4000S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00123 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 4883809 | WKA | 08/28/2015 | New datasheet |
| *A | 4992376 | WKA | 10/30/2015 | Updated Pinouts . Added $V_{DD} \geq 2.2V$ at $-40^\circ C$ under Conditions for specs SID247A, SID90, SID92. Updated Table 12 . Updated Ordering Information . |
| *B | 5037826 | SLAN | 12/08/2015 | Changed datasheet status to Preliminary |
| *C | 5104369 | WKA | 01/27/2016 | Added Errata. Added 25 WLCSP package details. Updated theta J_A and J_C values for all packages. |
| *D | 5139206 | WKA | 02/16/2016 | Updated copyright information at the end of the document. |
| *E | 5173961 | WKA | 03/15/2016 | Updated Pinouts . Updated values for SID79, BID194, SID175, and SID176. Updated CSD and IDAC Specifications . Updated 10-bit CapSense ADC Specifications . |
| *F | 5268662 | WKA | 05/12/2016 | Updated Alternate Pin Functions . Updated the following specs: SID310, SID312, SID313, SID314, SID314C, SID314D, SID314E, SID315, SID315C, SID315D, SID315E, SID322A, SID322B, SIDA109. Removed Errata section. Updated the Cypress logo and copyright information based on the template. |
| *G | 5330930 | WKA | 07/27/2016 | Updated LCD Segment Drive . Updated SID60 conditions. Updated IDD specs. Corrected package dimensions for WLCSP package and added WLCSP MSL condition. Moved datasheet status to Final. |
| *H | 5415365 | WKA | 09/14/2016 | Added 40-pin QFN pin and package details. Updated IDD spec values in DC Specifications . |
| *I | 5561833 | WKA | 01/09/2017 | Changed PRGIO references to Smart I/O. |
| *J | 5704046 | GNKK | 04/26/2017 | Updated the Cypress logo and copyright information. |

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