

Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

υ	е	τ	а	I	l	s

-XF

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4025lqi-s401

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



## Contents

Functional Definition	4
CPU and Memory Subsystem	4
System Resources	4
Analog Blocks	5
Programmable Digital Blocks	5
Fixed Function Digital	5
GPIO	6
Special Function Peripherals	6
Pinouts	7
Alternate Pin Functions	8
Power	10
Mode 1: 1.8 V to 5.5 V External Supply	10
Mode 2: 1.8 V ±5% External Supply	10
Development Support	11
Documentation	11
Online	11
Tools	11
Electrical Specifications	12
Absolute Maximum Ratings	12
Device Level Specifications	12

Analog Peripherals	
Digital Peripherals	
Memory	
System Resources	
Ordering Information	
Packaging	
Package Diagrams	
Acronyms	
Document Conventions	
Units of Measure	
Revision History	
Sales, Solutions, and Legal Info	rmation 35
Worldwide Sales and Design	Support
Products	
PSoC® Solutions	
Cypress Developer Communi	ty 35
Technical Support	





Figure 1. Block Diagram

PSoC 4000S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000S allows the customer to make.



## **Functional Definition**

#### **CPU and Memory Subsystem**

#### CPU

The Cortex-M0+ CPU in the PSoC 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4000S has four breakpoint (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4000S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

#### SRAM

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

### SROM

A supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section Power on page 10. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000S operates with a single external supply over the range of either 1.8 V  $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

#### Clock System

The PSoC 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC Creator.

#### Figure 2. PSoC 4000S MCU Clocking Architecture



### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

#### ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watch Crystal Oscillator (WCO)

The PSoC 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.



#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

#### Reset

The PSoC 4000S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

#### Voltage Reference

The PSoC 4000S reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a  $\pm 5\%$  reference.

## Analog Blocks

### Low-power Comparators (LPC)

The PSoC 4000S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

### Current DACs

The PSoC 4000S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

#### Analog Multiplexed Buses

The PSoC 4000S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

### **Programmable Digital Blocks**

The programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

### **Fixed Function Digital**

#### Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4000S.

#### Serial Communication Block (SCB)

The PSoC 4000S has two serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

**I<sup>2</sup>C Mode**: The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000S and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode and Fast-mode devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000S is not completely compliant with the  $I^2C$  spec in the following respect:

GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.



## GPIO

The PSoC 4000S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - □ Analog input mode (input and output buffers disabled)
  - □ Input only
  - □ Weak pull-up with strong pull-down
  - □ Strong pull-up with weak pull-down
  - □ Open drain with strong pull-down
  - Open drain with strong pull-up
  - □ Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4000S).

### **Special Function Peripherals**

#### CapSense

CapSense is supported in the PSoC 4000S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user. Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

#### LCD Segment Drive

The PSoC 4000S has an LCD controller, which can drive up to 8 commons and up to 28 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).



#### Table 1. PSoC 4000S Pin List (continued)

48	B-TQFP	32	2-QFN	24	4-QFN	2	5-CSP		40-QFN
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
17	P3.4							14	P3.4
18	P3.5							15	P3.5
19	P3.6							16	P3.6
20	P3.7							17	P3.7
21	VDDD								
22	P4.0	13	P4.0	9	P4.0	E3	P4.0	18	P4.0
23	P4.1	14	P4.1	10	P4.1	D2	P4.1	19	P4.1
24	P4.2	15	P4.2	11	P4.2	E2	P4.2	20	P4.2
25	P4.3	16	P4.3	12	P4.3	E1	P4.3	21	P4.3

#### Descriptions of the Pin functions are as follows:

**VDDD**: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

**VDD:** Power supply to all sections of the chip

**VSS:** Ground for all sections of the chip

### **Alternate Pin Functions**

Each port pin can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/ Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]		scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]		scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						
P0.4	wco.wco_in			scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7				scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0			tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1			tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2			tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]		scb[0].spi_clk:1
P1.3			tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]		scb[0].spi_select0:1
P1.4							scb[0].spi_select1:1
P1.5							scb[0].spi_select2:1



## **Development Support**

The PSoC 4000S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4000S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

#### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

#### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



## Table 3. DC Specifications (continued)

Typical values measured at V\_DD = 3.3 V and 25  $^\circ\text{C}.$ 

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions		
Sleep Mode, V	Sleep Mode, V <sub>DDD</sub> = 1.71 V to 1.89 V (Regulator bypassed)								
SID28	I <sub>DD23</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on	-	0.7	0.9	mA	6 MHz		
SID28A	I <sub>DD23A</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on	-	0.9	1.1	mA	12 MHz		
Deep Sleep M	ode, V <sub>DD</sub> = 1.8 V	to 3.6 V (Regulator on)							
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	60	μA	-		
Deep Sleep M	ode, V <sub>DD</sub> = 3.6 V	to 5.5 V (Regulator on)							
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	60	μA	-		
Deep Sleep M	ode, V <sub>DD</sub> = V <sub>CCD</sub>	, = 1.71 V to 1.89 V (Regulator bypasse	d)						
SID37	I <sub>DD32</sub>	I <sup>2</sup> C wakeup and WDT on	-	2.5	60	μA	-		
XRES Current	(RES Current								
SID307	I <sub>DD_XR</sub>	Supply current while XRES asserted	_	2	5	mA	_		

## Table 4. AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID48	F <sub>CPU</sub>	CPU frequency	DC	-	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 <sup>[3]</sup>	T <sub>SLEEP</sub>	Wakeup from Sleep mode	-	0	-	110	
SID50 <sup>[3]</sup>	T <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep mode	-	35	-	μο	



GPIO

### Table 5. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID57	V <sub>IH</sub> <sup>[3]</sup>	Input voltage high threshold	$0.7\times V_{DDD}$	-	_		CMOS Input
SID58	V <sub>IL</sub>	Input voltage low threshold	-	-	$0.3 \times V_{DDD}$		CMOS Input
SID241	V <sub>IH</sub> <sup>[3]</sup>	LVTTL input, V <sub>DDD</sub> < 2.7 V	$0.7\times V_{DDD}$	-	-		-
SID242	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> < 2.7 V	_	_	$0.3 \times V_{DDD}$		-
SID243	V <sub>IH</sub> <sup>[3]</sup>	LVTTL input, $V_{DDD} \ge 2.7 V$	2.0	-	_	.,	_
SID244	V <sub>IL</sub>	LVTTL input, $V_{DDD} \ge 2.7 V$	_	-	0.8	V	_
SID59	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.6	-	_		$I_{OH}$ = 4 mA at 3 V $V_{DDD}$
SID60	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.5	-	_		$I_{OH}$ = 1 mA at 3 V $V_{DDD}$
SID61	V <sub>OL</sub>	Output voltage low level	-	-	0.6		I <sub>OL</sub> = 4 mA at 1.8 V V <sub>DDD</sub>
SID62	V <sub>OL</sub>	Output voltage low level	-	-	0.6		$I_{OL}$ = 10 mA at 3 V $V_{DDD}$
SID62A	V <sub>OL</sub>	Output voltage low level	-	-	0.4		$I_{OL}$ = 3 mA at 3 V $V_{DDD}$
SID63	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	۲O	_
SID64	R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	K22	_
SID65	I <sub>IL</sub>	Input leakage current (absolute value)	-	-	2	nA	25 °C, V <sub>DDD</sub> = 3.0 V
SID66	C <sub>IN</sub>	Input capacitance	-	-	7	pF	-
SID67 <sup>[4]</sup>	V <sub>HYSTTL</sub>	Input hysteresis LVTTL	25	40	-		$V_{DDD} \ge 2.7 V$
SID68 <sup>[4]</sup>	V <sub>HYSCMOS</sub>	Input hysteresis CMOS	$0.05 \times V_{DDD}$	-	-	mV	V <sub>DD</sub> < 4.5 V
SID68A <sup>[4]</sup>	V <sub>HYSCMOS5V5</sub>	Input hysteresis CMOS	200	-	-		V <sub>DD</sub> > 4.5 V
SID69 <sup>[4]</sup>	I <sub>DIODE</sub>	Current through protection diode to $V_{DD}/V_{SS}$	-	_	100	μA	-
SID69A <sup>[4]</sup>	I <sub>TOT_GPIO</sub>	Maximum total source or sink chip current	_	_	200	mA	_

## Table 6. GPIO AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID70	T <sub>RISEF</sub>	Rise time in fast strong mode	2	-	12	ns	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID71	T <sub>FALLF</sub>	Fall time in fast strong mode	2	-	12	115	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID72	T <sub>RISES</sub>	Rise time in slow strong mode	10	-	60	-	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	_	60	_	3.3 V V <sub>DDD</sub> , Cload = 25 pF

Notes

3. V<sub>IH</sub> must not exceed V<sub>DDD</sub> + 0.2 V.
 4. Guaranteed by characterization.



#### Table 11. CSD and IDAC Specifications (continued)

SPEC ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	-	82	μA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	-	660	μΑ	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	-	_	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	-	-	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	-	-	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	-	-	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	-	-	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	-	-	10	μs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	-	-	10	μs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	-	2.2	_	nF	5-V rating, X7R or NP0 cap.

## Table 12. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SIDA94	A_RES	Resolution	-	_	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	-	_	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	-	-	_	Yes	
SIDA98	A_GAINERR	Gain error	_	_	±2	%	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 $\mu$ F
SIDA99	A_OFFSET	Input offset voltage	_	-	3	mV	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 $\mu$ F
SIDA100	A_ISAR	Current consumption	-	-	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	$V_{SSA}$	_	V <sub>DDA</sub>	V	
SIDA103	A_INRES	Input resistance	-	2.2	_	KΩ	
SIDA104	A_INCAP	Input capacitance	-	20	-	pF	
SIDA106	A_PSRR	Power supply rejection ratio	_	60	-	dB	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 $\mu$ F
SIDA107	A_TACQ	Sample acquisition time	-	1	-	μs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	_	_	21.3	μs	Does not include acqui- sition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	-	_	85.3	μs	Does not include acqui- sition time. Equivalent to 11.6 ksps including acquisition time.



### Table 12. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	-	61	_	dB	With 10-Hz input sine wave, external 2.4-V reference, V <sub>REF</sub> (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	-	-	22.4	kHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	-	-	2	LSB	V <sub>REF</sub> = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	_	-	1	LSB	

## **Digital Peripherals**

Timer Counter Pulse-Width Modulator (TCPWM)

## Table 13. TCPWM Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>			
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz		All modes (TCPWM)						
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	155	μA	All modes (TCPWM)					
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	-	-	650		All modes (TCPWM)			
SID.TCPWM.3	TCPWM <sub>FREQ</sub>	Operating frequency	_	_	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz			
SID.TCPWM.4	TPWM <sub>ENEXT</sub>	Input trigger pulse width	2/Fc –		-		For all trigger events <sup>[6]</sup>			
SID.TCPWM.5	TPWM <sub>EXT</sub>	Output trigger pulse widths	2/Fc	_	_		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs			
SID.TCPWM.5A	TC <sub>RES</sub>	Resolution of counter	1/Fc	-	Ι	ns	Minimum time between successive counts			
SID.TCPWM.5B	PWM <sub>RES</sub>	PWM resolution	1/Fc	Ι	Ι		Minimum pulse width of PWM Output			
SID.TCPWM.5C	Q <sub>RES</sub>	Quadrature inputs resolution	1/Fc	_	_		Minimum pulse width between Quadrature phase inputs			



# Table 18. UART DC Specifications<sup>[8]</sup>

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbps	-	-	55	μA	-
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbps	-	-	312	μA	-

## Table 19. UART AC Specifications<sup>[8]</sup>

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID162	F <sub>UART</sub>	Bit rate	-	-	1	Mbps	_

# Table 20. LCD Direct Drive DC Specifications<sup>[8]</sup>

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions		
SID154	I <sub>LCDLOW</sub>	Operating current in low power mode	-	5	-	μA	16 $\times$ 4 small segment disp. at 50 Hz		
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	-	500	5000	pF	-		
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	-	20	-	mV	-		
SID157	I <sub>LCDOP1</sub>	LCD system operating current Vbias = 5 V	-	2	-	m۸	32 × 4 segments. 50 Hz. 25 °C		
SID158	I <sub>LCDOP2</sub>	LCD system operating current Vbias = 3.3 V	_	2	_	ШA	$32 \times 4$ segments. 50 Hz. 25 °C		

## Table 21. LCD Direct Drive AC Specifications<sup>[8]</sup>

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID159	F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	-



Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	-	32.768	-	kHz	
SID399	FTOL	Frequency tolerance	-	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	-	50	-	kΩ	
SID401	PD	Drive Level	-	-	1	μW	
SID402	TSTART	Startup time	-	-	500	ms	
SID403	CL	Crystal Load Capacitance	6	-	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	-	1.35	_	pF	
SID405	IWCO1	Operating Current (high power mode)	-	-	8	uA	
SID406	IWCO2	Operating Current (low power mode)	-	-	1	uA	

#### Table 31. Watch Crystal Oscillator (WCO) Specifications

## Table 32. External Clock Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID305 <sup>[12]</sup>	ExtClkFreq	External clock input frequency	0	-	48	MHz	_
SID306 <sup>[12]</sup>	ExtClkDuty	Duty cycle; measured at V <sub>DD/2</sub>	45	-	55	%	_

## Table 33. Block Specs

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID262 <sup>[12]</sup>	T <sub>CLKSWITCH</sub>	System clock source switching time	3	-	4	Periods	_

## Table 34. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	-	-	1.6	ns	



## **Ordering Information**

The PSoC 4000S part numbers and features are listed in the following table.

## Table 35. PSoC 4000S Ordering Information

							Feat	tures							Package			
Category	MPN	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CapSense	10-bit CSD ADC	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	Old9	WLCSP (0.35-mm pitch)	24-Pin QFN	32-Pin QFN	40-Pin QFN	48-Pin TQFP
	CY8C4024FNI-S402	24	16	2	0	0	1	0	2	5	2	8	21	~				
	CY8C4024LQI-S401	24	16	2	0	0	1	0	2	5	2	8	19		~			
	CY8C4024LQI-S402	24	16	2	0	0	1	0	2	5	2	16	27			~		
	CY8C4024LQI-S403	24	16	2	0	0	1	0	2	5	2	16	34				~	
4024	CY8C4024AZI-S403	24	16	2	0	0	1	0	2	5	2	16	36					~
	CY8C4024FNI-S412	24	16	2	0	1	1	0	2	5	2	8	21	~				
	CY8C4024LQI-S411	24	16	2	0	1	1	0	2	5	2	8	19		~			
	CY8C4024LQI-S412	24	16	2	0	1	1	0	2	5	2	16	27			~		
	CY8C4024LQI-S413	24	16	2	0	1	1	0	2	5	2	16	34				~	
	CY8C4024AZI-S413	24	16	2	0	1	1	0	2	5	2	16	36					~
	CY8C4025FNI-S402	24	32	4	0	0	1	0	2	5	2	8	21	~				
	CY8C4025LQI-S401	24	32	4	0	0	1	0	2	5	2	8	19		~			
	CY8C4025LQI-S402	24	32	4	0	0	1	0	2	5	2	16	27			~		
4025	CY8C4025AZI-S403	24	32	4	0	0	1	0	2	5	2	16	36					~
4020	CY8C4025FNI-S412	24	32	4	0	1	1	0	2	5	2	8	21	~				
	CY8C4025LQI-S411	24	32	4	0	1	1	0	2	5	2	8	19		~			
	CY8C4025LQI-S412	24	32	4	0	1	1	0	2	5	2	16	27			~		
	CY8C4025AZI-S413	24	32	4	0	1	1	0	2	5	2	16	36					~
	CY8C4045FNI-S412	48	32	4	0	1	1	0	2	5	2	8	21	~				
4045	CY8C4045LQI-S411	48	32	4	0	1	1	0	2	5	2	8	19		~			
4040	CY8C4045LQI-S412	48	32	4	0	1	1	0	2	5	2	16	27			~		
	CY8C4045AZI-S413	48	32	4	0	1	1	0	2	5	2	16	36					~

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
в	CPU Speed	2	24 MHz
D	B CPU Speed		48 MHz



Field	Description	Values	Meaning
С	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		М	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:



![](_page_16_Picture_0.jpeg)

![](_page_16_Figure_2.jpeg)

Figure 7. 32-pin QFN Package Outline

Figure 8. 24-pin QFN Package Outline

![](_page_16_Figure_5.jpeg)

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

![](_page_17_Picture_0.jpeg)

### Figure 9. 25-Ball WLCSP

![](_page_17_Figure_3.jpeg)

![](_page_17_Figure_4.jpeg)

TOP VIEW

<u>SIDE VIEW</u>

## BOTTOM VIEW

![](_page_17_Figure_7.jpeg)

![](_page_17_Figure_8.jpeg)

ALL DIMENSIONS ARE IN MM JEDEC Publication 95; Design Guide 4.18 002-09957 \*\*

![](_page_18_Picture_0.jpeg)

# Acronyms

## Table 40. Acronyms Used in this Document

Acronym	Description		
abus	analog local bus		
ADC	analog-to-digital converter		
AG	analog global		
АНВ	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus		
ALU	arithmetic logic unit		
AMUXBUS	analog multiplexer bus		
API	application programming interface		
APSR	application program status register		
ARM®	advanced RISC machine, a CPU architecture		
ATM	automatic thump mode		
BW	bandwidth		
CAN	Controller Area Network, a communications protocol		
CMRR	common-mode rejection ratio		
CPU	central processing unit		
CRC	cyclic redundancy check, an error-checking protocol		
DAC	digital-to-analog converter, see also IDAC, VDAC		
DFB	digital filter block		
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.		
DMIPS	Dhrystone million instructions per second		
DMA	direct memory access, see also TD		
DNL	differential nonlinearity, see also INL		
DNU	do not use		
DR	port write data registers		
DSI	digital system interconnect		
DWT	data watchpoint and trace		
ECC	error correcting code		
ECO	external crystal oscillator		
EEPROM	electrically erasable programmable read-only memory		
EMI	electromagnetic interference		
EMIF	external memory interface		
EOC	end of conversion		
EOF	end of frame		
EPSR	execution program status register		
ESD	electrostatic discharge		

## Table 40. Acronyms Used in this Document (continued)

Acronym	Description		
ETM	embedded trace macrocell		
FIR	finite impulse response, see also IIR		
FPB	flash patch and breakpoint		
FS	full-speed		
GPIO	general-purpose input/output, applies to a PSoC pin		
HVI	high-voltage interrupt, see also LVI, LVD		
IC	integrated circuit		
IDAC	current DAC, see also DAC, VDAC		
IDE	integrated development environment		
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol		
IIR	infinite impulse response, see also FIR		
ILO	internal low-speed oscillator, see also IMO		
IMO	internal main oscillator, see also ILO		
INL	integral nonlinearity, see also DNL		
I/O	input/output, see also GPIO, DIO, SIO, USBIO		
IPOR	initial power-on reset		
IPSR	interrupt program status register		
IRQ	interrupt request		
ITM	instrumentation trace macrocell		
LCD	liquid crystal display		
LIN	Local Interconnect Network, a communications protocol.		
LR	link register		
LUT	lookup table		
LVD	low-voltage detect, see also LVI		
LVI	low-voltage interrupt, see also HVI		
LVTTL	low-voltage transistor-transistor logic		
MAC	multiply-accumulate		
MCU	microcontroller unit		
MISO	master-in slave-out		
NC	no connect		
NMI	nonmaskable interrupt		
NRZ	non-return-to-zero		
NVIC	nested vectored interrupt controller		
NVL	nonvolatile latch, see also WOL		
opamp	operational amplifier		
PAL	programmable array logic, see also PLD		

![](_page_19_Picture_0.jpeg)

# **Revision History**

Description Title: PSoC <sup>®</sup> 4: PSoC 4000S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00123						
Revision	ECN	Orig. of Change	Submission Date	Description of Change		
**	4883809	WKA	08/28/2015	New datasheet		
*A	4992376	WKA	10/30/2015	Updated Pinouts. Added V <sub>DDD</sub> ≥ 2.2V at –40 °C under Conditions for specs SID247A, SID90, SID92. Updated Table 12. Updated Ordering Information.		
*B	5037826	SLAN	12/08/2015	Changed datasheet status to Preliminary		
*C	5104369	WKA	01/27/2016	Added Errata. Added 25 WLCSP package details. Updated theta $J_A$ and $J_C$ values for all packages.		
*D	5139206	WKA	02/16/2016	Updated copyright information at the end of the document.		
*E	5173961	WKA	03/15/2016	Updated Pinouts. Updated values for SID79, BID194. SID175, and SID176. Updated CSD and IDAC Specifications. Updated 10-bit CapSense ADC Specifications.		
*F	5268662	WKA	05/12/2016	Updated Alternate Pin Functions. Updated the following specs: SID310, SID312, SID313, SID314, SID314C, SID314D, SID314E, SID315, SID315C, SID315D, SID315E, SID322A, SID322B, SIDA109. Removed Errata section. Updated the Cypress logo and copyright information based on the template.		
*G	5330930	WKA	07/27/2016	Updated LCD Segment Drive. Updated SID60 conditions. Updated IDD specs. Corrected package dimensions for WLCSP package and added WLCSP MSL condition. Moved datasheet status to Final.		
*H	5415365	WKA	09/14/2016	Added 40-pin QFN pin and package details. Updated IDD spec values in DC Specifications.		
*	5561833	WKA	01/09/2017	Changed PRGIO references to Smart I/O.		
*J	5704046	GNKK	04/26/2017	Updated the Cypress logo and copyright information.		

![](_page_20_Picture_0.jpeg)

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

#### Products

ARM <sup>®</sup> Cortex <sup>®</sup> Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

## **PSoC<sup>®</sup>Solutions**

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

#### **Cypress Developer Community**

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

#### **Technical Support**

cypress.com/support

© Cypress Semiconductor Corporation, 2015-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or properly damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.