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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-QFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4025lqi-s411t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4025lqi-s411t</a>

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## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0+ CPU in the PSoC 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4000S has four breakpoint (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4000S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

#### SRAM

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

#### SROM

A supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section [Power on page 10](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000S operates with a single external supply over the range of either 1.8 V  $\pm$ 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35  $\mu$ s. The opamps can remain operational in Deep Sleep mode.

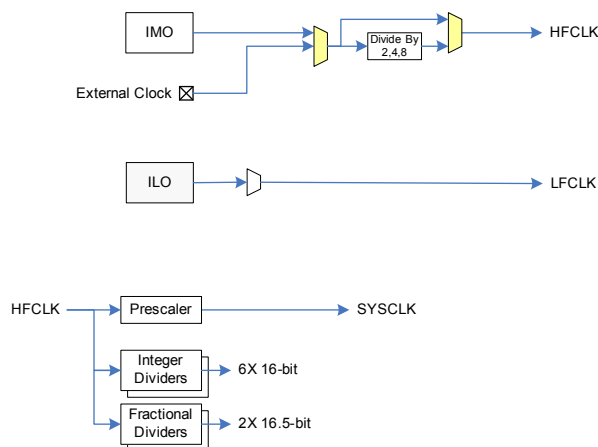
#### Clock System

The PSoC 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC Creator.

**Figure 2. PSoC 4000S MCU Clocking Architecture**



#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4000S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is  $\pm$ 2%.

#### ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watch Crystal Oscillator (WCO)

The PSoC 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

### Reset

The PSoC 4000S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

### Voltage Reference

The PSoC 4000S reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a  $\pm 5\%$  reference.

## Analog Blocks

### Low-power Comparators (LPC)

The PSoC 4000S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

### Current DACs

The PSoC 4000S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

### Analog Multiplexed Buses

The PSoC 4000S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

## Programmable Digital Blocks

The programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

## Fixed Function Digital

### Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4000S.

### Serial Communication Block (SCB)

The PSoC 4000S has two serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

**I<sup>2</sup>C Mode:** The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000S and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode and Fast-mode devices as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000S is not completely compliant with the I<sup>2</sup>C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.

**UART Mode:** This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode:** The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Coders), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

## GPIO

The PSoC 4000S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4000S).

## Special Function Peripherals

### CapSense

CapSense is supported in the PSoC 4000S through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

### LCD Segment Drive

The PSoC 4000S has an LCD controller, which can drive up to 8 commons and up to 28 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

**Table 1. PSoC 4000S Pin List** *(continued)*

48-TQFP		32-QFN		24-QFN		25-CSP		40-QFN	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
17	P3.4							14	P3.4
18	P3.5							15	P3.5
19	P3.6							16	P3.6
20	P3.7							17	P3.7
21	VDDD								
22	P4.0	13	P4.0	9	P4.0	E3	P4.0	18	P4.0
23	P4.1	14	P4.1	10	P4.1	D2	P4.1	19	P4.1
24	P4.2	15	P4.2	11	P4.2	E2	P4.2	20	P4.2
25	P4.3	16	P4.3	12	P4.3	E1	P4.3	21	P4.3

**Descriptions of the Pin functions are as follows:**

**VDDD:** Power supply for the digital section.

**VDDA:** Power supply for the analog section.

**VSSD, VSSA:** Ground pins for the digital and analog sections respectively.

**VCCD:** Regulated digital supply (1.8 V  $\pm$ 5%)

**VDD:** Power supply to all sections of the chip

**VSS:** Ground for all sections of the chip

### Alternate Pin Functions

Each port pin can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

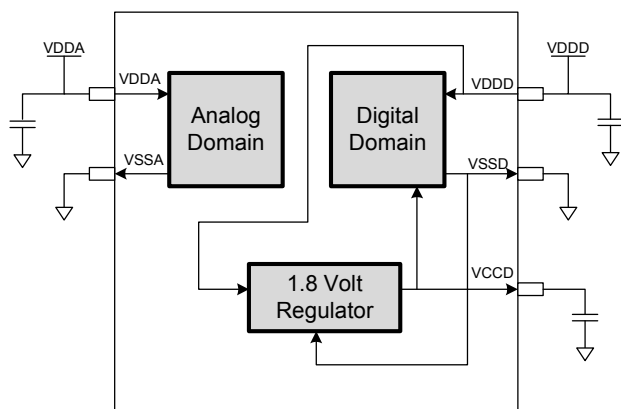
Port/ Pin	Analog	Smart I/O	Alternate Function 1	Alternate Function 2	Alternate Function 3	Deep Sleep 1	Deep Sleep 2
P0.0	lpcomp.in_p[0]				tcpwm.tr_in[0]		scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]				tcpwm.tr_in[1]		scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						
P0.4	wco.wco_in			scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6			srss.ext_clk	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7				scb[1].uart_rts:0			scb[1].spi_select0:1
P1.0			tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1			tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2			tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]		scb[0].spi_clk:1
P1.3			tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]		scb[0].spi_select0:1
P1.4							scb[0].spi_select1:1
P1.5							scb[0].spi_select2:1



## Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4000S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the  $V_{DD}$  input.

**Figure 3. Power Supply Connections**



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is  $1.8 \text{ V} \pm 5\%$  (externally regulated; 1.71 to 1.89, internal regulator bypassed).

### Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4000S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000S supplies the internal logic and its output is connected to the  $V_{CCD}$  pin. The  $V_{CCD}$  pin must be bypassed to ground via an external capacitor (0.1  $\mu\text{F}$ ; X5R ceramic or better) and must not be connected to anything else.

### Mode 2: $1.8 \text{ V} \pm 5\%$ External Supply

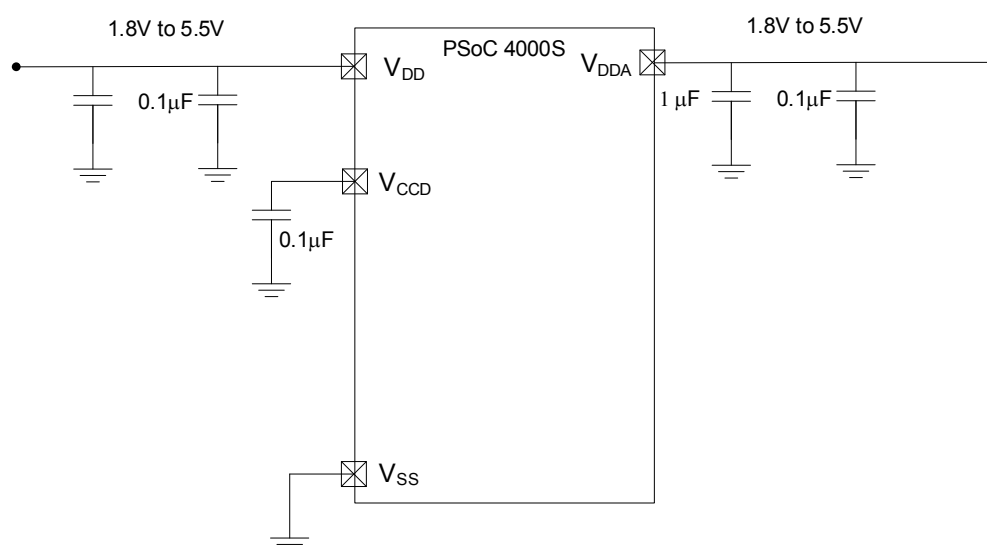
In this mode, the PSoC 4000S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the  $V_{DD}$  and  $V_{CCD}$  pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from  $V_{DDD}$  to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu\text{F}$  range, in parallel with a smaller capacitor (0.1  $\mu\text{F}$ , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

**Figure 4. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active**

Power supply bypass connections example



## Development Support

The PSoC 4000S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit [www.cypress.com/go/psoc4](http://www.cypress.com/go/psoc4) to find out more.

### Documentation

A suite of documentation supports the PSoC 4000S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide:** A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets:** The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual:** The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at [www.cypress.com/psoc4](http://www.cypress.com/psoc4).

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000S family is part of a development tool ecosystem. Visit us at [www.cypress.com/go/psoccreator](http://www.cypress.com/go/psoccreator) for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



**Table 3. DC Specifications** (continued)

 Typical values measured at  $V_{DD} = 3.3\text{ V}$  and  $25\text{ }^{\circ}\text{C}$ .

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
<b>Sleep Mode, <math>V_{DD} = 1.71\text{ V to }1.89\text{ V}</math> (Regulator bypassed)</b>							
SID28	$I_{DD23}$	I <sup>2</sup> C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHz
SID28A	$I_{DD23A}$	I <sup>2</sup> C wakeup, WDT, and Comparators on	–	0.9	1.1	mA	12 MHz
<b>Deep Sleep Mode, <math>V_{DD} = 1.8\text{ V to }3.6\text{ V}</math> (Regulator on)</b>							
SID31	$I_{DD26}$	I <sup>2</sup> C wakeup and WDT on	–	2.5	60	μA	–
<b>Deep Sleep Mode, <math>V_{DD} = 3.6\text{ V to }5.5\text{ V}</math> (Regulator on)</b>							
SID34	$I_{DD29}$	I <sup>2</sup> C wakeup and WDT on	–	2.5	60	μA	–
<b>Deep Sleep Mode, <math>V_{DD} = V_{CCD} = 1.71\text{ V to }1.89\text{ V}</math> (Regulator bypassed)</b>							
SID37	$I_{DD32}$	I <sup>2</sup> C wakeup and WDT on	–	2.5	60	μA	–
<b>XRES Current</b>							
SID307	$I_{DD\_XR}$	Supply current while XRES asserted	–	2	5	mA	–

**Table 4. AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	$F_{CPU}$	CPU frequency	DC	–	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49 <sup>[3]</sup>	$T_{SLEEP}$	Wakeup from Sleep mode	–	0	–	μs	
SID50 <sup>[3]</sup>	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

**Note**

2. Guaranteed by characterization.

**GPIO**
**Table 5. GPIO DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	$V_{IL}$	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	–	–		–
SID242	$V_{IL}$	LVTTL input, $V_{DD} < 2.7$ V	–	–	$0.3 \times V_{DD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	–	–		–
SID244	$V_{IL}$	LVTTL input, $V_{DD} \geq 2.7$ V	–	–	0.8		–
SID59	$V_{OH}$	Output voltage high level	$V_{DD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V $V_{DD}$
SID60	$V_{OH}$	Output voltage high level	$V_{DD} - 0.5$	–	–		$I_{OH} = 1$ mA at 3 V $V_{DD}$
SID61	$V_{OL}$	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V $V_{DD}$
SID62	$V_{OL}$	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V $V_{DD}$
SID62A	$V_{OL}$	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V $V_{DD}$
SID63	$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	$I_{IL}$	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.0$ V
SID66	$C_{IN}$	Input capacitance	–	–	7	pF	–
SID67 <sup>[4]</sup>	$V_{HYSTTL}$	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} \geq 2.7$ V
SID68 <sup>[4]</sup>	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–		$V_{DD} < 4.5$ V
SID68A <sup>[4]</sup>	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 <sup>[4]</sup>	$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	–	–	100	$\mu$ A	–
SID69A <sup>[4]</sup>	$I_{TOT\_GPIO}$	Maximum total source or sink chip current	–	–	200	mA	–

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	$T_{RISEF}$	Rise time in fast strong mode	2	–	12	ns	3.3 V $V_{DD}$ , Load = 25 pF
SID71	$T_{FALLF}$	Fall time in fast strong mode	2	–	12		3.3 V $V_{DD}$ , Load = 25 pF
SID72	$T_{RISES}$	Rise time in slow strong mode	10	–	60	–	3.3 V $V_{DD}$ , Load = 25 pF
SID73	$T_{FALLS}$	Fall time in slow strong mode	10	–	60	–	3.3 V $V_{DD}$ , Load = 25 pF

**Notes**

3.  $V_{IH}$  must not exceed  $V_{DD} + 0.2$  V.
4. Guaranteed by characterization.

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID74	F <sub>GPIOUT1</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F <sub>GPIOUT2</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DDD</sub> ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	F <sub>GPIOUT3</sub>	GPIO F <sub>OUT</sub> ; 3.3 V ≤ V <sub>DDD</sub> ≤ 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	F <sub>GPIOUT4</sub>	GPIO F <sub>OUT</sub> ; 1.71 V ≤ V <sub>DDD</sub> ≤ 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V ≤ V <sub>DDD</sub> ≤ 5.5 V	–	–	48		90/10% V <sub>IO</sub>

**XRES**
**Table 7. XRES DC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	–	–	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	–	–	0.3 × V <sub>DDD</sub>		
SID79	R <sub>PULLUP</sub>	Pull-up resistor	–	60	–	kΩ	–
SID80	C <sub>IN</sub>	Input capacitance	–	–	7	pF	–
SID81 <sup>[5]</sup>	V <sub>HYSXRES</sub>	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V <sub>DD</sub> > 4.5 V
SID82	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub>	–	–	100	μA	

**Table 8. XRES AC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83 <sup>[5]</sup>	T <sub>RESETWIDTH</sub>	Reset pulse width	1	–	–	μs	–
BID194 <sup>[5]</sup>	T <sub>RESETWAKE</sub>	Wake-up time from reset release	–	–	2.7	ms	–

**Note**

5. Guaranteed by characterization.

**Table 11. CSD and IDAC Specifications (continued)**

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	μA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	μA	LSB = 2.4-μA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-μA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

**Table 12. 10-bit CapSense ADC Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus.
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±2	%	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 μF
SIDA99	A_OFFSET	Input offset voltage	–	–	3	mV	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 μF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	$V_{SSA}$	–	$V_{DDA}$	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSR	Power supply rejection ratio	–	60	–	dB	In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 μF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	μs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = $F_{clk}/(2^{(N+2)})$ . Clock frequency = 48 MHz.	–	–	21.3	μs	Does not include acquisition time. Equivalent to 44.8 ksp/s including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = $F_{clk}/(2^{(N+2)})$ . Clock frequency = 48 MHz.	–	–	85.3	μs	Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time.

**Table 18. UART DC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	$I_{UART1}$	Block current consumption at 100 Kbps	–	–	55	μA	–
SID161	$I_{UART2}$	Block current consumption at 1000 Kbps	–	–	312	μA	–

**Table 19. UART AC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	$F_{UART}$	Bit rate	–	–	1	Mbps	–

**Table 20. LCD Direct Drive DC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	$I_{LCDLOW}$	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	$C_{LCDCAP}$	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	$LCD_{OFFSET}$	Long-term segment offset	–	20	–	mV	–
SID157	$I_{LCDOP1}$	LCD system operating current $V_{bias} = 5\text{ V}$	–	2	–	mA	32 × 4 segments. 50 Hz. 25 °C
SID158	$I_{LCDOP2}$	LCD system operating current $V_{bias} = 3.3\text{ V}$	–	2	–		32 × 4 segments. 50 Hz. 25 °C

**Table 21. LCD Direct Drive AC Specifications<sup>[8]</sup>**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	$F_{LCD}$	LCD frame rate	10	50	150	Hz	–

**Note**

8. Guaranteed by characterization.

### SWD Interface

**Table 26. SWD Interface Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCCLK $\leq$ 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCCLK $\leq$ 1/3 CPU clock frequency
SID215 <sup>[11]</sup>	T_SWDI_SETUP	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–	ns	–
SID216 <sup>[11]</sup>	T_SWDI_HOLD	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–		–
SID217 <sup>[11]</sup>	T_SWDO_VALID	$T = 1/f_{\text{SWDCCLK}}$	–	–	$0.5 \cdot T$		–
SID217A <sup>[11]</sup>	T_SWDO_HOLD	$T = 1/f_{\text{SWDCCLK}}$	1	–	–		–

### Internal Main Oscillator

**Table 27. IMO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_IMO1	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I_IMO2	IMO operating current at 24 MHz	–	–	180	μA	–

**Table 28. IMO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F_IMOTOL1	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	$\pm 2$	%	
SID226	T_STARTIMO	IMO startup time	–	–	7	μs	–
SID228	T_JITRMSIMO2	RMS jitter at 24 MHz	–	145	–	ps	–

### Internal Low-Speed Oscillator

**Table 29. ILO DC Specifications**

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231 <sup>[11]</sup>	I_ILO1	ILO operating current	–	0.3	1.05	μA	–

**Table 30. ILO AC Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 <sup>[11]</sup>	T_STARTILO1	ILO startup time	–	–	2	ms	–
SID236 <sup>[11]</sup>	T_ILODUTY	ILO duty cycle	40	50	60	%	–
SID237	F_ILOTRIM1	ILO frequency range	20	40	80	kHz	–

**Note**

11. Guaranteed by characterization.

**Table 31. Watch Crystal Oscillator (WCO) Specifications**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal Frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	
SID406	IWCO2	Operating Current (low power mode)	–	–	1	uA	

**Table 32. External Clock Specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 <sup>[12]</sup>	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 <sup>[12]</sup>	ExtClkDuty	Duty cycle; measured at V <sub>DD/2</sub>	45	–	55	%	–

**Table 33. Block Specs**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 <sup>[12]</sup>	T <sub>CLKSWITCH</sub>	System clock source switching time	3	–	4	Periods	–

**Table 34. Smart I/O Pass-through Time (Delay in Bypass Mode)**

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

**Note**

12. Guaranteed by characterization.



## Ordering Information

The PSoC 4000S part numbers and features are listed in the following table.

**Table 35. PSoC 4000S Ordering Information**

Category	MPN	Features												Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CapSense	10-bit CSD ADC	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	Smart I/Os	GPIO	WLCSP (0.35-mm pitch)	24-Pin QFN	32-Pin QFN	40-Pin QFN	48-Pin TQFP
4024	CY8C4024FNI-S402	24	16	2	0	0	1	0	2	5	2	8	21	✓				
	CY8C4024LQI-S401	24	16	2	0	0	1	0	2	5	2	8	19		✓			
	CY8C4024LQI-S402	24	16	2	0	0	1	0	2	5	2	16	27			✓		
	CY8C4024LQI-S403	24	16	2	0	0	1	0	2	5	2	16	34				✓	
	CY8C4024AZI-S403	24	16	2	0	0	1	0	2	5	2	16	36					✓
	CY8C4024FNI-S412	24	16	2	0	1	1	0	2	5	2	8	21	✓				
	CY8C4024LQI-S411	24	16	2	0	1	1	0	2	5	2	8	19		✓			
	CY8C4024LQI-S412	24	16	2	0	1	1	0	2	5	2	16	27			✓		
	CY8C4024LQI-S413	24	16	2	0	1	1	0	2	5	2	16	34				✓	
	CY8C4024AZI-S413	24	16	2	0	1	1	0	2	5	2	16	36					✓
4025	CY8C4025FNI-S402	24	32	4	0	0	1	0	2	5	2	8	21	✓				
	CY8C4025LQI-S401	24	32	4	0	0	1	0	2	5	2	8	19		✓			
	CY8C4025LQI-S402	24	32	4	0	0	1	0	2	5	2	16	27			✓		
	CY8C4025AZI-S403	24	32	4	0	0	1	0	2	5	2	16	36					✓
	CY8C4025FNI-S412	24	32	4	0	1	1	0	2	5	2	8	21	✓				
	CY8C4025LQI-S411	24	32	4	0	1	1	0	2	5	2	8	19		✓			
	CY8C4025LQI-S412	24	32	4	0	1	1	0	2	5	2	16	27			✓		
	CY8C4025AZI-S413	24	32	4	0	1	1	0	2	5	2	16	36					✓
4045	CY8C4045FNI-S412	48	32	4	0	1	1	0	2	5	2	8	21	✓				
	CY8C4045LQI-S411	48	32	4	0	1	1	0	2	5	2	8	19		✓			
	CY8C4045LQI-S412	48	32	4	0	1	1	0	2	5	2	16	27			✓		
	CY8C4045AZI-S413	48	32	4	0	1	1	0	2	5	2	16	36					✓

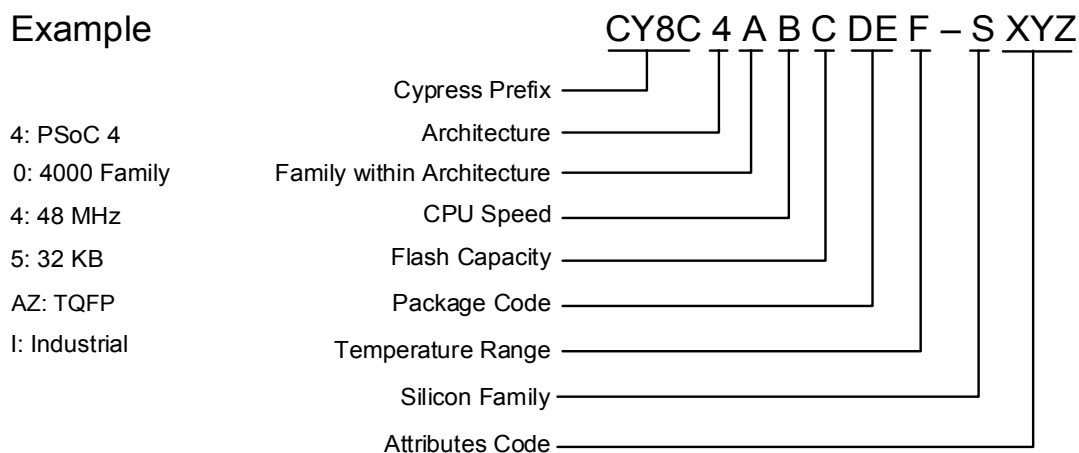
The nomenclature used in the preceding table is based on the following part numbering convention:

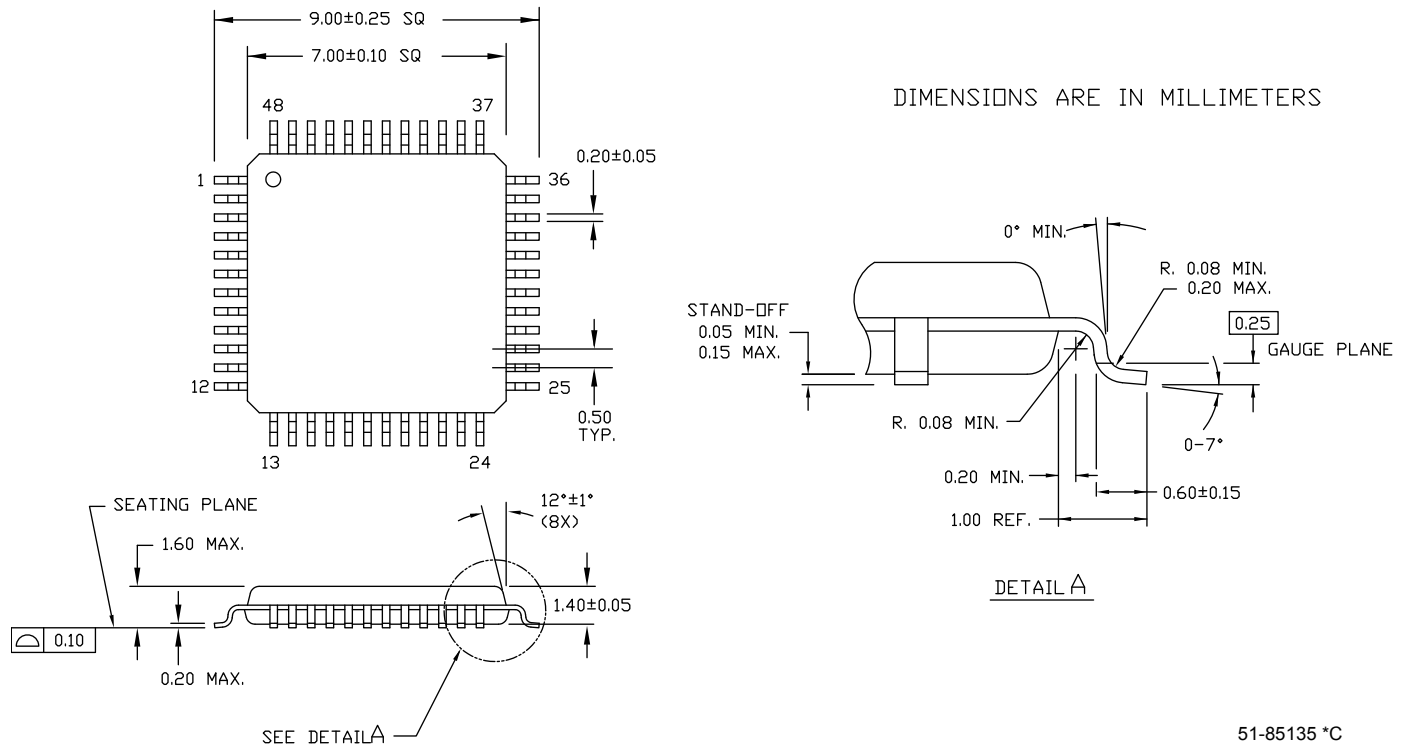
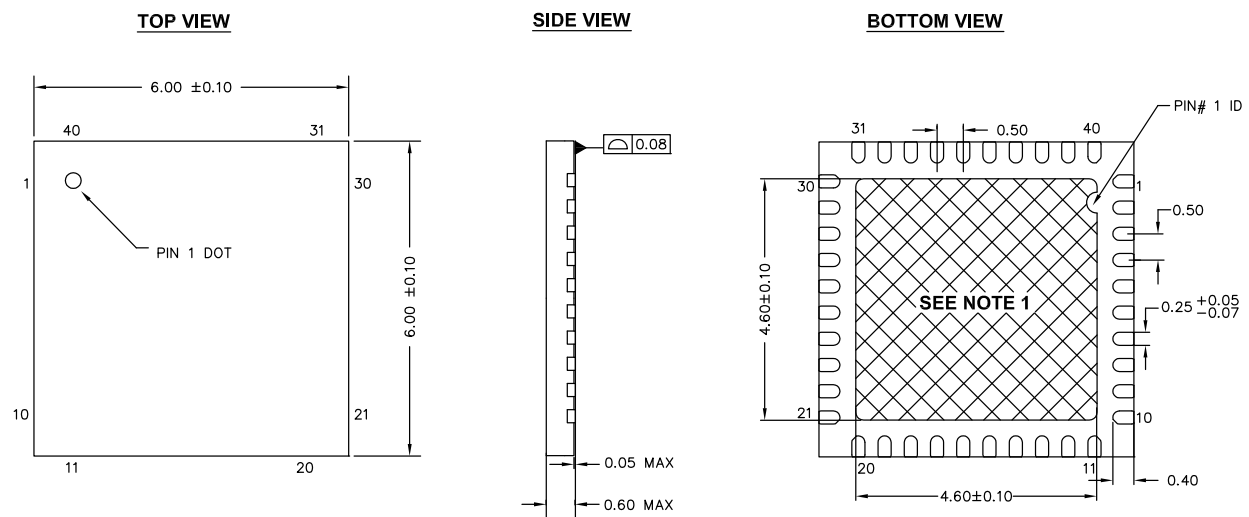
Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	0	4000 Family
B	CPU Speed	2	24 MHz
		4	48 MHz


Field	Description	Values	Meaning
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	S	PSoC 4A-S1, PSoC 4A-S2
		M	PSoC 4A-M
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

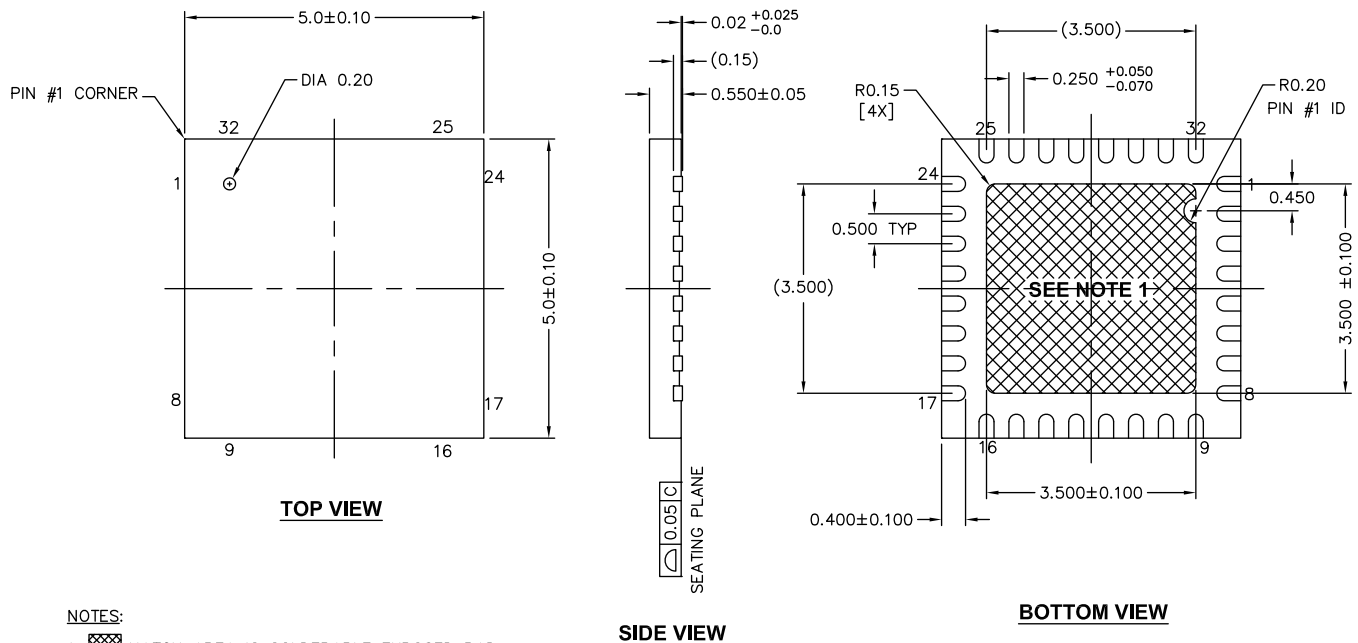
### Example



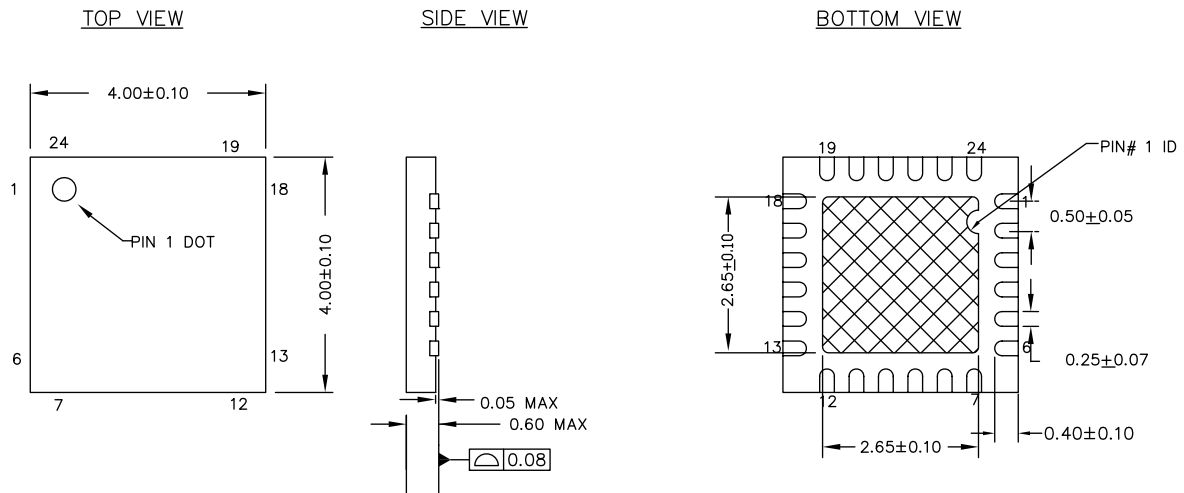
**Package Diagrams**
**Figure 5. 48-pin TQFP Package Outline**

**Figure 6. 40-pin QFN Package Outline**

**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 \*A

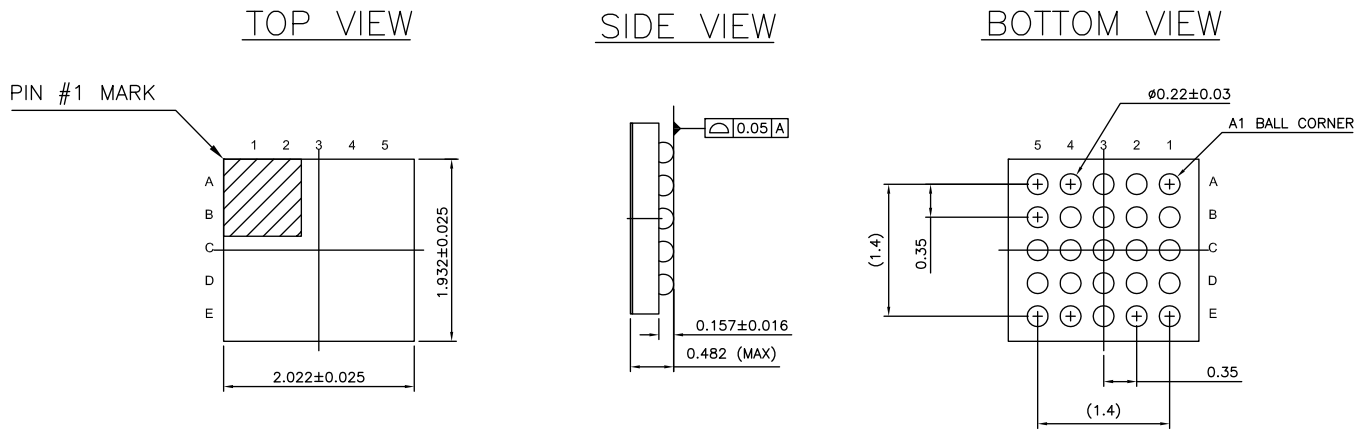
**Figure 7. 32-pin QFN Package Outline**


001-42168 \*E

**Figure 8. 24-pin QFN Package Outline**


001-13937 \*F

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

**Figure 9. 25-Ball WLCSP**


ALL DIMENSIONS ARE IN MM  
 JEDEC Publication 95; Design Guide 4.18

002-09957 \*\*

## Revision History

Description Title: PSoC® 4: PSoC 4000S Family Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-00123				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4883809	WKA	08/28/2015	New datasheet
*A	4992376	WKA	10/30/2015	Updated <a href="#">Pinouts</a> . Added $V_{DD} \geq 2.2V$ at $-40^{\circ}C$ under Conditions for specs SID247A, SID90, SID92. Updated <a href="#">Table 12</a> . Updated <a href="#">Ordering Information</a> .
*B	5037826	SLAN	12/08/2015	Changed datasheet status to Preliminary
*C	5104369	WKA	01/27/2016	Added Errata. Added 25 WLCSP package details. Updated theta $J_A$ and $J_C$ values for all packages.
*D	5139206	WKA	02/16/2016	Updated copyright information at the end of the document.
*E	5173961	WKA	03/15/2016	Updated <a href="#">Pinouts</a> . Updated values for SID79, BID194, SID175, and SID176. Updated <a href="#">CSD and IDAC Specifications</a> . Updated <a href="#">10-bit CapSense ADC Specifications</a> .
*F	5268662	WKA	05/12/2016	Updated <a href="#">Alternate Pin Functions</a> . Updated the following specs: SID310, SID312, SID313, SID314, SID314C, SID314D, SID314E, SID315, SID315C, SID315D, SID315E, SID322A, SID322B, SIDA109. Removed Errata section. Updated the Cypress logo and copyright information based on the template.
*G	5330930	WKA	07/27/2016	Updated <a href="#">LCD Segment Drive</a> . Updated SID60 conditions. Updated IDD specs. Corrected package dimensions for WLCSP package and added WLCSP MSL condition. Moved datasheet status to Final.
*H	5415365	WKA	09/14/2016	Added 40-pin QFN pin and package details. Updated IDD spec values in <a href="#">DC Specifications</a> .
*I	5561833	WKA	01/09/2017	Changed PRGIO references to Smart I/O.
*J	5704046	GNKK	04/26/2017	Updated the Cypress logo and copyright information.