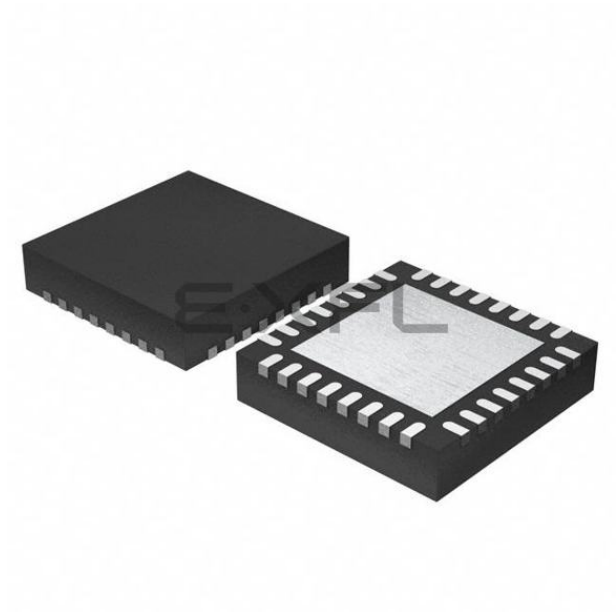

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## What is "Embedded - Microcontrollers"?

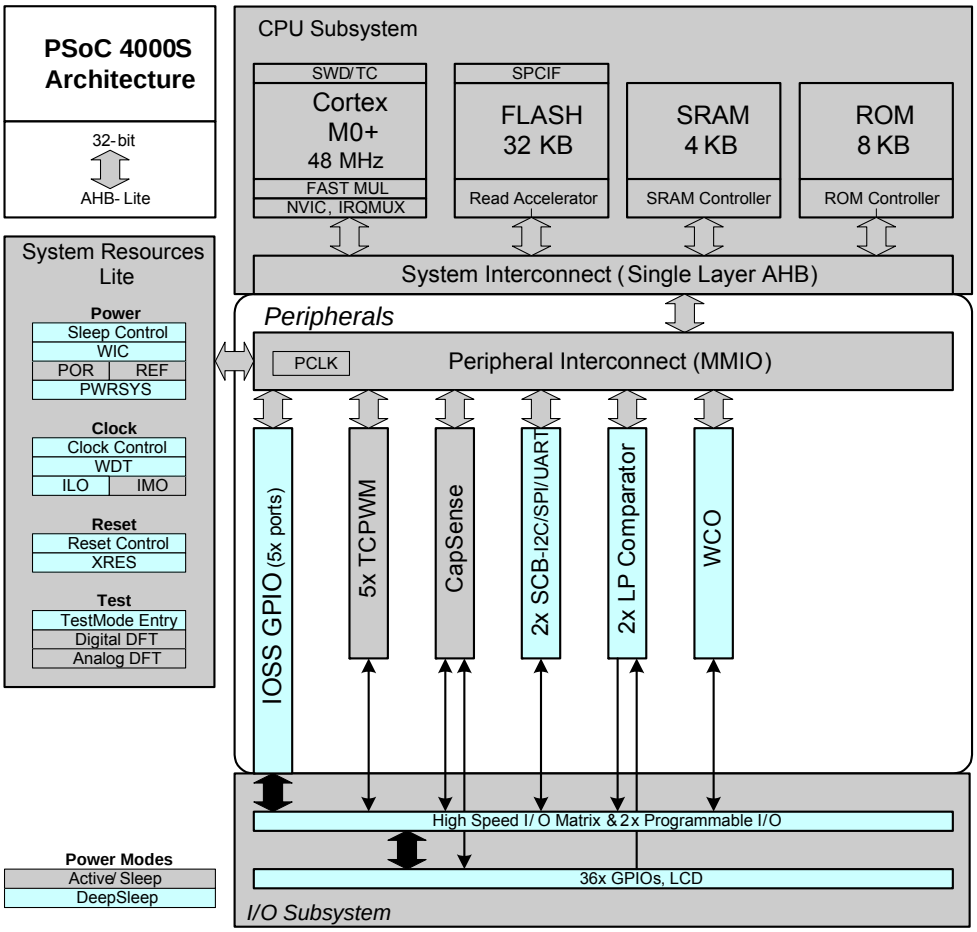
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4045lqi-s412 |

## Contents

**Figure 1. Block Diagram**




PSoC 4000S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4000S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4000S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4000S allows the customer to make.

# Functional Definition

## CPU and Memory Subsystem

### *CPU*

The Cortex-M0+ CPU in the PSoC 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4000S has four breakpoint (address) comparators and two watchpoint (data) comparators.

### *Flash*

The PSoC 4000S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

### *SRAM*

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

### *SROM*

A supervisory ROM that contains boot and configuration routines is provided.

## System Resources

### *Power System*

The power system is described in detail in the section Power on page 10. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC 4000S operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC 4000S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

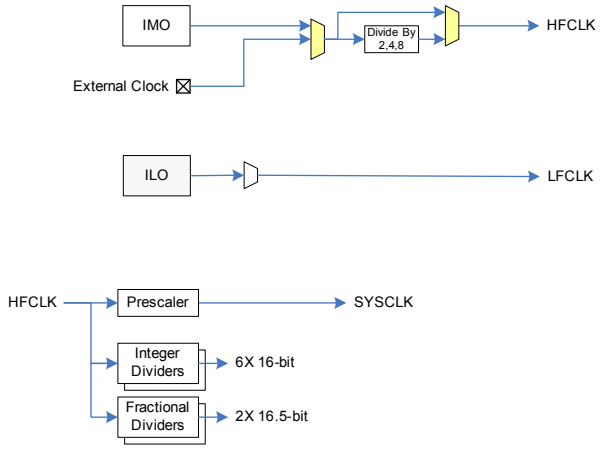
### *Clock System*

The PSoC 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC Creator.

**Figure 2. PSoC 4000S MCU Clocking Architecture**




### *IMO Clock Source*

The IMO is the primary source of internal clocking in the PSoC 4000S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

### *ILO Clock Source*

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

### *Watch Crystal Oscillator (WCO)*

The PSoC 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

*Watchdog Timer*

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

*Reset*

The PSoC 4000S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

*Voltage Reference*

The PSoC 4000S reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a ±5% reference.

## Analog Blocks

*Low-power Comparators (LPC)*

The PSoC 4000S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

*Current DACs*

The PSoC 4000S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

*Analog Multiplexed Buses*

The PSoC 4000S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

## Programmable Digital Blocks

The programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

## Fixed Function Digital

*Timer/Counter/PWM (TCPWM) Block*

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC 4000S.

*Serial Communication Block (SCB)*

The PSoC 4000S has two serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

**I²C Mode**: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC 4000S and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC 4000S is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

## Pinouts

The following table provides the pin list for PSoC 4000S for the 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, and 25-ball CSP packages. All port pins support GPIO. Pin 11 is a No-Connect in the 48-TQFP.

**Table 1. PSoC 4000S Pin List**

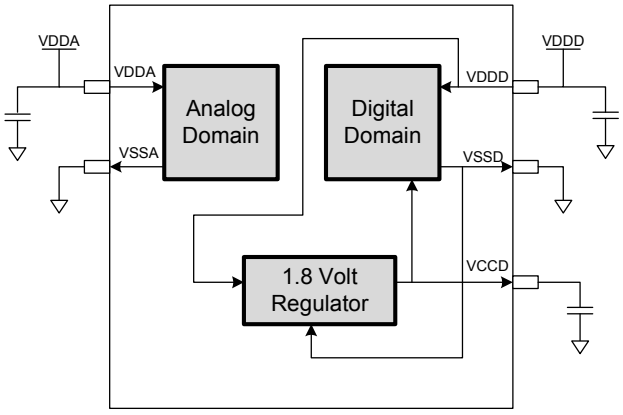
| 48-TQFP | | 32-QFN | | 24-QFN | | 25-CSP | | 40-QFN | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 28 | P0.0 | 17 | P0.0 | 13 | P0.0 | D1 | P0.0 | 22 | P0.0 |
| 29 | P0.1 | 18 | P0.1 | 14 | P0.1 | C3 | P0.1 | 23 | P0.1 |
| 30 | P0.2 | 19 | P0.2 | | | | | 24 | P0.2 |
| 31 | P0.3 | 20 | P0.3 | | | | | 25 | P0.3 |
| 32 | P0.4 | 21 | P0.4 | 15 | P0.4 | C2 | P0.4 | 26 | P0.4 |
| 33 | P0.5 | 22 | P0.5 | 16 | P0.5 | C1 | P0.5 | 27 | P0.5 |
| 34 | P0.6 | 23 | P0.6 | 17 | P0.6 | B1 | P0.6 | 28 | P0.6 |
| 35 | P0.7 | | | | | B2 | P0.7 | 29 | P0.7 |
| 36 | XRES | 24 | XRES | 18 | XRES | B3 | XRES | 30 | XRES |
| 37 | VCCD | 25 | VCCD | 19 | VCCD | A1 | VCCD | 31 | VCCD |
| 38 | VSSD | 26 | VSSD | 20 | VSSD | A2 | VSS | | |
| 39 | VDDD | 27 | VDD | 21 | VDD | A3 | VDD | 32 | VDDD |
| 40 | VDDA | 27 | VDD | 21 | VDD | A3 | VDD | 33 | VDDA |
| 41 | VSSA | 28 | VSSA | 22 | VSSA | A2 | VSS | 34 | VSSA |
| 42 | P1.0 | 29 | P1.0 | | | | | 35 | P1.0 |
| 43 | P1.1 | 30 | P1.1 | | | | | 36 | P1.1 |
| 44 | P1.2 | 31 | P1.2 | 23 | P1.2 | A4 | P1.2 | 37 | P1.2 |
| 45 | P1.3 | 32 | P1.3 | 24 | P1.3 | B4 | P1.3 | 38 | P1.3 |
| 46 | P1.4 | | | | | | | 39 | P1.4 |
| 47 | P1.5 | | | | | | | | |
| 48 | P1.6 | | | | | | | | |
| 1 | P1.7 | 1 | P1.7 | 1 | P1.7 | A5 | P1.7 | 40 | P1.7 |
| 2 | P2.0 | 2 | P2.0 | 2 | P2.0 | B5 | P2.0 | 1 | P2.0 |
| 3 | P2.1 | 3 | P2.1 | 3 | P2.1 | C5 | P2.1 | 2 | P2.1 |
| 4 | P2.2 | 4 | P2.2 | | | | | 3 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | | | | | 4 | P2.3 |
| 6 | P2.4 | | | | | | | 5 | P2.4 |
| 7 | P2.5 | 6 | P2.5 | | | | | 6 | P2.5 |
| 8 | P2.6 | 7 | P2.6 | 4 | P2.6 | D5 | P2.6 | 7 | P2.6 |
| 9 | P2.7 | 8 | P2.7 | 5 | P2.7 | C4 | P2.7 | 8 | P2.7 |
| 10 | VSSD | | | | | A2 | VSS | 9 | VSSD |
| 12 | P3.0 | 9 | P3.0 | 6 | P3.0 | E5 | P3.0 | 10 | P3.0 |
| 13 | P3.1 | 10 | P3.1 | | | D4 | P3.1 | 11 | P3.1 |
| 14 | P3.2 | 11 | P3.2 | 7 | P3.2 | E4 | P3.2 | 12 | P3.2 |
| 16 | P3.3 | 12 | P3.3 | 8 | P3.3 | D3 | P3.3 | 13 | P3.3 |

| Port/ Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|---|---|---|---|---|---|---|---|
| P1.6 | | | | | | | scb[0].spi_select3:1 |
| P1.7 | | | | | | | |
| P2.0 | | prgio[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | | prgio[0].io[1] | tcpwm.line_compl[4]:0 | | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | | prgio[0].io[2] | | | | | scb[1].spi_clk:2 |
| P2.3 | | prgio[0].io[3] | | | | | scb[1].spi_select0:2 |
| P2.4 | | prgio[0].io[4] | tcpwm.line[0]:1 | | | | scb[1].spi_select1:1 |
| P2.5 | | prgio[0].io[5] | tcpwm.line_compl[0]:1 | | | | scb[1].spi_select2:1 |
| P2.6 | | prgio[0].io[6] | tcpwm.line[1]:1 | | | | scb[1].spi_select3:1 |
| P2.7 | | prgio[0].io[7] | tcpwm.line_compl[1]:1 | | | lpcomp.comp[0]:1 | |
| P3.0 | | prgio[1].io[0] | tcpwm.line[0]:0 | scb[1].uart_rx:1 | | scb[1].i2c_scl:2 | scb[1].spi_mosi:0 |
| P3.1 | | prgio[1].io[1] | tcpwm.line_compl[0]:0 | scb[1].uart_tx:1 | | scb[1].i2c_sda:2 | scb[1].spi_miso:0 |
| P3.2 | | prgio[1].io[2] | tcpwm.line[1]:0 | scb[1].uart_cts:1 | | cpuss.swd_data | scb[1].spi_clk:0 |
| P3.3 | | prgio[1].io[3] | tcpwm.line_compl[1]:0 | scb[1].uart_rts:1 | | cpuss.swd_clk | scb[1].spi_select0:0 |
| P3.4 | | prgio[1].io[4] | tcpwm.line[2]:0 | | tcpwm.tr_in[6] | | scb[1].spi_select1:0 |
| P3.5 | | prgio[1].io[5] | tcpwm.line_compl[2]:0 | | tcpwm.tr_in[7] | | scb[1].spi_select2:0 |
| P3.6 | | prgio[1].io[6] | tcpwm.line[3]:0 | | tcpwm.tr_in[8] | | scb[1].spi_select3:0 |
| P3.7 | | prgio[1].io[7] | tcpwm.line_compl[3]:0 | | tcpwm.tr_in[9] | lpcomp.comp[1]:1 | |
| P4.0 | csd.vref_ext | | | scb[0].uart_rx:0 | tcpwm.tr_in[10] | scb[0].i2c_scl:1 | scb[0].spi_mosi:0 |
| P4.1 | csd.cshieldpads | | | scb[0].uart_tx:0 | tcpwm.tr_in[11] | scb[0].i2c_sda:1 | scb[0].spi_miso:0 |
| P4.2 | csd.cmodpad | | | scb[0].uart_cts:0 | | lpcomp.comp[0]:0 | scb[0].spi_clk:0 |
| P4.3 | csd.csh_tank | | | scb[0].uart_rts:0 | | lpcomp.comp[1]:0 | scb[0].spi_select0:0 |
| | | | | | | | |

## Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4000S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the $V_{DD}$ input.

**Figure 3. Power Supply Connections**




There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

### Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the PSoC 4000S is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4000S supplies the internal logic and its output is connected to the $V_{CCD}$ pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

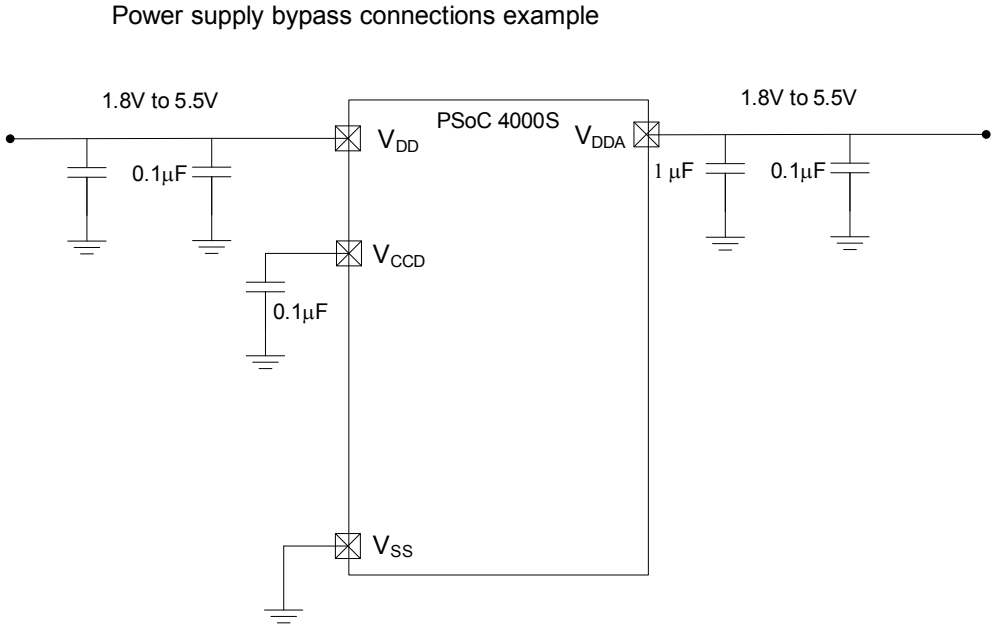
### Mode 2: 1.8 V ±5% External Supply

In this mode, the PSoC 4000S is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

**Figure 4. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active**



## Development Support

The PSoC 4000S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4000S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4000S family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

**Table 6. GPIO AC Specifications**

(Guaranteed by Characterization) *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID74 | $F_{GPIOUT1}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Fast strong mode | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | $F_{GPIOUT2}$ | GPIO $F_{OUT}$; 1.71 V≤ $V_{DDD}$≤ 3.3 V Fast strong mode | – | – | 16.7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | $F_{GPIOUT3}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DDD}$ ≤ 5.5 V Slow strong mode | – | – | 7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | $F_{GPIOUT4}$ | GPIO $F_{OUT}$; 1.71 V ≤ $V_{DDD}$ ≤ 3.3 V Slow strong mode. | – | – | 3.5 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | $F_{GPIOIN}$ | GPIO input operating frequency; 1.71 V ≤ $V_{DDD}$ ≤ 5.5 V | – | – | 48 | | 90/10% $V_{IO}$ |

*XRES*

**Table 7. XRES DC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID77 | $V_{IH}$ | Input voltage high threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS Input |
| SID78 | $V_{IL}$ | Input voltage low threshold | – | – | 0.3 × $V_{DDD}$ | | |
| SID79 | $R_{PULLUP}$ | Pull-up resistor | – | 60 | – | kΩ | – |
| SID80 | $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| SID81[5] | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Typical hysteresis is 200 mV for $V_{DD}$ > 4.5 V |
| SID82 | $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | |

**Table 8. XRES AC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID83[5] | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | µs | – |
| BID194[5] | $T_{RESETWAKE}$ | Wake-up time from reset release | – | – | 2.7 | ms | – |

**Note**
5. Guaranteed by characterization.

*CSD*

**Table 11. CSD and IDAC Specifications**

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD}$ > 2 V (with ripple), 25 °C $T_A$, Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD}$ > 1.75V (with ripple), 25 °C $T_A$, Parasitic Capacitance ($C_P$) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | µA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator. |
| SID.CSD#15 | $V_{REF}$ | Voltage reference for CSD and Comparator | 0.6 | 1.2 | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#15A | VREF_EXT | External Voltage reference for CSD and Comparator | 0.6 | | $V_{DDA}$ - 0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | µA | |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | µA | |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ±5% or 1.8 V to 5.5 V |
| SID308A | VCOMPIDAC | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA}$ –0.6 | V | $V_{DDA}$ - 0.06 or 4.4, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA}$ < 2 V |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. $V_{DDA}$ > 2 V. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID314A | IDAC1CRT2 | Output current of IDAC1(7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID314B | IDAC1CRT3 | Output current of IDAC1(7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID314D | IDAC1CRT22 | Output current of IDAC1(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID314E | IDAC1CRT32 | Output current of IDAC1(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | µA | LSB = 37.5-nA typ. |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | µA | LSB = 300-nA typ. |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | µA | LSB = 2.4-µA typ. |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | µA | LSB = 75-nA typ. |
| SID315D | IDAC2CRT22 | Output current of IDAC2(7 bits) in medium range, 2X mode | 69 | – | 82 | µA | LSB = 600-nA typ. |
| SID315E | IDAC2CRT32 | Output current of IDAC2(7 bits) in high range, 2X mode | 540 | – | 660 | µA | LSB = 4.8-µA typ. |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | µA | LSB = 37.5-nA typ. |

**Table 11. CSD and IDAC Specifications** *(continued)*

| SPEC ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID315G | IDAC3CRT23 | Output current of IDAC in 8-bit mode in medium range | 69 | – | 82 | µA | LSB = 300-nA typ. |
| SID315H | IDAC3CRT33 | Output current of IDAC in 8-bit mode in high range | 540 | – | 660 | µA | LSB = 2.4-µA typ. |
| SID320 | IDACOFFSET | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode |
| SID321 | IDACGAIN | Full-scale error less offset | – | – | ±10 | % | |
| SID322 | IDACMISMATCH1 | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | IDACMISMATCH2 | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 5.6 | LSB | LSB = 300-nA typ. |
| SID322B | IDACMISMATCH3 | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 6.8 | LSB | LSB = 2.4-µA typ. |
| SID323 | IDACSET8 | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID324 | IDACSET7 | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | µs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

**Table 12. 10-bit CapSense ADC Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SIDA95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | Defined by AMUX Bus. |
| SIDA97 | A-MONO | Monotonicity | – | – | – | Yes | |
| SIDA98 | A_GAINERR | Gain error | – | – | ±2 | % | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA99 | A_OFFSET | Input offset voltage | – | – | 3 | mV | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA100 | A_ISAR | Current consumption | – | – | 0.25 | mA | |
| SIDA101 | A_VINS | Input voltage range - single ended | $V_{SSA}$ | – | $V_{DDA}$ | V | |
| SIDA103 | A_INRES | Input resistance | – | 2.2 | – | KΩ | |
| SIDA104 | A_INCAP | Input capacitance | – | 20 | – | pF | |
| SIDA106 | A_PSRR | Power supply rejection ratio | – | 60 | – | dB | In $V_{REF}$ (2.4 V) mode with $V_{DDA}$ bypass capacitance of 10 µF |
| SIDA107 | A_TACQ | Sample acquisition time | – | 1 | – | µs | |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 21.3 | µs | Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz. | – | – | 85.3 | µs | Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time. |

*I²C*

**Table 14. Fixed I²C DC Specifications**[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID149 | $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 50 | µA | – |
| SID150 | $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 135 | | – |
| SID151 | $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 310 | | – |
| SID152 | $I_{I2C4}$ | I²C enabled in Deep Sleep mode | – | – | 1.4 | | |

**Table 15. Fixed I²C AC Specifications**[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID153 | $F_{I2C1}$ | Bit rate | – | – | 1 | Msps | – |

**Table 16. SPI DC Specifications**[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID163 | ISPI1 | Block current consumption at 1 Mbps | – | – | 360 | µA | – |
| SID164 | ISPI2 | Block current consumption at 4 Mbps | – | – | 560 | | – |
| SID165 | ISPI3 | Block current consumption at 8 Mbps | – | – | 600 | | – |

**Table 17. SPI AC Specifications**[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID166 | FSPI | SPI operating frequency (Master; 6X Oversampling) | – | – | 8 | MHz | |
| **Fixed SPI Master Mode AC Specifications** | | | | | | | |
| SID167 | TDMO | MOSI Valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | TDSI | MISO Valid before SClock capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | THMO | Previous MOSI data hold time | 0 | – | – | | Referred to Slave capturing edge |
| **Fixed SPI Slave Mode AC Specifications** | | | | | | | |
| SID170 | TDMI | MOSI Valid before Sclock Capturing edge | 40 | – | – | ns | – |
| SID171 | TDSO | MISO Valid after Sclock driving edge | – | – | 42 + 3*Tcpu | | $T_{CPU} = 1/F_{CPU}$ |
| SID171A | TDSO_EXT | MISO Valid after Sclock driving edge in Ext. Clk mode | – | – | 48 | | – |
| SID172 | THSO | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | TSSELSSCK | SSEL Valid to first SCK Valid edge | – | – | 100 | ns | – |

**Note**
7. Guaranteed by characterization.

**Table 18. UART DC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbps | – | – | 55 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbps | – | – | 312 | µA | – |

**Table 19. UART AC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Table 20. LCD Direct Drive DC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID154 | $I_{LCDLOW}$ | Operating current in low power mode | _ | 5 | – | µA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | _ | 500 | 5000 | pF | – |
| SID156 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | $I_{LCDOP1}$ | LCD system operating current Vbias = 5 V | _ | 2 | – | mA | 32 × 4 segments. 50 Hz. 25 °C |
| SID158 | $I_{LCDOP2}$ | LCD system operating current Vbias = 3.3 V | _ | 2 | – | | 32 × 4 segments. 50 Hz. 25 °C |

**Table 21. LCD Direct Drive AC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID159 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

**Note**
8. Guaranteed by characterization.

## Memory

**Table 22. Flash DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID173 | $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | – |

**Table 23. Flash AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID174 | $T_{ROWWRITE}$[9] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | $T_{ROWERASE}$[9] | Row erase time | – | – | 16 | | – |
| SID176 | $T_{ROWPROGRAM}$[9] | Row program time after erase | – | – | 4 | | – |
| SID178 | $T_{BULKERASE}$[9] | Bulk erase time (32 KB) | – | – | 35 | | – |
| SID180[10] | $T_{DEVPROG}$[9] | Total device program time | – | – | 7 | Seconds | – |
| SID181[10] | $F_{END}$ | Flash endurance | 100 K | – | – | Cycles | – |
| SID182[10] | $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles | 20 | – | – | Years | – |
| SID182A[10] | – | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles | 10 | – | – | | – |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | | CPU execution from Flash |

## System Resources

*Power-on Reset (POR)*

**Table 24. Power On Reset (PRES)**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up |
| SID185[10] | $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186[10] | $V_{FALLIPOR}$ | Falling trip voltage | 0.70 | – | 1.4 | | – |

**Table 25. Brown-out Detect (BOD) for $V_{CCD}$**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID190[10] | $V_{FALLPPOR}$ | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192[10] | $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

**Notes**
9. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
10. Guaranteed by characterization.

*SWD Interface*

**Table 26. SWD Interface Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID213 | F_SWDCLK1 | 3.3 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | 1.71 V ≤ $V_{DD}$ ≤ 3.3 V | – | – | 7 | | SWDCLK ≤ 1/3 CPU clock frequency |
| SID215[11] | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25*T | – | – | ns | – |
| SID216[11] | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25*T | – | – | | – |
| SID217[11] | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5*T | | – |
| SID217A[11] | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | | – |

*Internal Main Oscillator*

**Table 27. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 250 | µA | – |
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 180 | µA | – |

**Table 28. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2 | % | |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 7 | µs | – |
| SID228 | $T_{JITRMSIMO2}$ | RMS jitter at 24 MHz | – | 145 | – | ps | – |

*Internal Low-Speed Oscillator*

**Table 29. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231[11] | $I_{ILO1}$ | ILO operating current | – | 0.3 | 1.05 | µA | – |

**Table 30. ILO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234[11] | $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | – |
| SID236[11] | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | $F_{ILOTRIM1}$ | ILO frequency range | 20 | 40 | 80 | kHz | – |

**Note**
11. Guaranteed by characterization.

**Table 31. Watch Crystal Oscillator (WCO) Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID398 | FWCO | Crystal Frequency | – | 32.768 | – | kHz | |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | |
| SID401 | PD | Drive Level | – | – | 1 | µW | |
| SID402 | TSTART | Startup time | – | – | 500 | ms | |
| SID403 | CL | Crystal Load Capacitance | 6 | – | 12.5 | pF | |
| SID404 | C0 | Crystal Shunt Capacitance | – | 1.35 | – | pF | |
| SID405 | IWCO1 | Operating Current (high power mode) | – | – | 8 | uA | |
| SID406 | IWCO2 | Operating Current (low power mode) | – | – | 1 | uA | |

**Table 32. External Clock Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID305[12] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306[12] | ExtClkDuty | Duty cycle; measured at $V_{DD/2}$ | 45 | – | 55 | % | – |

**Table 33. Block Specs**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID262[12] | $T_{CLKSWITCH}$ | System clock source switching time | 3 | – | 4 | Periods | – |

**Table 34. Smart I/O Pass-through Time (Delay in Bypass Mode)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

**Note**
12. Guaranteed by characterization.

## Packaging

The PSoC 4000S will be offered in 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, and 25-ball WLCSP packages. Package dimensions and Cypress drawing numbers are in the following table.

**Table 36. Package List**

| Spec ID# | Package | Description | Package Dwg |
|---|---|---|---|
| BID20 | 48-pin TQFP | 7 × 7 × 1.4 mm height with 0.5-mm pitch | 51-85135 |
| BID27 | 40-pin QFN | 6 × 6 × 0.6 mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32-pin QFN | 5 × 5 × 0.6 mm height with 0.5-mm pitch | 001-42168 |
| BID34 | 24-pin QFN | 4 × 4 × 0.6 mm height with 0.5-mm pitch | 001-13937 |
| BID34F | 25-ball WLCSP | 2.02 × 1.93 × 0.48 mm height with 0.35-mm pitch | 002-09957 |

**Table 37. Package Thermal Characteristics**

| Parameter | Description | Package | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | | –40 | 25 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ | 48-pin TQFP | – | 73.5 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 48-pin TQFP | – | 33.5 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 40-pin QFN | – | 17.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 40-pin QFN | – | 2.8 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 32-pin QFN | – | 20.8 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 32-pin QFN | – | 5.9 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 24-pin QFN | – | 21.7 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 24-pin QFN | – | 5.6 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ | 25-ball WLCSP | – | 54.6 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ | 25-ball WLCSP | – | 0.5 | – | °C/Watt |

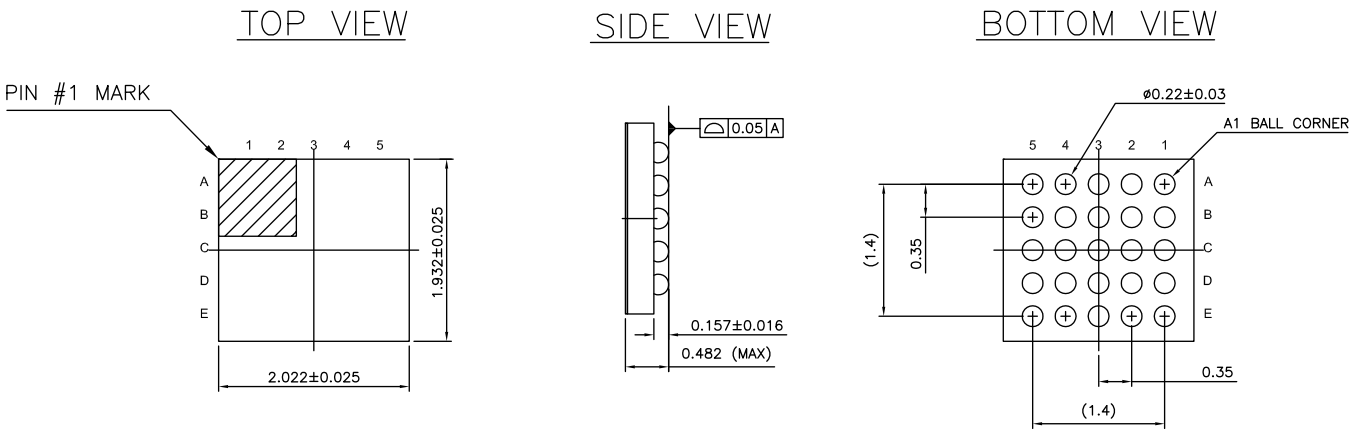
**Table 38. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| All | 260 °C | 30 seconds |

**Table 39. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020**

| Package | MSL |
|---|---|
| All except WLCSP | MSL 3 |
| 25-ball WLCSP | MSL 1 |

**Figure 9. 25-Ball WLCSP**

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## Acronyms

**Table 40. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 40. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

## Revision History

| Description Title: PSoC® 4: PSoC 4000S Family Datasheet Programmable System-on-Chip (PSoC)<br>Document Number: 002-00123 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 4883809 | WKA | 08/28/2015 | New datasheet |
| *A | 4992376 | WKA | 10/30/2015 | Updated Pinouts.<br>Added $V_{DDD}$ ≥ 2.2V at –40 °C under Conditions for specs SID247A, SID90, SID92.<br>Updated Table 12.<br>Updated Ordering Information. |
| *B | 5037826 | SLAN | 12/08/2015 | Changed datasheet status to Preliminary |
| *C | 5104369 | WKA | 01/27/2016 | Added Errata.<br>Added 25 WLCSP package details.<br>Updated theta $J_A$ and $J_C$ values for all packages. |
| *D | 5139206 | WKA | 02/16/2016 | Updated copyright information at the end of the document. |
| *E | 5173961 | WKA | 03/15/2016 | Updated Pinouts.<br>Updated values for SID79, BID194. SID175, and SID176.<br>Updated CSD and IDAC Specifications.<br>Updated 10-bit CapSense ADC Specifications. |
| *F | 5268662 | WKA | 05/12/2016 | Updated Alternate Pin Functions.<br>Updated the following specs:<br>SID310, SID312, SID313, SID314, SID314C, SID314D, SID314E, SID315, SID315C, SID315D, SID315E, SID322A, SID322B, SIDA109.<br>Removed Errata section.<br>Updated the Cypress logo and copyright information based on the template. |
| *G | 5330930 | WKA | 07/27/2016 | Updated LCD Segment Drive.<br>Updated SID60 conditions.<br>Updated IDD specs.<br>Corrected package dimensions for WLCSP package and added WLCSP MSL condition.<br>Moved datasheet status to Final. |
| *H | 5415365 | WKA | 09/14/2016 | Added 40-pin QFN pin and package details.<br>Updated IDD spec values in DC Specifications. |
| *I | 5561833 | WKA | 01/09/2017 | Changed PRGIO references to Smart I/O. |
| *J | 5704046 | GNKK | 04/26/2017 | Updated the Cypress logo and copyright information. |