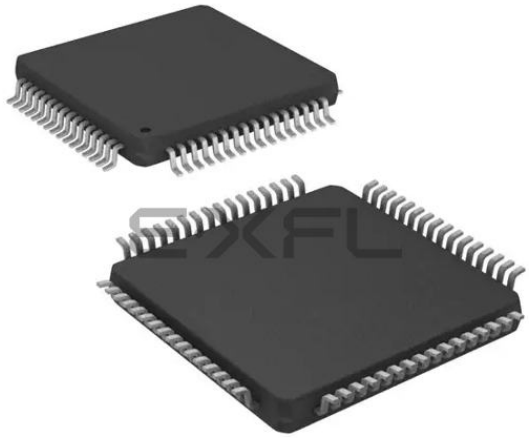

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f021-gq

Notes

1.7. 12-Bit Analog to Digital Converter

The C8051F020/1 has an on-chip 12-bit SAR ADC (ADC0) with a 9-channel input multiplexer and programmable gain amplifier. With a maximum throughput of 100 ksps, the ADC offers true 12-bit accuracy with an INL of ±1LSB. C8051F022/3 devices include a 10-bit SAR ADC with similar specifications and configuration options. The ADC0 voltage reference is selected between the DAC0 output and an external VREF pin. On C8051F020/2 devices, ADC0 has its own dedicated VREF0 input pin; on C8051F021/3 devices, the ADC0 shares the VREFA input pin with the 8-bit ADC1. The on-chip 15 ppm/°C voltage reference may generate the voltage reference for other system components or the on-chip ADCs via the VREF output pin.

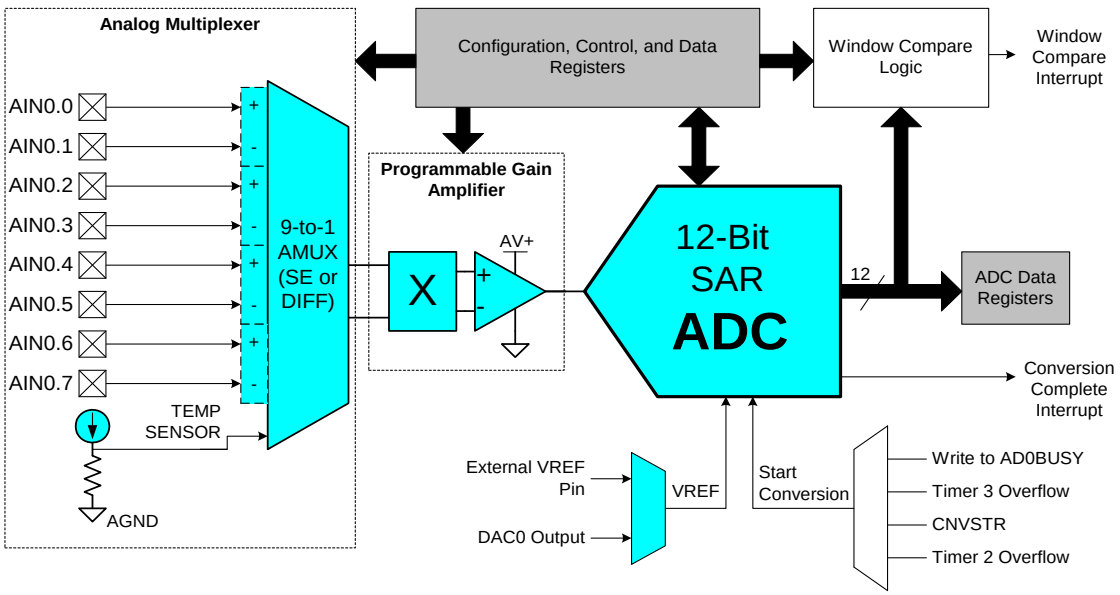
The ADC is under full control of the CIP-51 microcontroller via its associated Special Function Registers. One input channel is tied to an internal temperature sensor, while the other eight channels are available externally. Each pair of the eight external input channels can be configured as either two single-ended inputs or a single differential input. The system controller can also put the ADC into shutdown mode to save power.

A programmable gain amplifier follows the analog multiplexer. The gain can be set in software from 0.5 to 16 in powers of 2. The gain stage can be especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset (in differential mode, a DAC could be used to provide the DC offset).

Conversions can be started in four ways; a software command, an overflow of Timer 2, an overflow of Timer 3, or an external signal input. This flexibility allows the start of conversion to be triggered by software events, external HW signals, or a periodic timer overflow signal. Conversion completions are indicated by a status bit and an interrupt (if enabled). The resulting 10 or 12-bit data word is latched into two SFRs upon completion of a conversion. The data can be right or left justified in these registers under software control.

Window Compare registers for the ADC data can be configured to interrupt the controller when ADC data is within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within the specified window.

Figure 1.11. 12-Bit ADC Block Diagram



Notes

Figure 5.11. ADC0 Data Word Example (C8051F020/1)

12-bit ADC0 Data Word appears in the ADC0 Data Word Registers as follows:

ADC0H[3:0]:ADC0L[7:0], if AD0LJST = 0

(ADC0H[7:4] will be sign-extension of ADC0H.3 for a differential reading, otherwise = 0000b).

ADC0H[7:0]:ADC0L[7:4], if AD0LJST = 1

(ADC0L[3:0] = 0000b).

Example: ADC0 Data Word Conversion Map, AIN0 Input in Single-Ended Mode

(AMX0CF = 0x00, AMX0SL = 0x00)

AIN0-AGND (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF * (4095/4096)	0x0FFF	0xFFF0
VREF / 2	0x0800	0x8000
VREF * (2047/4096)	0x07FF	0x7FF0
0	0x0000	0x0000

Example: ADC0 Data Word Conversion Map, AIN0-AIN1 Differential Input Pair

(AMX0CF = 0x01, AMX0SL = 0x00)

AIN0-AGND (Volts)	**ADC0H:ADC0L** (AD0LJST = 0)	**ADC0H:ADC0L** (AD0LJST = 1)
VREF * (2047/2048)	0x07FF	0x7FF0
VREF / 2	0x0400	0x4000
VREF * (1/2048)	0x0001	0x0010
0	0x0000	0x0000
-VREF * (1/2048)	0xFFFF (-1d)	0xFFF0
-VREF / 2	0xFC00 (-1024d)	0xC000
-VREF	0xF800 (-2048d)	0x8000

For AD0LJST = 0:

$$Code = Vin \times \frac{Gain}{VREF} \times 2^n$$; 'n' = 12 for Single-Ended; 'n'=11 for Differential.

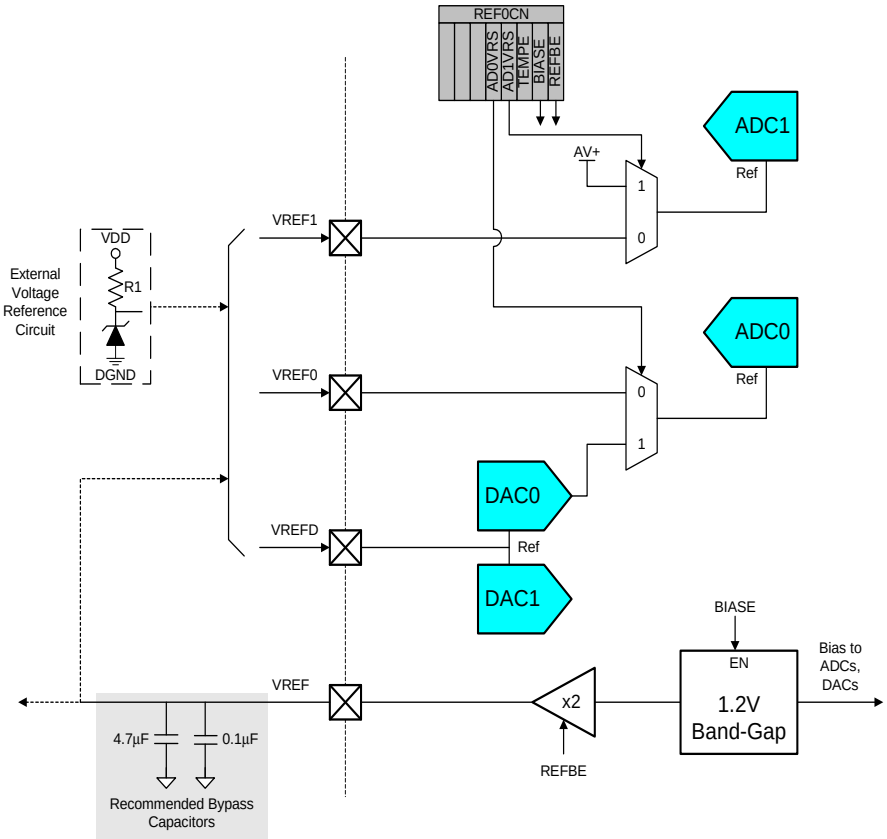
9. VOLTAGE REFERENCE (C8051F020/2)

The voltage reference circuit offers full flexibility in operating the ADC and DAC modules. Three voltage reference input pins allow each ADC and the two DACs to reference an external voltage reference or the on-chip voltage reference output. ADC0 may also reference the DAC0 output internally, and ADC1 may reference the analog power supply voltage, via the VREF multiplexers shown in Figure 9.1.

The internal voltage reference circuit consists of a 1.2 V, 15 ppm/°C (typical) bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the voltage reference input pins shown in Figure 9.1. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to AGND, as shown in Figure 9.1. See Table 9.1 for voltage reference specifications.

The Reference Control Register, REF0CN (defined in Figure 9.2) enables/disables the internal reference generator and selects the reference inputs for ADC0 and ADC1. The BIASE bit in REF0CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 µA (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if either DAC or ADC is used, regardless of whether the voltage reference is derived from the on-chip reference or supplied by an off-chip source. If neither the ADC nor the DAC are being used, both of these bits can be set to logic 0 to conserve power. Bits AD0VRS and AD1VRS select the ADC0 and ADC1 voltage reference sources, respectively. The electrical specifications for the Voltage Reference circuit are given in Table 9.1.

Figure 9.1. Voltage Reference Functional Block Diagram



12.2.7. Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic l. Future product versions may use these bits to implement new features in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the datasheet associated with their corresponding system function.

Figure 12.3. SP: Stack Pointer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x81

Bits7-0: SP: Stack Pointer.
The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

Figure 12.4. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x82

Bits7-0: DPL: Data Pointer Low.
The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and FLASH memory.

Figure 12.5. DPH: Data Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0x83

Bits7-0: DPH: Data Pointer High.
The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and FLASH memory.

13.1. Power-on Reset

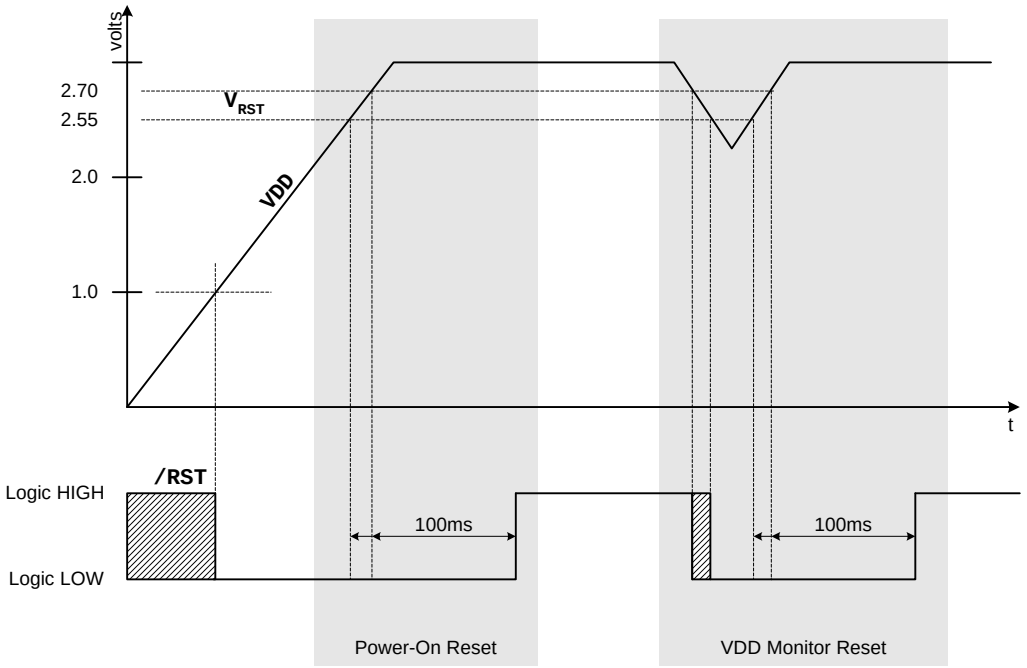
The C8051F020/1/2/3 family incorporates a power supply monitor that holds the MCU in the reset state until VDD rises above the V_{RST} level during power-up. See Figure 13.2 for timing diagram, and refer to Table 13.1 for the Electrical Characteristics of the power supply monitor circuit. The /RST pin is asserted low until the end of the 100 ms VDD Monitor timeout in order to allow the VDD supply to stabilize.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC Register are indeterminate. PORSF is cleared by all other resets. Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

The VDD monitor function is enabled by tying the MONEN pin directly to VDD. This is the recommended configuration for the MONEN pin.

.

Figure 13.2. Reset Timing



13.2. Power-fail Reset

When a power-down transition or power irregularity causes VDD to drop below V_{RST}, the power supply monitor will drive the /RST pin low and return the CIP-51 to the reset state. When VDD returns to a level above VRST, the CIP-51 will leave the reset state in the same manner as that for the power-on reset (see Figure 13.2). Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if VDD dropped below the level required for data retention. If the PORSF flag is set to logic 1, the data may no longer be valid.

MCU with proprietary value-added firmware before distribution. The value-added firmware can be protected while allowing additional code to be programmed in remaining program memory space later.

The Software Read Limit (SRL) is a 16-bit address that establishes two logical partitions in the program memory space. The first is an upper partition consisting of all the program memory locations at or above the SRL address, and the second is a lower partition consisting of all the program memory locations starting at 0x0000 up to (but excluding) the SRL address. Software in the upper partition can execute code in the lower partition, but is prohibited from reading locations in the lower partition using the MOVC instruction. (Executing a MOVC instruction from the upper partition with a source address in the lower partition will always return a data value of 0x00.) Software running in the lower partition can access locations in both the upper and lower partition without restriction.

The Value-added firmware should be placed in the lower partition. On reset, control is passed to the value-added firmware via the reset vector. Once the value-added firmware completes its initial execution, it branches to a predetermined location in the upper partition. If entry points are published, software running in the upper partition may execute program code in the lower partition, but it cannot read the contents of the lower partition. Parameters may be passed to the program code running in the lower partition either through the typical method of placing them on the stack or in registers before the call or by placing them in prescribed memory locations in the upper partition.

The SRL address is specified using the contents of the FLASH Access Register. The 16-bit SRL address is calculated as 0xNN00, where NN is the contents of the SRL Security Register. Thus, the SRL can be located on 256-byte boundaries anywhere in program memory space. However, the 512-byte erase sector size essentially requires that a 512 boundary be used. The contents of a non-initialized SRL security byte is 0x00, thereby setting the SRL address to 0x0000 and allowing read access to all locations in program memory space by default.

Figure 15.2. FLACL: FLASH Access Limit

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB7

Bits 7-0: FLACL: FLASH Access Limit.
This register holds the high byte of the 16-bit program memory read/write/erase limit address. The entire 16-bit access limit address value is calculated as 0xNN00 where NN is replaced by contents of FLACL. A write to this register sets the FLASH Access Limit. This register can only be written once after any reset. Any subsequent writes are ignored until the next reset.

Figure 15.4. PSCTL: Program Store Read/Write Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	SFLE	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8F

Bits7-3: UNUSED. Read = 00000b, Write = don't care.

Bit2: SFLE: Scratchpad FLASH Memory Access Enable.
When this bit is set, FLASH reads and writes from user software are directed to the 128-byte Scratch-pad FLASH sector. When SFLE is set to logic 1, FLASH accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes out of this range will yield unpredictable results.
0: FLASH access from user software directed to the 64k byte Program/Data FLASH sector.
1: FLASH access from user software directed to the 128 byte Scratchpad sector.

Bit1: PSEE: Program Store Erase Enable.
Setting this bit allows an entire page of the FLASH program memory to be erased provided the PSWE bit is also set. After setting this bit, a write to FLASH memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: FLASH program memory erasure disabled.
1: FLASH program memory erasure enabled.

Bit0: PSWE: Program Store Write Enable.
Setting this bit allows writing a byte of data to the FLASH program memory using the MOVX instruction. The location must be erased before writing data.
0: Write to FLASH program memory disabled.
1: Write to FLASH program memory enabled.

Figure 16.1. EMI0CN: External Memory Interface Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PGSEL7	PGSEL6	PGSEL5	PGSEL4	PGSEL3	PGSEL2	PGSEL1	PGSEL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xAF

Bits7-0: PGSEL[7:0]: XRAM Page Select Bits.
The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM.
0x00: 0x0000 to 0x00FF
0x01: 0x0100 to 0x01FF
...
0xFE: 0xFE00 to 0xFEFF
0xFF: 0xFF00 to 0xFFFF

Figure 16.2. EMI0CF: External Memory Configuration

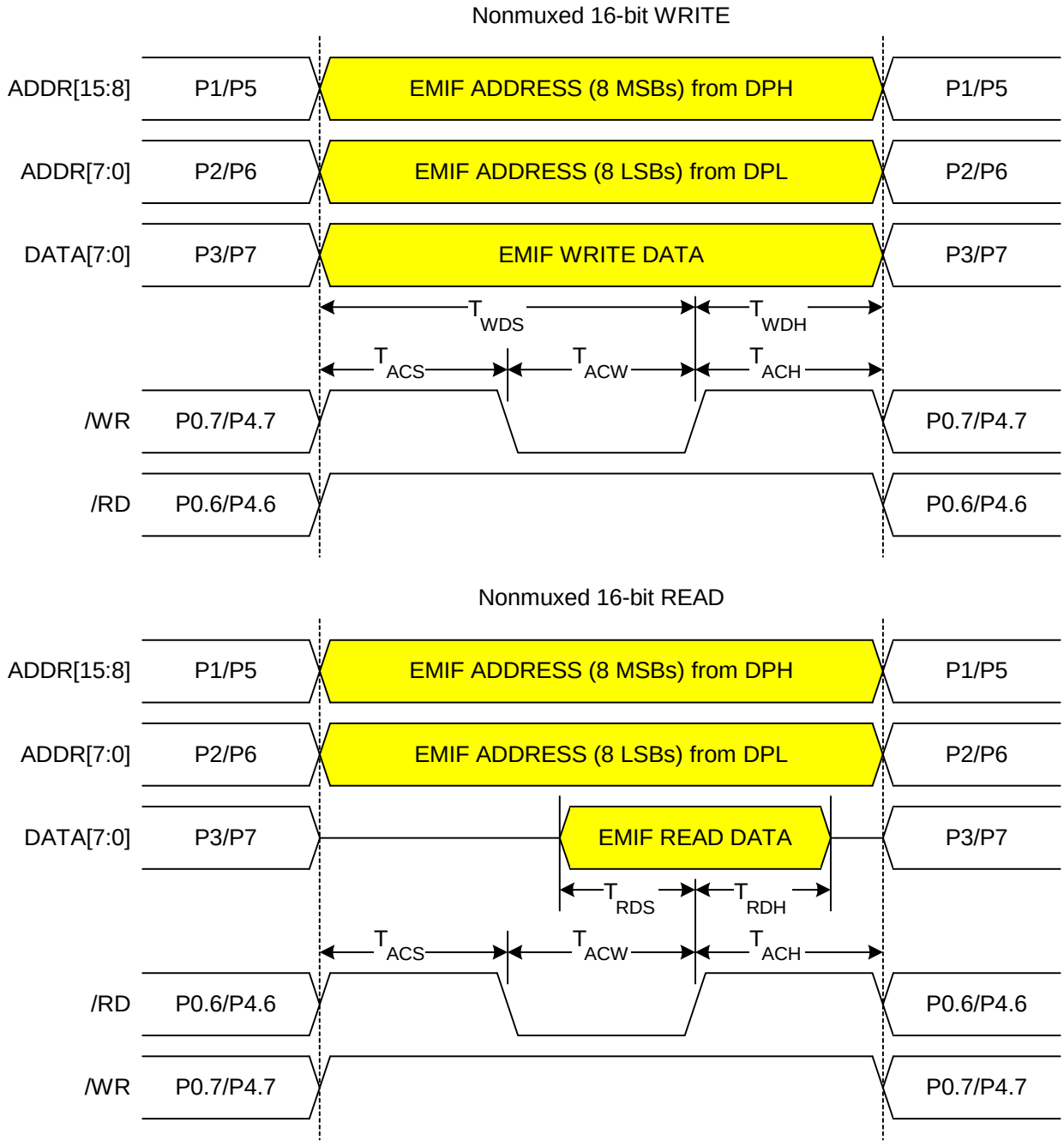
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PRTSEL	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA3

Bits7-6: Unused. Read = 00b. Write = don't care.
Bit5: PRTSEL: EMIF Port Select.
0: EMIF active on P0-P3.
1: EMIF active on P4-P7.
Bit4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).
Bits3-2: EMD1-0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 4k boundary are directed on-chip. Accesses above the 4k boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 4k boundary are directed on-chip. Accesses above the 4k boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.
Bits1-0: EALE1-0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

16.6.1. Non-multiplexed Mode

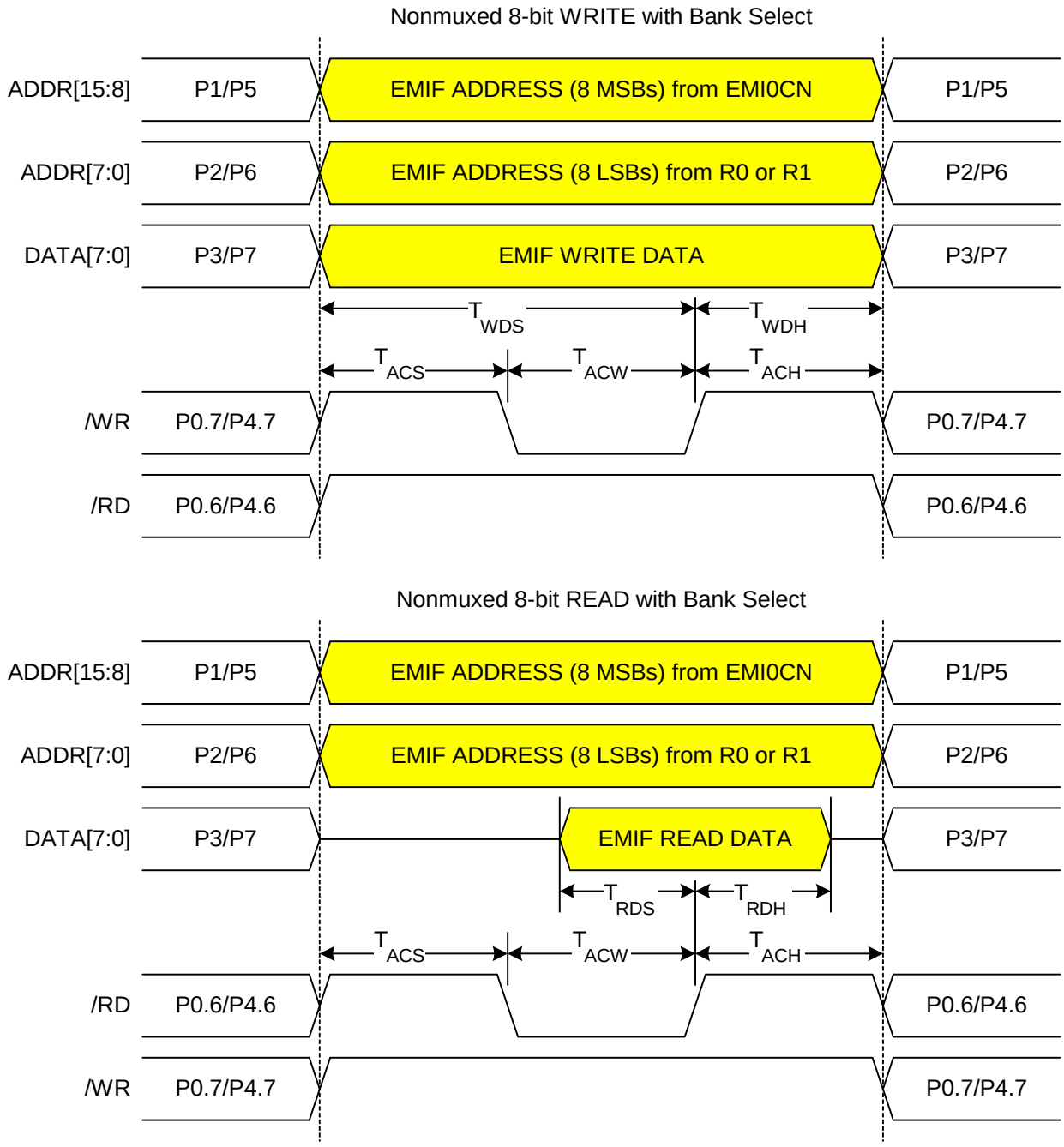
16.6.1.1. 16-bit MOVX: EMI0CF[4:2] = ‘101’, ‘110’, or ‘111’.

Figure 16.7. Non-multiplexed 16-bit MOVX Timing



16.6.1.3. 8-bit MOVX with Bank Select: EMI0CF[4:2] = '110'.

Figure 16.9. Non-multiplexed 8-bit MOVX with Bank Select Timing



17.1. Ports 0 through 3 and the Priority Crossbar Decoder

The Priority Crossbar Decoder, or “Crossbar”, allocates and assigns Port pins on Port 0 through Port 3 to the digital peripherals (UARTs, SMBus, PCA, Timers, etc.) on the device using a priority order. The Port pins are allocated in order starting with P0.0 and continue through P3.7 if necessary. The digital peripherals are assigned Port pins in a priority order which is listed in Figure 17.3, with UART0 having the highest priority and CNVSTR having the lowest priority.

17.1.1. Crossbar Pin Assignment and Allocation

The Crossbar assigns Port pins to a peripheral if the corresponding enable bits of the peripheral are set to a logic 1 in the Crossbar configuration registers XBR0, XBR1, and XBR2, shown in Figure 17.7, Figure 17.8, and Figure 17.9. For example, if the UART0EN bit (XBR0.2) is set to a logic 1, the TX0 and RX0 pins will be mapped to P0.0 and P0.1 respectively. Because UART0 has the highest priority, its pins will always be mapped to P0.0 and P0.1 when UART0EN is set to a logic 1. If a digital peripheral’s enable bits are not set to a logic 1, then its ports are not accessible at the Port pins of the device. Also note that the Crossbar assigns pins to all associated functions when a serial communication peripheral is selected (i.e. SMBus, SPI, UART). It would be impossible, for example, to assign TX0

Figure 17.3. Priority Crossbar Decode Table (EMIFLE = 0; P1MDIN = 0xFF)

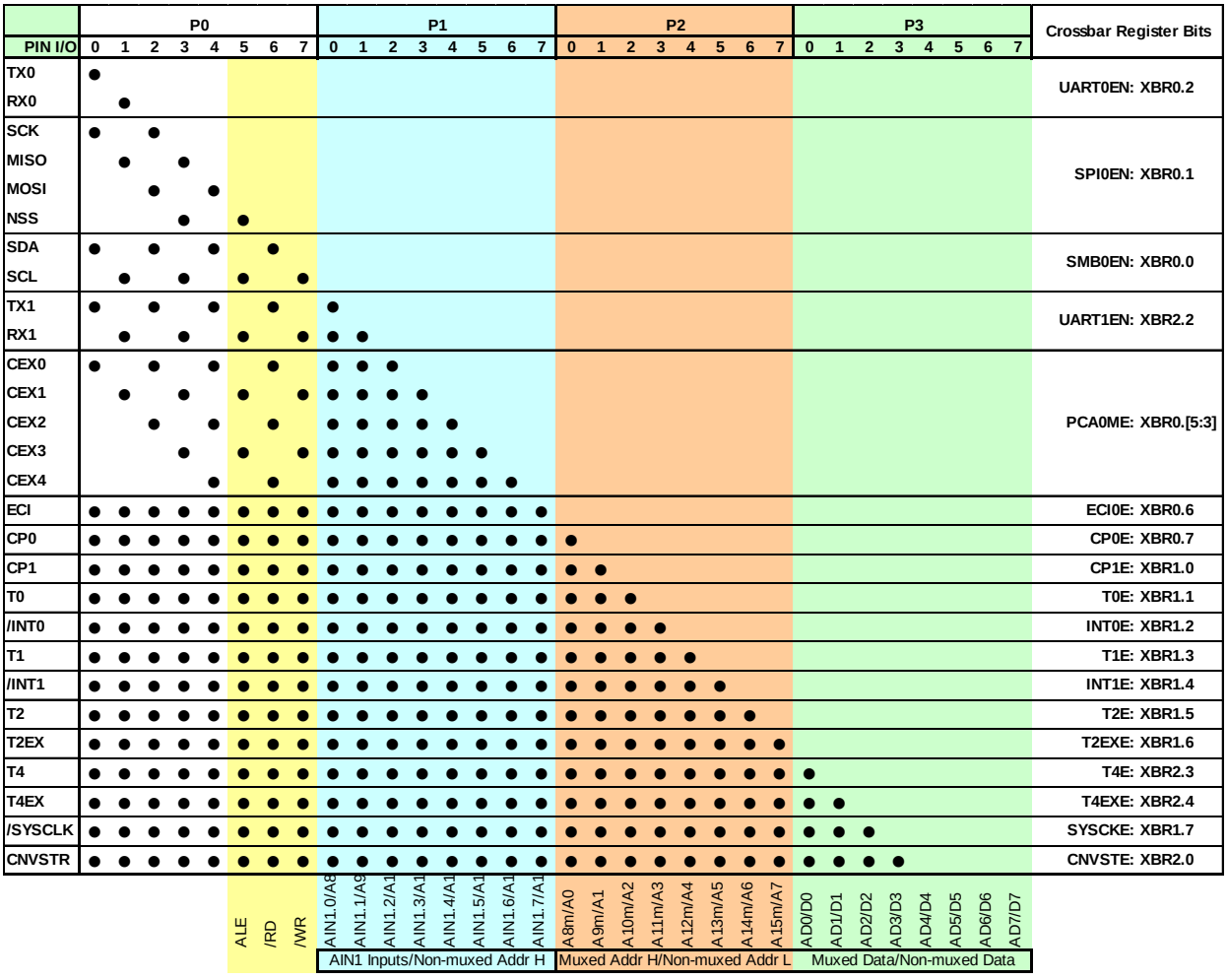


Table 18.1. SMB0STA Status Codes and States

Mode	Status Code	SMBus State	Typical Action
MT/ MR	0x08	START condition transmitted.	Load SMB0DAT with Slave Address + R/W. Clear STA.
	0x10	Repeated START condition transmitted.	Load SMB0DAT with Slave Address + R/W. Clear STA.
Master Transmitter	0x18	Slave Address + W transmitted. ACK received.	Load SMB0DAT with data to be transmitted.
	0x20	Slave Address + W transmitted. NACK received.	Acknowledge poll to retry. Set STO + STA.
	0x28	Data byte transmitted. ACK received.	1) Load SMB0DAT with next byte, OR 2) Set STO, OR 3) Clear STO then set STA for repeated START.
	0x30	Data byte transmitted. NACK received.	1) Retry transfer OR 2) Set STO.
	0x38	Arbitration Lost.	Save current data.
Master Receiver	0x40	Slave Address + R transmitted. ACK received.	If only receiving one byte, clear AA (send NACK after received byte). Wait for received data.
	0x48	Slave Address + R transmitted. NACK received.	Acknowledge poll to retry. Set STO + STA.
	0x50	Data byte received. ACK transmitted.	Read SMB0DAT. Wait for next byte. If next byte is last byte, clear AA.
	0x58	Data byte received. NACK transmitted.	Set STO.

Table 20.2. Oscillator Frequencies for Standard Baud Rates

Oscillator frequency (MHz)	Divide Factor	Timer 1 Load Value*	Resulting Baud Rate (Hz)**
25.0	434	0xE5	57600 (57870)
25.0	868	0xCA	28800
24.576	320	0xEC	76800
24.576	848	0xCB	28800 (28921)
24.0	208	0XF3	115200 (115384)
24.0	833	0xCC	28800 (28846)
23.592	205	0xF3	115200 (113423)
23.592	819	0xCD	28800 (28911)
22.1184	192	0xF4	115200
22.1184	768	0xD0	28800
18.432	160	0xF6	115200
18.432	640	0xD8	28800
16.5888	144	0xF7	115200
16.5888	576	0xDC	28800
14.7456	128	0xF8	115200
14.7456	512	0xE0	28800
12.9024	112	0xF9	115200
12.9024	448	0xE4	28800
11.0592	96	0xFA	115200
11.0592	348	0xE8	28800
9.216	80	0xFB	115200
9.216	320	0xEC	28800
7.3728	64	0xFC	115200
7.3728	256	0xF0	28800
5.5296	48	0xFD	115200
5.5296	192	0xF4	28800
3.6864	32	0xFE	115200
3.6864	128	0xF8	28800
1.8432	16	0xFF	115200
1.8432	64	0xFC	28800

* Assumes SMOD0=1 and T1M=1.

** Numbers in parenthesis show the actual baud rate.

22.1.2. Mode 1: 16-bit Counter/Timer with Auto-Reload

The Counter/Timer with Auto-Reload mode sets the TF2 timer overflow flag when the counter/timer register overflows from 0xFFFF to 0x0000. An interrupt is generated if enabled. On overflow, the 16-bit value held in the two capture registers (RCAP2H, RCAP2L) is automatically loaded into the counter/timer register and the timer is restarted.

Counter/Timer with Auto-Reload mode is selected by clearing the CP/RL2 bit. Setting TR2 to logic 1 enables and starts the timer. Timer 2 can use either the system clock or transitions on an external input pin (T2) as its clock source, as specified by the C/T2 bit. If EXEN2 is set to logic 1, a high-to-low transition on T2EX will also cause a Timer 2 reload, and a Timer 2 interrupt if enabled. If EXEN2 is logic 0, transitions on T2EX will be ignored.

Figure 22.12. T2 Mode 1 Block Diagram

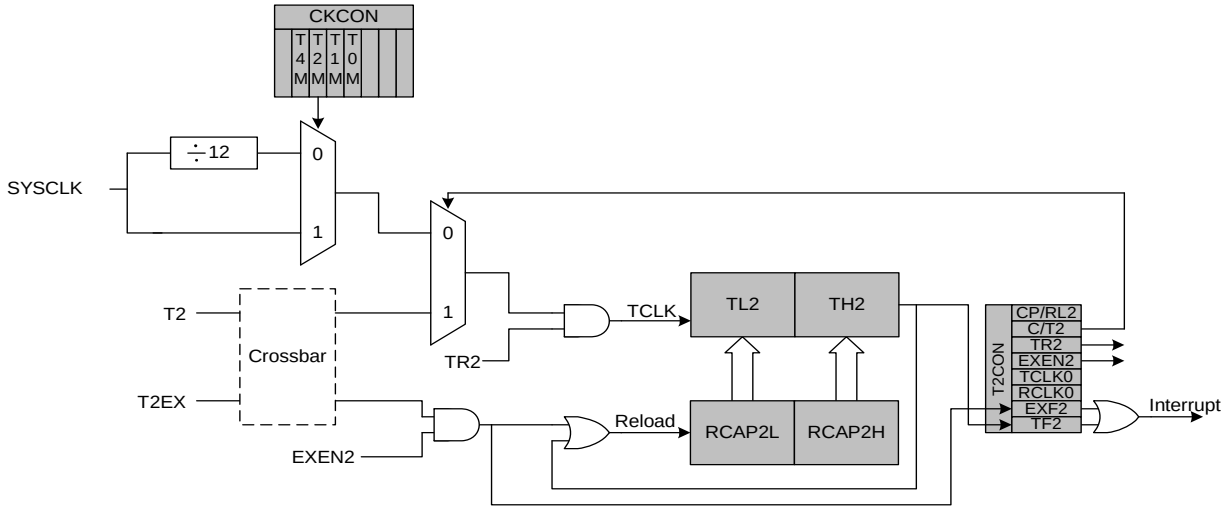


Figure 22.20. TMR3CN: Timer 3 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF3	-	-	-	-	TR3	T3M	T3XCLK	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x91

Bit7: TF3: Timer3 Overflow Flag.
Set by hardware when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 Interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bits6-3: UNUSED. Read = 0000b, Write = don't care.

Bit2: TR3: Timer 3 Run Control.
This bit enables/disables Timer 3.
0: Timer 3 disabled.
1: Timer 3 enabled.

Bit1: T3M: Timer 3 Clock Select.
This bit controls the division of the system clock supplied to Counter/Timer 3.
0: Counter/Timer 3 uses the system clock divided by 12.
1: Counter/Timer 3 uses the system clock.

Bit0: T3XCLK: Timer 3 External Clock Select
This bit selects the external oscillator input divided by 8 as the Timer 3 clock source. When T3XCLK is logic 1, bit T3M (TMR3CN.1) is ignored.
0: Timer 3 clock source defined by bit T3M (TMR3CN.1).
1: Timer 3 clock source is the external oscillator input divided by 8.

Figure 22.21. TMR3RLL: Timer 3 Reload Register Low Byte

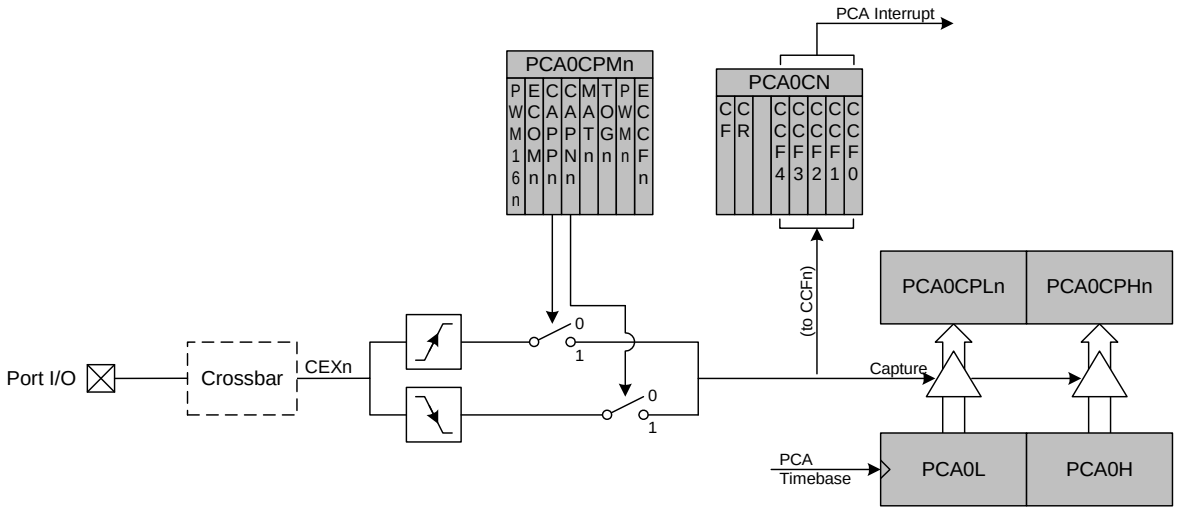
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x92

Bits 7-0: TMR3RLL: Timer 3 Reload Register Low Byte.
Timer 3 is configured as an auto-reload timer. This register holds the low byte of the reload value.

23.2.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes PCA0 to capture the value of the PCA0 counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software.

Figure 23.4. PCA Capture Mode Diagram



Note: The CEXn input signal must remain high or low for at least 2 system clock cycles in order to be valid.

Figure 23.13. PCA0L: PCA0 Counter/Timer Low Byte

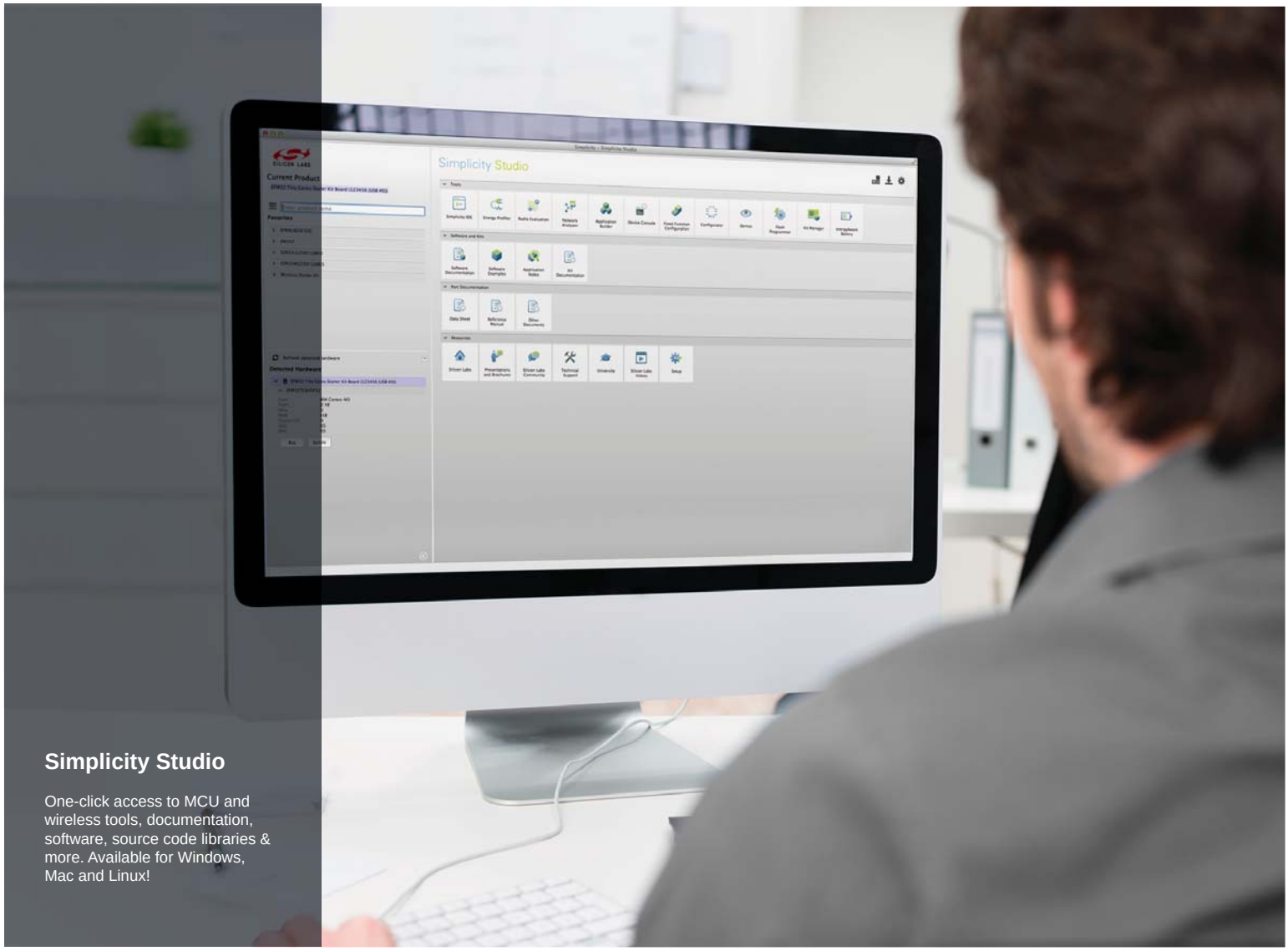
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xE9

Bits 7-0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

Figure 23.14. PCA0H: PCA0 Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF9

Bits 7-0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.



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