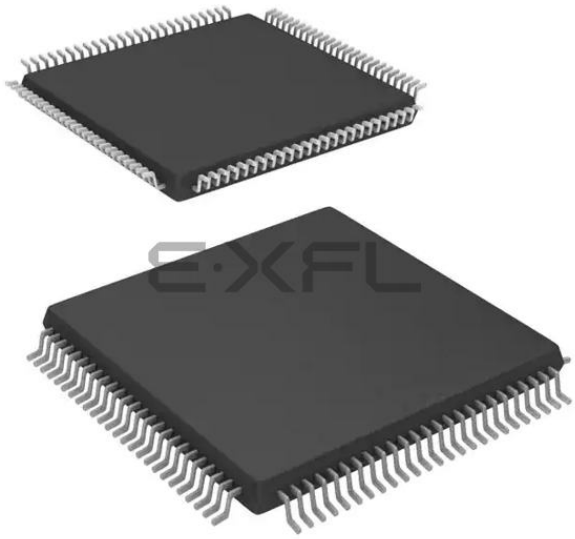

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f022

4. PINOUT AND PACKAGE DEFINITIONS

Table 4.1. Pin Definitions

Name	Pin Numbers		Type	Description
	F020	F021		
	F022	F023		
VDD	37, 64, 90	24, 41, 57		Digital Supply Voltage. Must be tied to +2.7 to +3.6 V.
DGND	38, 63, 89	25, 40, 56		Digital Ground. Must be tied to Ground.
AV+	11, 14	6		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AGND	10, 13	5		Analog Ground. Must be tied to Ground.
TMS	1	58	D In	JTAG Test Mode Select with internal pull-up.
TCK	2	59	D In	JTAG Test Clock with internal pull-up.
TDI	3	60	D In	JTAG Test Data Input with internal pull-up. TDI is latched on the rising edge of TCK.
TDO	4	61	D Out	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
/RST	5	62	D I/O	Device Reset. Open-drain output of internal VDD monitor. Is driven low when VDD is <2.7 V and MONEN is high. An external source can initiate a system reset by driving this pin low.
XTAL1	26	17	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	27	18	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
MONEN	28	19	D In	VDD Monitor Enable. When tied high, this pin enables the internal VDD monitor, which forces a system reset when VDD is < 2.7 V. When tied low, the internal VDD monitor is disabled.
VREF	12	7	A I/O	Bandgap Voltage Reference Output (all devices). DAC Voltage Reference Input (F021/3 only).
VREFA		8	A In	ADC0 and ADC1 Voltage Reference Input.
VREF0	16		A In	ADC0 Voltage Reference Input.
VREF1	17		A In	ADC1 Voltage Reference Input.
VREFD	15		A In	DAC Voltage Reference Input.

7.2.3. Settling Time Requirements

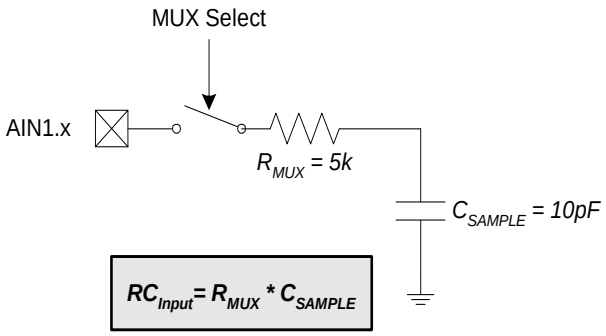
When the ADC1 input configuration is changed (i.e., a different MUX or PGA selection), a minimum settling (or tracking) time is required before an accurate conversion can be performed. This settling time is determined by the ADC1 MUX resistance, the ADC1 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Figure 7.3 shows the equivalent ADC1 input circuit. The required ADC1 settling time for a given settling accuracy (SA) may be approximated by Equation 7.1. Note that in low-power tracking mode, three SAR1 clocks are used for tracking at the start of every conversion. For most applications, these three SAR1 clocks will meet the tracking requirements. See Table 7.1 for absolute minimum settling time requirements.

Equation 7.1. ADC1 Settling Time Requirements

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required tracking time in seconds
R_{TOTAL} is the sum of the ADC1 MUX resistance and any external source resistance.
n is the ADC resolution in bits (8).

Figure 7.3. ADC1 Equivalent Input Circuit



8.1.1. Update Output On-Demand

In its default mode (DAC0CN.[4:3] = ‘00’) the DAC0 output is updated “on-demand” on a write to the high-byte of the DAC0 data register (DAC0H). It’s important to note that writes to DAC0L are held, and have no effect on the DAC0 output until a write to DAC0H takes place. If writing a full 12-bit word to the DAC data registers, the 12-bit data word is written to the low byte (DAC0L) and high byte (DAC0H) data registers. Data is latched into DAC0 after a write to the corresponding DAC0H register, **so the write sequence should be DAC0L followed by DAC0H** if the full 12-bit resolution is required. The DAC can be used in 8-bit mode by initializing DAC0L to the desired value (typically 0x00), and writing data to only DAC0H (also see **Section 8.2** for information on formatting the 12-bit DAC data word within the 16-bit SFR space).

8.1.2. Update Output Based on Timer Overflow

Similar to the ADC operation, in which an ADC conversion can be initiated by a timer overflow independently of the processor, the DAC outputs can use a Timer overflow to schedule an output update event. This feature is useful in systems where the DAC is used to generate a waveform of a defined sampling rate by eliminating the effects of variable interrupt latency and instruction execution on the timing of the DAC output. When the DAC0MD bits (DAC0CN.[4:3]) are set to ‘01’, ‘10’, or ‘11’, writes to both DAC data registers (DAC0L and DAC0H) are held until an associated Timer overflow event (Timer 3, Timer 4, or Timer 2, respectively) occurs, at which time the DAC0H:DAC0L contents are copied to the DAC input latches allowing the DAC output to change to the new value.

8.2. DAC Output Scaling/Justification

In some instances, input data should be shifted prior to a DAC0 write operation to properly justify data within the DAC input registers. This action would typically require one or more load and shift operations, adding software overhead and slowing DAC throughput. To alleviate this problem, the data-formatting feature provides a means for the user to program the orientation of the DAC0 data word within data registers DAC0H and DAC0L. The three DAC0DF bits (DAC0CN.[2:0]) allow the user to specify one of five data word orientations as shown in the DAC0CN register definition.

DAC1 is functionally the same as DAC0 described above. The electrical specifications for both DAC0 and DAC1 are given in Table 8.1.

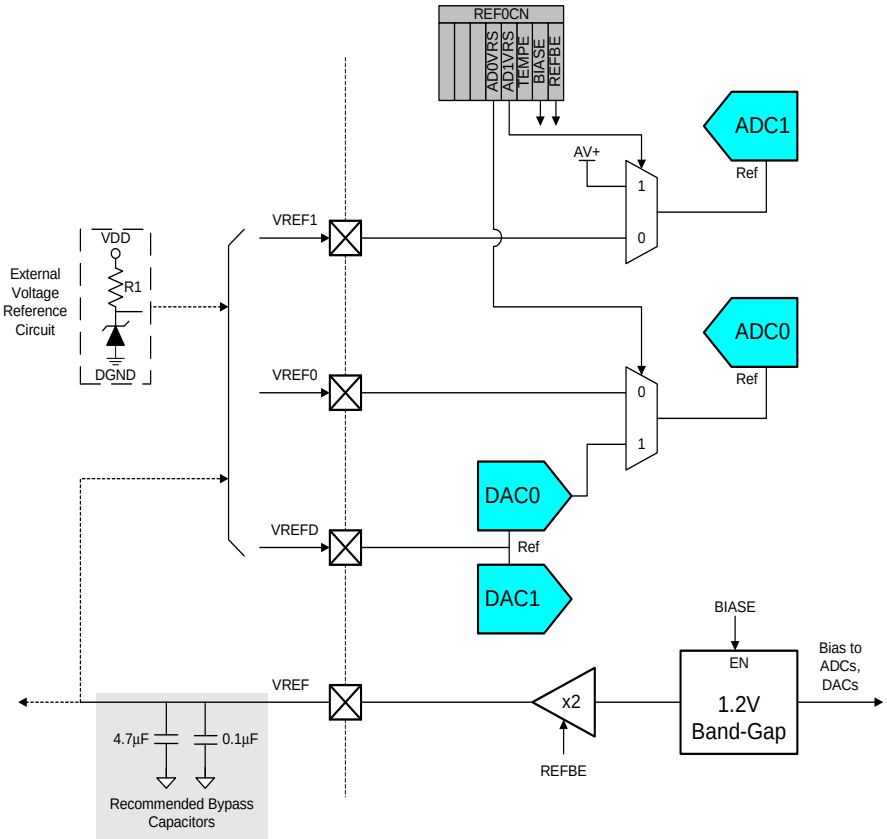
9. VOLTAGE REFERENCE (C8051F020/2)

The voltage reference circuit offers full flexibility in operating the ADC and DAC modules. Three voltage reference input pins allow each ADC and the two DACs to reference an external voltage reference or the on-chip voltage reference output. ADC0 may also reference the DAC0 output internally, and ADC1 may reference the analog power supply voltage, via the VREF multiplexers shown in Figure 9.1.

The internal voltage reference circuit consists of a 1.2 V, 15 ppm/°C (typical) bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the voltage reference input pins shown in Figure 9.1. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to AGND, as shown in Figure 9.1. See Table 9.1 for voltage reference specifications.

The Reference Control Register, REF0CN (defined in Figure 9.2) enables/disables the internal reference generator and selects the reference inputs for ADC0 and ADC1. The BIASE bit in REF0CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 µA (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if either DAC or ADC is used, regardless of whether the voltage reference is derived from the on-chip reference or supplied by an off-chip source. If neither the ADC nor the DAC are being used, both of these bits can be set to logic 0 to conserve power. Bits AD0VRS and AD1VRS select the ADC0 and ADC1 voltage reference sources, respectively. The electrical specifications for the Voltage Reference circuit are given in Table 9.1.

Figure 9.1. Voltage Reference Functional Block Diagram



12. CIP-51 MICROCONTROLLER

The MCU system controller core is the CIP-51 microcontroller. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The MCU family has a superset of all the peripherals included with a standard 8051. Included are five 16-bit counter/timers (see description in **Section 22**), two full-duplex UARTs (see description in **Section 20** and **Section 21**), 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space (see **Section 12.2.6**), and 8/4 byte-wide I/O Ports (see description in **Section 17**). The CIP-51 also includes on-chip debug hardware (see description in **Section 24**), and interfaces directly with the MCUs' analog and digital subsystems providing a complete data acquisition or control-system solution in a single integrated circuit.

The CIP-51 Microcontroller core implements the standard 8051 organization and peripherals as well as additional custom peripherals and functions to extend its capability (see Figure 12.1 for a block diagram). The CIP-51 includes the following features:

- Fully Compatible with MCS-51 Instruction Set
- 25 MIPS Peak Throughput with 25 MHz Clock
- 0 to 25 MHz Clock Frequency
- 256 Bytes of Internal RAM
- 8/4 Byte-Wide I/O Ports
- Extended Interrupt Handler
- Reset Input
- Power Management Modes
- On-chip Debug Logic
- Program and Data Memory Security

Figure 12.1. CIP-51 Block Diagram

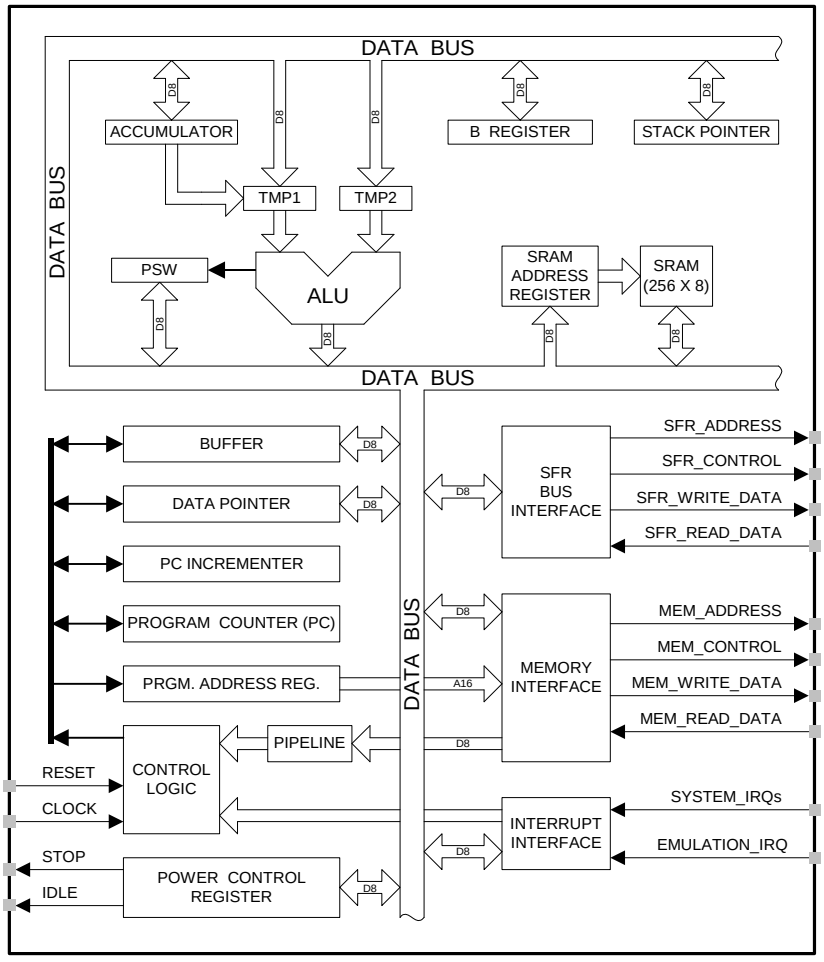


Table 12.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page No.
†P6	0x86	Port 6 Latch	page 181†
†P7	0x96	Port 7 Latch	page 181†
†P74OUT	0xB5	Port 4 through 7 Output Mode	page 179†
PCA0CN	0xD8	PCA Control	page 259
PCA0CPH0	0xFA	PCA Capture 0 High	page 263
PCA0CPH1	0xFB	PCA Capture 1 High	page 263
PCA0CPH2	0xFC	PCA Capture 2 High	page 263
PCA0CPH3	0xFD	PCA Capture 3 High	page 263
PCA0CPH4	0xFE	PCA Capture 4 High	page 263
PCA0CPL0	0xEA	PCA Capture 0 Low	page 263
PCA0CPL1	0xEB	PCA Capture 1 Low	page 263
PCA0CPL2	0xEC	PCA Capture 2 Low	page 263
PCA0CPL3	0xED	PCA Capture 3 Low	page 263
PCA0CPL4	0xEE	PCA Capture 4 Low	page 263
PCA0CPM0	0xDA	PCA Module 0 Mode Register	page 261
PCA0CPM1	0xDB	PCA Module 1 Mode Register	page 261
PCA0CPM2	0xDC	PCA Module 2 Mode Register	page 261
PCA0CPM3	0xDD	PCA Module 3 Mode Register	page 261
PCA0CPM4	0xDE	PCA Module 4 Mode Register	page 261
PCA0H	0xF9	PCA Counter High	page 262
PCA0L	0xE9	PCA Counter Low	page 262
PCA0MD	0xD9	PCA Mode	page 260
PCON	0x87	Power Control	page 126
PSCTL	0x8F	Program Store R/W Control	page 144
PSW	0xD0	Program Status Word	page 114
RCAP2H	0xCB	Timer/Counter 2 Capture High	page 239
RCAP2L	0xCA	Timer/Counter 2 Capture Low	page 239
RCAP4H	0xE5	Timer/Counter 4 Capture High	page 248
RCAP4L	0xE4	Timer/Counter 4 Capture Low	page 248
REF0CN	0xD1	Programmable Voltage Reference Control	page 92†, page 94††
RSTSRC	0xEF	Reset Source Register	page 132
SADDR0	0xA9	UART0 Slave Address	page 214
SADDR1	0xF3	UART1 Slave Address	page 224
SADEN0	0xB9	UART0 Slave Address Enable	page 214
SADEN1	0xAE	UART1 Slave Address Enable	page 224
SBUF0	0x99	UART0 Data Buffer	page 214
SBUF1	0xF2	UART1 Data Buffer	page 224
SCON0	0x98	UART0 Control	page 213
SCON1	0xF1	UART1 Control	page 223
SMB0ADR	0xC3	SMBus Slave Address	page 193
SMB0CN	0xC0	SMBus Control	page 191
SMB0CR	0xCF	SMBus Clock Rate	page 192
SMB0DAT	0xC2	SMBus Data	page 193
SMB0STA	0xC1	SMBus Status	page 194
SP	0x81	Stack Pointer	page 113

Table 12.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	Description	Page No.
SPI0CFG	0x9A	SPI Configuration	page 201
SPI0CKR	0x9D	SPI Clock Rate Control	page 203
SPI0CN	0xF8	SPI Control	page 202
SPI0DAT	0x9B	SPI Data	page 203
T2CON	0xC8	Timer/Counter 2 Control	page 238
T4CON	0xC9	Timer/Counter 4 Control	page 247
TCON	0x88	Timer/Counter Control	page 231
TH0	0x8C	Timer/Counter 0 High	page 233
TH1	0x8D	Timer/Counter 1 High	page 233
TH2	0xCD	Timer/Counter 2 High	page 239
TH4	0xF5	Timer/Counter 4 High	page 248
TL0	0x8A	Timer/Counter 0 Low	page 233
TL1	0x8B	Timer/Counter 1 Low	page 233
TL2	0xCC	Timer/Counter 2 Low	page 239
TL4	0xF4	Timer/Counter 4 Low	page 248
TMOD	0x89	Timer/Counter Mode	page 232
TMR3CN	0x91	Timer 3 Control	page 241
TMR3H	0x95	Timer 3 High	page 242
TMR3L	0x94	Timer 3 Low	page 242
TMR3RLH	0x93	Timer 3 Reload High	page 242
TMR3RLL	0x92	Timer 3 Reload Low	page 241
WDTCN	0xFF	Watchdog Timer Control	page 131
XBR0	0xE1	Port I/O Crossbar Control 0	page 170
XBR1	0xE2	Port I/O Crossbar Control 1	page 171
XBR2	0xE3	Port I/O Crossbar Control 2	page 172
0x97, 0xA2, 0xB3, 0xB4, 0xCE, 0xDF		Reserved	

* Refers to a register in the C8051F020/1 only.
** Refers to a register in the C8051F022/3 only.
† Refers to a register in the C8051F020/2 only.
†† Refers to a register in the C8051F021/3 only.

Table 12.4. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	Always Enabled	Always Highest
External Interrupt 0 (/INT0)	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 (/INT1)	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y		ES0 (IE.4)	PS0 (IP.4)
Timer 2 Overflow (or EXF2)	0x002B	5	TF2 (T2CON.7)	Y		ET2 (IE.5)	PT2 (IP.5)
Serial Peripheral Interface	0x0033	6	SPIF (SPI0CN.7)	Y		ESPI0 (EIE1.0)	PSPI0 (EIP1.0)
SMBus Interface	0x003B	7	SI (SMB0CN.3)	Y		ESMB0 (EIE1.1)	PSMB0 (EIP1.1)
ADC0 Window Comparator	0x0043	8	AD0WINT (ADC0CN.2)	Y		EWADC0 (EIE1.2)	PWADC0 (EIP1.2)
Programmable Counter Array	0x004B	9	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y		EPCA0 (EIE1.3)	PPCA0 (EIP1.3)
Comparator 0 Falling Edge	0x0053	10	CP0FIF (CPT0CN.4)			ECP0F (EIE1.4)	PCP0F (EIP1.4)
Comparator 0 Rising Edge	0x005B	11	CP0RIF (CPT0CN.5)			ECP0R (EIE1.5)	PCP0R (EIP1.5)
Comparator 1 Falling Edge	0x0063	12	CP1FIF (CPT1CN.4)			ECP1F (EIE1.6)	PCP1F (EIP1.6)
Comparator 1 Rising Edge	0x006B	13	CP1RIF (CPT1CN.5)			ECP1R (EIE1.7)	PCP1F (EIP1.7)
Timer 3 Overflow	0x0073	14	TF3 (TMR3CN.7)			ET3 (EIE2.0)	PT3 (EIP2.0)
ADC0 End of Conversion	0x007B	15	AD0INT (ADC0CN.5)	Y		EADC0 (EIE2.1)	PADC0 (EIP2.1)
Timer 4 Overflow	0x0083	16	TF4 (T4CON.7)			ET4 (EIE2.2)	PT4 (EIP2.2)
ADC1 End of Conversion	0x008B	17	AD1INT (ADC1CN.5)			EADC1 (EIE2.3)	PADC1 (EIP2.3)
External Interrupt 6	0x0093	18	IE6 (P3IF.5)			EX6 (EIE2.4)	PX6 (EIP2.4)
External Interrupt 7	0x009B	19	IE7 (P3IF.6)			EX7 (EIE2.5)	PX7 (EIP2.5)
UART1	0x00A3	20	RI1 (SCON1.0) TI1 (SCON1.1)			ES1	PS1
External Crystal OSC Ready	0x00AB	21	XTLVLD (OSCXCN.7)			EXVLD (EIE2.7)	PXVLD (EIP2.7)

Figure 12.13. EIP1: Extended Interrupt Priority 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PCP1R	PCP1F	PCP0R	PCP0F	PPCA0	PWADC0	PSMB0	PSPI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF6

Bit7: PCP1R: Comparator1 (CP1) Rising Interrupt Priority Control.
This bit sets the priority of the CP1 interrupt.
0: CP1 rising interrupt set to low priority level.
1: CP1 rising interrupt set to high priority level.

Bit6: PCP1F: Comparator1 (CP1) Falling Interrupt Priority Control.
This bit sets the priority of the CP1 interrupt.
0: CP1 falling interrupt set to low priority level.
1: CP1 falling interrupt set to high priority level.

Bit5: PCP0R: Comparator0 (CP0) Rising Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: CP0 rising interrupt set to low priority level.
1: CP0 rising interrupt set to high priority level.

Bit4: PCP0F: Comparator0 (CP0) Falling Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: CP0 falling interrupt set to low priority level.
1: CP0 falling interrupt set to high priority level.

Bit3: PPCA0: Programmable Counter Array (PCA0) Interrupt Priority Control.
This bit sets the priority of the PCA0 interrupt.
0: PCA0 interrupt set to low priority level.
1: PCA0 interrupt set to high priority level.

Bit2: PWADC0: ADC0 Window Comparator Interrupt Priority Control.
This bit sets the priority of the ADC0 Window interrupt.
0: ADC0 Window interrupt set to low priority level.
1: ADC0 Window interrupt set to high priority level.

Bit1: PSMB0: System Management Bus (SMBus0) Interrupt Priority Control.
This bit sets the priority of the SMBus0 interrupt.
0: SMBus interrupt set to low priority level.
1: SMBus interrupt set to high priority level.

Bit0: PSPI0: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.

Figure 14.3. OSCXCN: External Oscillator Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xB1

Bit7: XTLVLD: Crystal Oscillator Valid Flag
(Valid only when XOSCMD = 11x.)
0: Crystal Oscillator is unused or not yet stable
1: Crystal Oscillator is running and stable

Bits6-4: XOSCMD2-0: External Oscillator Mode Bits
00x: Off. XTAL1 pin is grounded internally.
010: System Clock from External CMOS Clock on XTAL1 pin.
011: System Clock from External CMOS Clock on XTAL1 pin divided by 2.
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = undefined, Write = don't care

Bits2-0: XFCN2-0: External Oscillator Frequency Control Bits
000-111:

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f < 12 kHz	f < 25 kHz	K Factor = 0.44
001	12 kHz < f ≤ 30 kHz	25 kHz < f ≤ 50 kHz	K Factor = 1.4
010	30 kHz < f ≤ 95 kHz	50 kHz < f ≤ 100 kHz	K Factor = 4.4
011	95 kHz < f ≤ 270 kHz	100 kHz < f ≤ 200 kHz	K Factor = 13
100	270 kHz < f ≤ 720 kHz	200 kHz < f ≤ 400 kHz	K Factor = 38
101	720 kHz < f ≤ 2.2 MHz	400 kHz < f ≤ 800 kHz	K Factor = 100
110	2.2 MHz < f ≤ 6.7 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 420
111	f > 6.7 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1400

CRYSTAL MODE (Circuit from Figure 14.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match the crystal or ceramic resonator frequency.

RC MODE (Circuit from Figure 14.1, Option 2; XOSCMD = 10x)
Choose oscillation frequency range where:
$f = 1.23(10^3) / (R * C)$, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pull-up resistor value in kΩ

C MODE (Circuit from Figure 14.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
f = KF / (C * AV+), where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
AV+ = Analog Power Supply on MCU in volts

16. EXTERNAL DATA MEMORY INTERFACE AND ON-CHIP XRAM

The C8051F020/1/2/3 MCUs include 4k bytes of on-chip RAM mapped into the external data memory space (XRAM), as well as an External Data Memory Interface which can be used to access off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using the MOVX indirect addressing mode using R0 or R1. If the MOVX instruction is used with an 8-bit address operand (such as @R1), then the high byte of the 16-bit address is provided by the External Memory Interface Control Register (EMI0CN, shown in Figure 16.1). Note: the MOVX instruction can also be used for writing to the FLASH memory. See **Section "15. FLASH MEMORY" on page 139** for details. The MOVX instruction accesses XRAM by default. The EMIF can be configured to appear on the lower I/O ports (P0-P3) or the upper I/O ports (P4-P7).

16.1. Accessing XRAM

The XRAM memory space is accessed using the MOVX instruction. The MOVX instruction has two forms, both of which use an indirect addressing method. The first method uses the Data Pointer, DPTR, a 16-bit register which contains the effective address of the XRAM location to be read or written. The second method uses R0 or R1 in combination with the EMI0CN register to generate the effective XRAM address. Examples of both of these methods are given below.

16.1.1. 16-Bit MOVX Example

The 16-bit form of the MOVX instruction accesses the memory location pointed to by the contents of the DPTR register. The following series of instructions reads the value of the byte at address 0x1234 into the accumulator A:

```
MOV    DPTR, #1234h        ; load DPTR with 16-bit address to read (0x1234)
MOVX   A, @DPTR            ; load contents of 0x1234 into accumulator A
```

The above example uses the 16-bit immediate MOV instruction to set the contents of DPTR. Alternately, the DPTR can be accessed through the SFR registers DPH, which contains the upper 8-bits of DPTR, and DPL, which contains the lower 8-bits of DPTR.

16.1.2. 8-Bit MOVX Example

The 8-bit form of the MOVX instruction uses the contents of the EMI0CN SFR to determine the upper 8-bits of the effective address to be accessed and the contents of R0 or R1 to determine the lower 8-bits of the effective address to be accessed. The following series of instructions read the contents of the byte at address 0x1234 into the accumulator A.

```
MOV    EMI0CN, #12h        ; load high byte of address into EMI0CN
MOV    R0, #34h            ; load low byte of address into R0 (or R1)
MOVX   a, @R0              ; load contents of 0x1234 into accumulator A
```

16.5. Memory Mode Selection

The external data memory space can be configured in one of four modes, shown in Figure 16.5, based on the EMIF Mode bits in the EMI0CF register (Figure 16.2). These modes are summarized below. More information about the different modes can be found in **Section " ." on page 152**.

16.5.1. Internal XRAM Only

When EMI0CF.[3:2] are set to '00', all MOVX instructions will target the internal XRAM space on the device. Memory accesses to addresses beyond the populated space will wrap on 4k boundaries. As an example, the addresses 0x1000 and 0x2000 both evaluate to address 0x0000 in on-chip XRAM space.

- 8-bit MOVX operations use the contents of EMI0CN to determine the high-byte of the effective address and R0 or R1 to determine the low-byte of the effective address.
- 16-bit MOVX operations use the contents of the 16-bit DPTR to determine the effective address.

16.5.2. Split Mode without Bank Select

When EMI0CF.[3:2] are set to '01', the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the 4k boundary will access on-chip XRAM space.
- Effective addresses beyond the 4k boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The lower 8-bits of the Address Bus A[7:0] are driven as defined by R0 or R1. However, in the "No Bank Select" mode, an 8-bit MOVX operation will not drive the upper 8-bits A[15:8] of the Address Bus during an off-chip access. This allows the user to manipulate the upper address bits at will by setting the Port state directly. This behavior is in contrast with "Split Mode with Bank Select" described below.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and unlike 8-bit MOVX operations, the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

Figure 16.5. EMIF Operating Modes

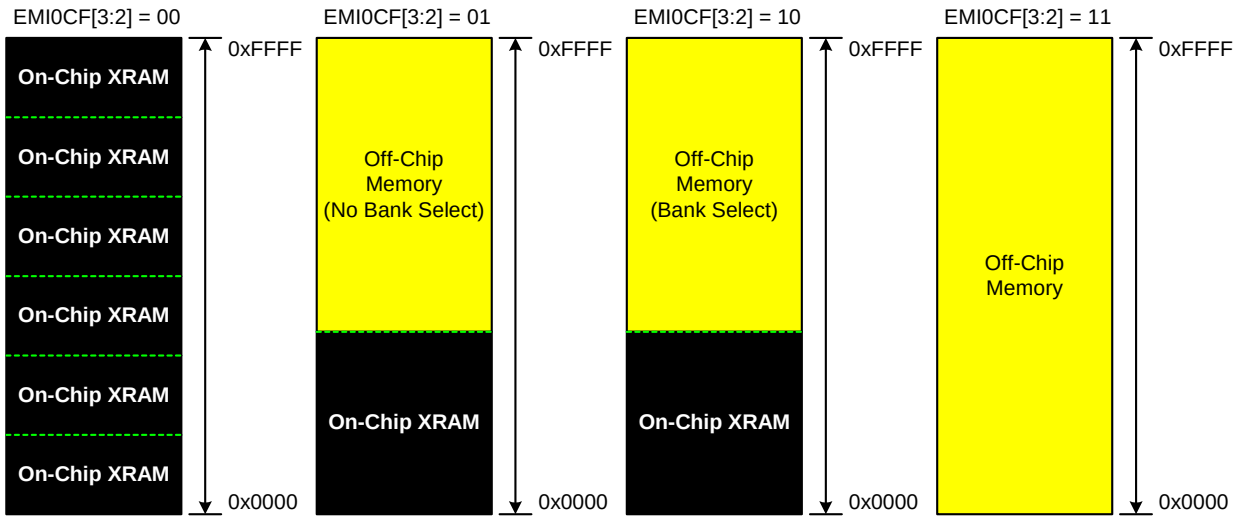


Table 16.1. AC Parameters for External Memory Interface

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
T_{SYSCLK}	System Clock Period	40		ns
T_{ACS}	Address / Control Setup Time	0	$3*T_{SYSCLK}$	ns
T_{ACW}	Address / Control Pulse Width	$1*T_{SYSCLK}$	$16*T_{SYSCLK}$	ns
T_{ACH}	Address / Control Hold Time	0	$3*T_{SYSCLK}$	ns
T_{ALEH}	Address Latch Enable High Time	$1*T_{SYSCLK}$	$4*T_{SYSCLK}$	ns
T_{ALEL}	Address Latch Enable Low Time	$1*T_{SYSCLK}$	$4*T_{SYSCLK}$	ns
T_{WDS}	Write Data Setup Time	$1*T_{SYSCLK}$	$19*T_{SYSCLK}$	ns
T_{WDH}	Write Data Hold Time	0	$3*T_{SYSCLK}$	ns
T_{RDS}	Read Data Setup Time	20		ns
T_{RDH}	Read Data Hold Time	0		ns

17.1. Ports 0 through 3 and the Priority Crossbar Decoder

The Priority Crossbar Decoder, or “Crossbar”, allocates and assigns Port pins on Port 0 through Port 3 to the digital peripherals (UARTs, SMBus, PCA, Timers, etc.) on the device using a priority order. The Port pins are allocated in order starting with P0.0 and continue through P3.7 if necessary. The digital peripherals are assigned Port pins in a priority order which is listed in Figure 17.3, with UART0 having the highest priority and CNVSTR having the lowest priority.

17.1.1. Crossbar Pin Assignment and Allocation

The Crossbar assigns Port pins to a peripheral if the corresponding enable bits of the peripheral are set to a logic 1 in the Crossbar configuration registers XBR0, XBR1, and XBR2, shown in Figure 17.7, Figure 17.8, and Figure 17.9. For example, if the UART0EN bit (XBR0.2) is set to a logic 1, the TX0 and RX0 pins will be mapped to P0.0 and P0.1 respectively. Because UART0 has the highest priority, its pins will always be mapped to P0.0 and P0.1 when UART0EN is set to a logic 1. If a digital peripheral’s enable bits are not set to a logic 1, then its ports are not accessible at the Port pins of the device. Also note that the Crossbar assigns pins to all associated functions when a serial communication peripheral is selected (i.e. SMBus, SPI, UART). It would be impossible, for example, to assign TX0

Figure 17.3. Priority Crossbar Decode Table (EMIFLE = 0; P1MDIN = 0xFF)

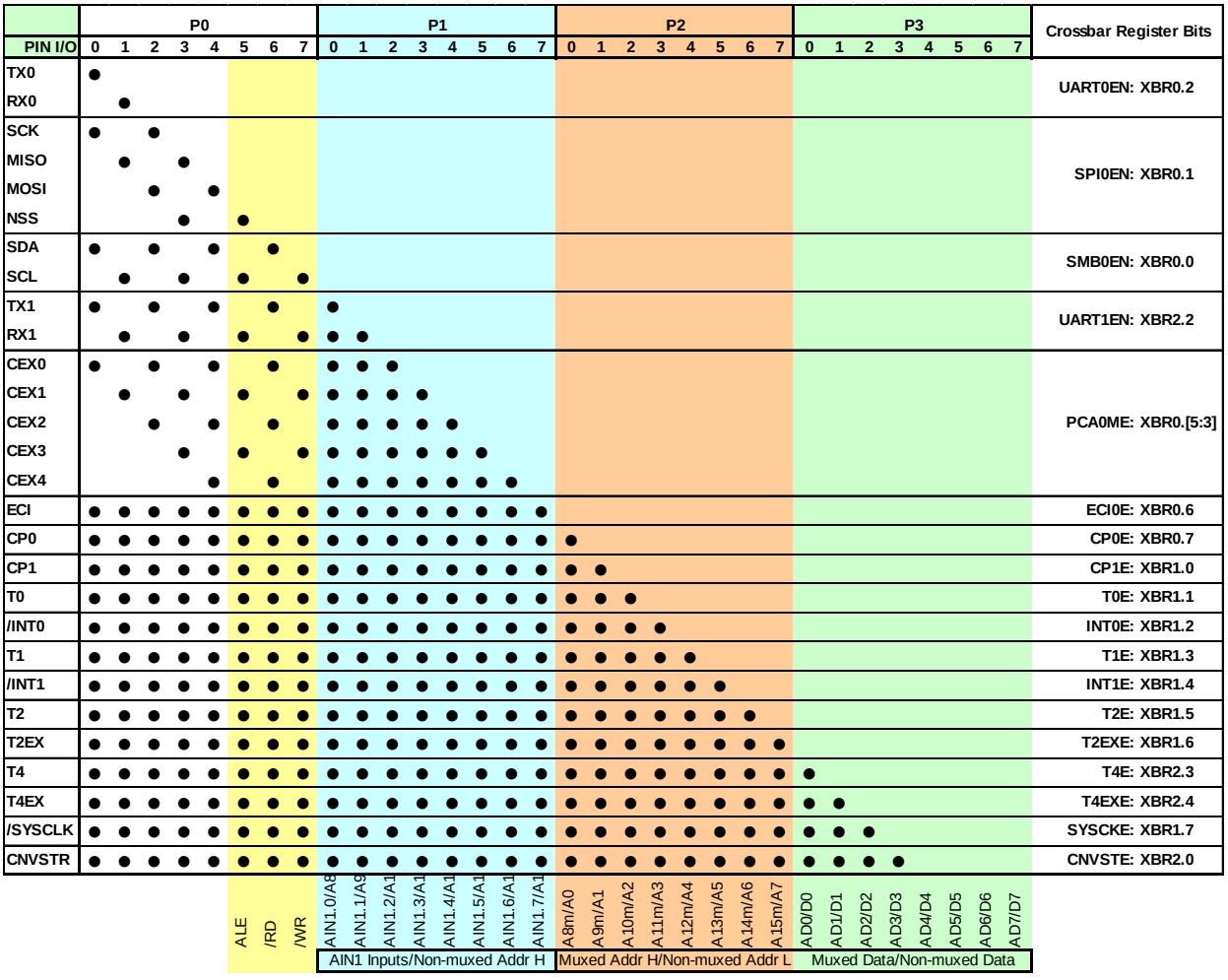


Figure 17.8. XBR1: Port I/O Crossbar Register 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SYSCKE	T2EXE	T2E	INT1E	T1E	INT0E	T0E	CP1E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE2

Bit7: SYSCKE: /SYSCLK Output Enable Bit.
0: /SYSCLK unavailable at Port pin.
1: /SYSCLK routed to Port pin.

Bit6: T2EXE: T2EX Input Enable Bit.
0: T2EX unavailable at Port pin.
1: T2EX routed to Port pin.

Bit5: T2E: T2 Input Enable Bit.
0: T2 unavailable at Port pin.
1: T2 routed to Port pin.

Bit4: INT1E: /INT1 Input Enable Bit.
0: /INT1 unavailable at Port pin.
1: /INT1 routed to Port pin.

Bit3: T1E: T1 Input Enable Bit.
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.

Bit2: INT0E: /INT0 Input Enable Bit.
0: /INT0 unavailable at Port pin.
1: /INT1 routed to Port pin.

Bit1: T0E: T0 Input Enable Bit.
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.

Bit0: CP1E: CP1 Output Enable Bit.
0: CP1 unavailable at Port pin.
1: CP1 routed to Port pin.

Figure 17.14. P1MDOUT: Port1 Output Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA5

Bits7-0: P1MDOUT.[7:0]: Port1 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

Note: SDA, SCL, and RX0 (when UART0 is in Mode 0) and RX1 (when UART1 is in Mode 0) are always configured as Open-Drain when they appear on Port pins.

Figure 17.15. P2: Port2 Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xA0

Bits7-0: P2.[7:0]: Port2 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, XBR2, and XBR3 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P2MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, XBR2, and XBR3 Register settings).
0: P2.n pin is logic low.
1: P2.n pin is logic high.

Note: P2.[7:0] can be driven by the External Data Memory Interface (as Address[15:8] in Multiplexed mode, or as Address[7:0] in Non-multiplexed mode). See **Section "16. EXTERNAL DATA MEMORY INTERFACE AND ON-CHIP XRAM" on page 145** for more information about the External Memory Interface.

Figure 17.16. P2MDOUT: Port2 Output Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA6

Bits7-0: P2MDOUT.[7:0]: Port2 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

Note: SDA, SCL, and RX0 (when UART0 is in Mode 0) and RX1 (when UART1 is in Mode 0) are always configured as Open-Drain when they appear on Port pins.

Figure 17.19. P3IF: Port3 Interrupt Flag Register

R/W	R/W	R	R	R/W	R/W	R/W	R/W	Reset Value
IE7	IE6	-	-	IE7CF	IE6CF	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xAD

Bit7: IE7: External Interrupt 7 Pending Flag
0: No falling edge has been detected on P3.7 since this bit was last cleared.
1: This flag is set by hardware when a falling edge on P3.7 is detected.
Bit6: IE6: External Interrupt 6 Pending Flag
0: No falling edge has been detected on P3.6 since this bit was last cleared.
1: This flag is set by hardware when a falling edge on P3.6 is detected.
Bits5-4: UNUSED. Read = 00b, Write = don't care.
Bit3: IE7CF: External Interrupt 7 Edge Configuration
0: External Interrupt 7 triggered by a falling edge on the IE7 input.
1: External Interrupt 7 triggered by a rising edge on the IE7 input.
Bit2: IE6CF: External Interrupt 6 Edge Configuration
0: External Interrupt 6 triggered by a falling edge on the IE6 input.
1: External Interrupt 6 triggered by a rising edge on the IE6 input.
Bits1-0: UNUSED. Read = 00b, Write = don't care.

17.2. Ports 4 through 7 (C8051F020/2 only)

All Port pins on Ports 4 through 7 can be accessed as General-Purpose I/O (GPIO) pins by reading and writing the associated Port Data registers (See Figure 17.21, Figure 17.22, Figure 17.23, and Figure 17.24), a set of SFRs which are byte-addressable.

A Read of a Port Data register (or Port bit) will always return the logic state present at the pin itself, regardless of whether the Crossbar has allocated the pin for peripheral use or not. An exception to this occurs during the execution of a *read-modify-write* instruction (ANL, ORL, XRL, CPL, INC, DEC, DJNZ, JBC, CLR, SET, and the bitwise MOV operation). During the *read* cycle of the *read-modify-write* instruction, it is the contents of the Port Data register, not the state of the Port pins themselves, which is read.

17.2.1. Configuring Ports which are not Pinned Out

Although P4, P5, P6, and P7 are not brought out to pins on the C8051F021/3 devices, the Port Data registers are still present and can be used by software. Because the digital input paths also remain active, it is recommended that these pins not be left in a 'floating' state in order to avoid unnecessary power dissipation arising from the inputs floating to non-valid logic levels. This condition can be prevented by any of the following:

1. Leave the weak pull-up devices enabled by setting WEAKPUD (XBR2.7) to a logic 0.
2. Configure the output modes of P4, P5, P6, and P7 to "Push-Pull" by writing P74OUT = 0xFF.
3. Force the output states of P4, P5, P6, and P7 to logic 0 by writing zeros to the Port Data registers: P4 = 0x00, P5 = 0x00, P6= 0x00, and P7 = 0x00.

17.2.2. Configuring the Output Modes of the Port Pins

The output mode of each port pin can be configured to be either Open-Drain or Push-Pull. In the Push-Pull configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to be driven to VDD. In the Open-Drain configuration, a logic 0 in the associated bit in the

Figure 20.8. SCON0: UART0 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SM00/FE0	SM10/RXOV0	SM20/TXCOL0	REN0	TB80	RB80	TI0	RI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x98

Bits7-6: The function of these bits is determined by the SSTAT0 bit in register PCON.
If SSTAT0 is logic 1, these bits are UART0 status indicators as described in **Section 20.3**.
If SSTAT0 is logic 0, these bits select the Serial Port Operation Mode as shown below.
SM00-SM10: Serial Port Operation Mode:

SM00	SM10	Mode
0	0	Mode 0: Synchronous Mode
0	1	Mode 1: 8-Bit UART, Variable Baud Rate
1	0	Mode 2: 9-Bit UART, Fixed Baud Rate
1	1	Mode 3: 9-Bit UART, Variable Baud Rate

Bit5: SM20: Multiprocessor Communication Enable.
If SSTAT0 is logic 1, this bit is a UART0 status indicator as described in **Section 20.3**.
If SSTAT0 is logic 0, the function of this bit is dependent on the Serial Port Operation Mode.
Mode 0: No effect.
Mode 1: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI0 will only be activated if stop bit is logic level 1.
Modes 2 and 3: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1 and the received address matches the UART0 address or the broadcast address.

Bit4: REN0: Receive Enable.
This bit enables/disables the UART0 receiver.
0: UART0 reception disabled.
1: UART0 reception enabled.

Bit3: TB80: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in Modes 2 and 3. It is not used in Modes 0 and 1. Set or cleared by software as required.

Bit2: RB80: Ninth Receive Bit.
The bit is assigned the logic level of the ninth bit received in Modes 2 and 3. In Mode 1, if SM20 is logic 0, RB80 is assigned the logic level of the received stop bit. RB8 is not used in Mode 0.

Bit1: TI0: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in Mode 0, or at the beginning of the stop bit in other modes). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software

Bit0: RI0: Receive Interrupt Flag.
Set by hardware when a byte of data has been received by UART0 (as selected by the SM20 bit). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

22.3.3. Mode 2: Baud Rate Generator

Timer 4 can be used as a baud rate generator for UART1 when UART1 is operated in modes 1 or 3 (refer to Section "21.1. UART1 Operational Modes" on page 216 for more information on the UART1 operational modes). In Baud Rate Generator mode, Timer 4 works similarly to the auto-reload mode. On overflow, the 16-bit value held in the two capture registers (RCAP4H, RCAP4L) is automatically loaded into the counter/timer register. However, the TF4 overflow flag is not set and no interrupt is generated. Instead, the overflow event is used as the input to the UART's shift clock. Timer 4 overflows can be selected to generate baud rates for transmit and/or receive independently.

The Baud Rate Generator mode is selected by setting RCLK1 (T4CON.5) and/or TCLK1 (T4CON.4) to '1'. When RCLK1 or TCLK1 is set to logic 1, Timer 4 operates in the auto-reload mode regardless of the state of the CP/RL4 bit. Note that in Baud Rate Generator mode, the Timer 4 timebase is the system clock divided by two. When selected as the UART1 baud clock source, Timer 4 defines the UART1 baud rate as follows:

*Baud Rate = SYSCLK / ((65536 - [RCAP4H, RCAP4L]) * 32)*

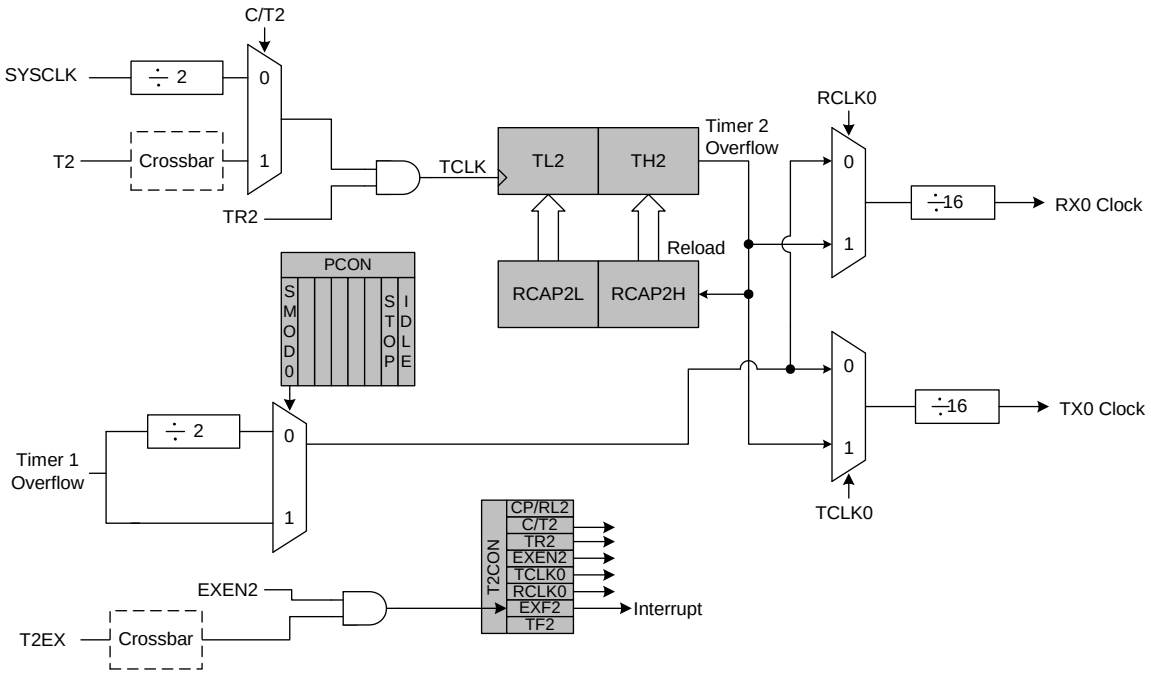
If a different time base is required, setting the C/T4 bit to logic 1 will allow the timebase to be derived from the external input pin T4. In this case, the baud rate for the UART is calculated as:

*Baud Rate = F_{CLK} / ((65536 - [RCAP4H, RCAP4L]) * 16)*

Where F_{CLK} is the frequency of the signal (TCLK) supplied to Timer 4 and [RCAP4H, RCAP4L] is the 16-bit value held in the capture registers.

As explained above, in Baud Rate Generator mode, Timer 4 does not set the TF4 overflow flag and therefore cannot generate an interrupt. However, if EXEN4 is set to logic 1, a high-to-low transition on the T4EX input pin will set the EXF4 flag and a Timer 4 interrupt will occur if enabled. Therefore, the T4EX input may be used as an additional external interrupt source.

Figure 22.27. T4 Mode 2 Block Diagram



24.1. Boundary Scan

The DR in the Boundary Scan path is an 134-bit shift register. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature via the EXTEST and SAMPLE commands.

Table 24.1. Boundary Data Register Bit Definitions

EXTEST provides access to both capture and update actions, while Sample only performs a capture.

Bit	Action	Target
0	Capture	Reset Enable from MCU (C8051F021/3 devices)
	Update	Reset Enable to /RST pin (C8051F021/3 devices)
1	Capture	Reset input from /RST pin (C8051F021/3 devices)
	Update	Reset output to /RST pin (C8051F021/3 devices)
2	Capture	Reset Enable from MCU (C8051F020/2 devices)
	Update	Reset Enable to /RST pin (C8051F020/2 devices)
3	Capture	Reset input from /RST pin (C8051F020/2 devices)
	Update	Reset output to /RST pin (C8051F020/2 devices)
4	Capture	External Clock from XTAL1 pin
	Update	Not used
5	Capture	Weak pullup enable from MCU
	Update	Weak pullup enable to Port Pins
6, 8, 10, 12, 14, 16, 18, 20	Capture	P0.n output enable from MCU (e.g. Bit6=P0.0, Bit8=P0.1, etc.)
	Update	P0.n output enable to pin (e.g. Bit6=P0.0oe, Bit8=P0.1oe, etc.)
7, 9, 11, 13, 15, 17, 19, 21	Capture	P0.n input from pin (e.g. Bit7=P0.0, Bit9=P0.1, etc.)
	Update	P0.n output to pin (e.g. Bit7=P0.0, Bit9=P0.1, etc.)
22, 24, 26, 28, 30, 32, 34, 36	Capture	P1.n output enable from MCU
	Update	P1.n output enable to pin
23, 25, 27, 29, 31, 33, 35, 37	Capture	P1.n input from pin
	Update	P1.n output to pin
38, 40, 42, 44, 46, 48, 50, 52	Capture	P2.n output enable from MCU
	Update	P2.n output enable to pin
39, 41, 43, 45, 47, 49, 51, 53	Capture	P2.n input from pin
	Update	P2.n output to pin
54, 56, 58, 60, 62, 64, 66, 68	Capture	P3.n output enable from MCU
	Update	P3.n output enable to pin
55, 57, 59, 61, 63, 65, 67, 69	Capture	P3.n input from pin
	Update	P3.n output to pin
70, 72, 74, 76, 78, 80, 82, 84	Capture	P4.n output enable from MCU
	Update	P4.n output enable to pin
71, 73, 75, 77, 79, 81, 83, 85	Capture	P4.n input from pin
	Update	P4.n output to pin
86, 88, 90, 92, 94, 96, 98, 100	Capture	P5.n output enable from MCU
	Update	P5.n output enable to pin
87, 89, 91, 93, 95, 97, 99, 101	Capture	P5.n input from pin
	Update	P5.n output to pin
102, 104, 106, 108, 110, 112, 114, 116	Capture	P6.n output enable from MCU
	Update	P6.n output enable to pin
103, 105, 107, 109, 111, 113, 115, 117	Capture	P6.n input from pin
	Update	P6.n output to pin