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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f023-gq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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1.3. JTAG Debug and Boundary Scan

The C8051F020 family has on-chip JTAG boundary scan and debug circuitry that provides *non-intrusive, full speed, in-circuit debugging using the production part installed in the end application*, via the four-pin JTAG interface. The JTAG port is fully compliant to IEEE 1149.1, providing full boundary scan for test and manufacturing purposes.

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, watchpoints, a stack monitor, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F020DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F020/1/2/3 MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to JTAG serial adapter. It also has a target application board with the associated MCU installed, plus the RS-232 and JTAG cables, and wall-mount power supply. The Development Kit requires a Windows 95/98/NT/ME/2000 computer with one available RS-232 serial port. As shown in Figure 1.8, the PC is connected via RS-232 to the Serial Adapter. A six-inch ribbon cable connects the Serial Adapter to the user's application board, picking up the four JTAG pins and VDD and GND. The Serial Adapter takes its power from the application board; it requires roughly 20 mA at 2.7-3.6 V. For applications where there is not sufficient power available from the target system, the provided power supply can be connected directly to the Serial Adapter.

Silicon Labs' debug environment is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use and preserves the performance of the precision analog peripherals.



Figure 1.8. Development/In-System Debug Diagram



5.2.2. **Tracking Modes**

The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked when a conversion is not in progress. When the AD0TM bit is logic 1, ADC0 operates in lowpower track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.3). Tracking can also be disabled (shutdown) when the entire chip is in low power standby or sleep modes. Low-power trackand-hold mode is also useful when AMUX or PGA settings are frequently changed, to ensure that settling time requirements are met (see Section "5.2.3. Settling Time Requirements" on page 46).



Figure 5.3. 12-Bit ADC Track and Conversion Example Timing

B. ADC Timing for Internal Trigger Sources





7. ADC1 (8-BIT ADC)

The ADC1 subsystem for the C8051F020/1/2/3 consists of an 8-channel, configurable analog multiplexer (AMUX1), a programmable gain amplifier (PGA1), and a 500 ksps, 8-bit successive-approximation-register ADC with integrated track-and-hold (see block diagram in Figure 7.1). The AMUX1, PGA1, and Data Conversion Modes, are all configurable under software control via the Special Function Registers shown in Figure 7.1. The ADC1 subsystem (8-bit ADC, track-and-hold and PGA) is enabled only when the AD1EN bit in the ADC1 Control register (ADC1CN) is set to logic 1. The ADC1 subsystem is in low power shutdown when this bit is logic 0. The voltage reference used by ADC1 is selected as described in Section "9. VOLTAGE REFERENCE (C8051F020/2)" on page 91 for C8051F020/2 devices, or Section "10. VOLTAGE REFERENCE (C8051F021/3)" on page 93 for C8051F021/3 devices.



Figure 7.1. ADC1 Functional Block Diagram

7.1. Analog Multiplexer and PGA

Eight ADC1 channels are available for measurement, as selected by the AMX1SL register (see Figure 7.5). The PGA amplifies the ADC1 output signal by an amount determined by the states of the AMP1GN2-0 bits in the ADC1 Configuration register, ADC1CF (Figure 7.4). The PGA can be software-programmed for gains of 0.5, 1, 2, or 4. Gain defaults to 0.5 on reset.

Important Note: AIN1 pins also function as Port 1 I/O pins, and must be configured as analog inputs when used as ADC1 inputs. To configure an AIN1 pin for analog input, set to '0' the corresponding bit in register P1MDIN. Port 1 pins selected as analog inputs are skipped by the Digital I/O Crossbar. See Section "17.1.6. Configuring Port 1 Pins as Analog Inputs (AIN1.[7:0])" on page 165 for more information on configuring the AIN1 pins.





Figure 8.2. DAC0H: DAC0 High Byte Register

Figure 8.3. DAC0L: DAC0 Low Byte Register

-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value				
									00000000				
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:				
									0xD2				
]	Bits7-0:	DAC0 Data Word Least Significant Byte.											





Figure 11.2. Comparator Hysteresis Plot

0. Comparator0 can also be programmed as a reset source; for details, see Section "13.6. Comparator0 Reset" on page 129.

The operation of Comparator1 is identical to that of Comparator0, though Comparator1 may not be configured as a reset source. Comparator1 is controlled by the CPT1CN Register (Figure 11.4). The complete electrical specifications for the Comparators are given in Table 11.1.



Table 11.1.	Comparator	Electrical	Characteristics
	Comparator	Liccuitcai	chiai accertiseres

VDD = 3.0 V, AV+ = 3.0 V, $-40^{\circ}C$ to $+85^{\circ}C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
Response Time 1	CP+ - CP- = 100 mV		4		μs
Response Time 2	CP+ - CP- = 10 mV		12		μs
Common-Mode Rejection Ratio			1.5	4	mV/V
Positive Hysteresis 1	CPnHYP1-0 = 00		0	1	mV
Positive Hysteresis 2	CPnHYP1-0 = 01	2	4.5	7	mV
Positive Hysteresis 3	CPnHYP1-0 = 10	4	9	13	mV
Positive Hysteresis 4	CPnHYP1-0 = 11	10	17	25	mV
Negative Hysteresis 1	CPnHYN1-0 = 00		0	1	mV
Negative Hysteresis 2	CPnHYN1-0 = 01	2	4.5	7	mV
Negative Hysteresis 3	CPnHYN1-0 = 10	4	9	13	mV
Negative Hysteresis 4	CPnHYN1-0 = 11	10	17	25	mV
Inverting or Non-Inverting Input Voltage Range		-0.25		(AV+) + 0.25	V
Input Capacitance			7		pF
Input Bias Current		-5	0.001	+5	nA
Input Offset Voltage		-10		+10	mV
POWER SUPPLY					
Power-up Time	CPnEN from 0 to 1		20		μs
Power Supply Rejection			0.1	1	mV/V
Supply Current	Operating Mode (each comparator) at DC		1.5	10	μA



12.2.7. Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic l. Future product versions may use these bits to implement new features in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the datasheet associated with their corresponding system function.

Figure 12.3. SP: Stack Pointer



Figure 12.4. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value 00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x82
Bits7-0:	DPL: Data Po The DPL regi XRAM and F	inter Low. ster is the lo LASH memo	w byte of the ory.	e 16-bit DPT	R. DPTR is u	used to acces	s indirectly	y addressed

Figure 12.5. DPH: Data Pointer High Byte





R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PXVLD	EP1	PX7	PX6	PADC1	PT4	PADC0	PT3	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								0xF7
Bit7:	PXVLD: Exte	ernal Clock S	ource Valid	(XTLVLD) I	nterrupt Pri	ority Control.		
	This bit sets the	he priority of	the XTLVL	D interrupt.				
	0: XTLVLD in	nterrupt set t	o low priori	ty level.				
	1: XTLVLD in	nterrupt set t	o high priori	ity level.				
Bit6:	EP1: UART1	Interrupt Pri	ority Contro	1.				
	This bit sets the	he priority of	the UART1	interrupt.				
	0: UART1 int	errupt set to	low priority.					
	1: UART1 int	errupt set to	high priority					
Bit5:	PX7: External	I Interrupt 7	Priority Con	trol.				
	This bit sets the	he priority of	the Externa	l Interrupt 7.				
	0: External In	terrupt 7 set	to low prior	ity level.				
	1: External In	terrupt 7 set	to high prior	rity level.				
Bit4:	PX6: External	I Interrupt 6	Priority Con	trol.				
	This bit sets the	he priority of	the Externa	l Interrupt 6.				
	0: External In	terrupt 6 set	to low prior	ity level.				
	1: External In	terrupt 6 set	to high prior	rity level.	_			
Bit3:	PADC1: ADC	C1 End Of Co	onversion In	terrupt Priori	ty Control.			
	This bit sets the	he priority of	the ADC1	End of Conve	ersion interr	upt.		
	0: ADC1 End	of Conversion	on interrupt	set to low pri	ority.			
Dia	1: ADCI End	of Conversi	on interrupt	set to low pri	ority.			
Bit2:	P14: Timer 4	Interrupt Pri	ority Contro	l.				
	This bit sets the	he priority of	the Timer 4	interrupt.				
	0: Timer 4 int	errupt set to	low priority.					
D'(1)	1: Timer 4 int	errupt set to	low priority.		C			
BIUL	PADCO: ADC	End of Con	the ADCO	Frupt Priority	Control.	t		
	1 nis dit sets u	of Conversion	the ADCU	end of Conve	ersion Interr	upt.		
	0: ADC0 End	of Conversion	on interrupt	set to low pri	ionity level.			
BitO	1. ADC0 Ella DT3: Timor 3	Interrupt Pri	ority Contro	set to mgn pr	ionty level.			
BIIU.	This bit sets the	ha priority of	the Timer 3	intorrupts				
	1 ms on sets u	errunt priorit	v determine	d by default :	riority orde	r		
	1. Timer 3 int	errupt set to	high priority	u by uctault j	monty of the			
	1. 1111CI 5 1110	errupt set to	ingii priority	10 / 01.				

Figure 12.14. EIP2: Extended Interrupt Priority 2



Figure 17.6. Crossbar Example:
(EMIFLE = 1; EMIF in Multiplexed Mode; P1MDIN = 0xE3;
XBR0 = 0x05; XBR1 = 0x14; XBR2 = 0x46)

				Р	0							I	P1							P	2				P3					Crossbar Register B			
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	Grosabar Register Dits
тхо	٠																																UARTOEN: XBR0.2
RX0		٠																															CARTOEN. ABROLE
SCK																																	
MISO		٠																															SPINEN: XBP0 1
MOSI																																	OF IDEN. ADIO.1
NSS									٠																								
SDA			٠																														
SCL				•					•					•																			SWIDUEN. ABRU.U
TX1					•																												
RX1		•							٠					•																			UARTIEN: ABR2.2
CEX0					٠												٠																
CEX1		•							•					•	•	•	•	•															
CEX2										•					•	•	•	•	•														PCA0ME: XBR0.[5:3]
CEX3									•					•		•	•	•	•	•													
CEX4										•					•	•	•	•	•	•	•												
ECI	•	•	•	•	•				•	•				•		•	•	•	•	•	•	•											ECI0E: XBR0.6
CP0	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•										CP0E: XBR0.7
CP1	•	•	•	•	•				•	•				•		•	•	•	•	•	•	•	•	•									CP1E: XBR1.0
TO		•	•	•	•				•	•				•		•	•	•	•	•	•	•	•	•	•								T0E: XBR1.1
/INT0	•	•	•	•	•				•	•				•		•	•	•	•	•	•	•	•	•	•	•							INT0E: XBR1.2
T1	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•						T1E: XBR1.3
/INT1	•	•	•	•	•				•	•				٠		•	•	•	•	•	•	•	•	•	•	•	•	•					INT1E: XBR1.4
T2	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•				T2E: XBR1.5
T2EX	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•			T2EXE: XBR1.6
Τ4	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		T4E: XBR2.3
T4EX	•	•	•	•	•				•	•				•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	T4EXE: XBR2.4
/SYSCLK	•	•	•	•	•				•	•				•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	SYSCKE: XBR1.7
CNVSTR	•	•	•	•	•				•	•		_		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	CNVSTE: XBR2.0
		÷		-					A8	A9	Ā	Ā	Ā	A1	A1	A1	-	_	2	3	4	2	9	5	-	-							
							_	~	11.0/	11.1/	1.2/	1.3/	1.4	11.5/	11.6/	11.7/	n/A(n/A	d/m(d/m	d/m	3m/P	fm/⊅	Jm/	0/D0	101	2/D2	3/D3	4/D4	5/D5	8/D6	7/D7	
						ALE	/RD	WF	AIN	AIN	AIN	AIN	AIN	AIN	AIN	AIN	A8r	A 9r	A 10	A11	A 12	A 13	A 14	A 15	AD	AD.	AD:	AD	ΡĎ	ΑŬ	ΡĞ	AD	
									A	N1 I	nput	s/No	n-mi	ixed	Add	lr H	Mu	xed	Addr	H/N	on-m	nuxe	hA h	dr L	M	uxeo	d Da	ta/N	on-m	uxec	Da	ita	



Setting the SMBus0 Free Timer Enable bit (FTE, SMB0CN.1) to logic 1 enables the timer in SMB0CR. When SCL goes high, the timer in SMB0CR counts up. A timer overflow indicates a free bus timeout: if SMBus0 is waiting to generate a START, it will do so after this timeout. The bus free period should be less than 50 μ s (see Figure 18.9, SMBus0 Clock Rate Register).

When the TOE bit in SMB0CN is set to logic 1, Timer 3 is used to detect SCL low timeouts. If Timer 3 is enabled (see Section "22.2. Timer 3" on page 240), Timer 3 is forced to reload when SCL is high, and forced to count when SCL is low. With Timer 3 enabled and configured to overflow after 25 ms (and TOE set), a Timer 3 overflow indicates a SCL low timeout; the Timer 3 interrupt service routine can then be used to reset SMBus0 communication in the event of an SCL low timeout.



18.4.2. Clock Rate Register

		•				-						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value				
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xCF				
Bits7-0:	 SMB0CR.[7:0]: SMBus0 Clock Rate Preset The SMB0CR Clock Rate register controls the frequency of the serial clock SCL in master 8-bit word stored in the SMB0CR Register preloads a dedicated 8-bit timer. The timer con- when it rolls over to 0x00, the SCL logic state toggles. The SMB0CR setting should be bounded by the following equation , where <i>SMB0CR</i> is th 8-bit value in register SMB0CR, and <i>SYSCLK</i> is the system clock frequency in Hz: 											
	$SMB0CR < ((288 - 0.85 \cdot SYSCLK) / 1.125)$											
	The resulting	SCL signal	high and low	times are gi	ven by the f	ollowing equa	ations:					
		T_{LO}	_W = (256	– SMB0C	CR)/SYSC	CLK						
		T _{HIGH}	$\cong (258 - S)$	MB0CR)/	SYSCLK	(+ 625 <i>ns</i>						
	Using the samequation:	is given in	the following									
		T _{BFT}	$a \cong 10 \times \frac{(2)}{2}$	56 – SMB SYSC	$\frac{0CR)+1}{LK}$							

Figure 18.9. SMB0CR: SMBus0 Clock Rate Register



18.4.5. Status Register

The SMB0STA Status register holds an 8-bit status code indicating the current state of the SMBus0 interface. There are 28 possible SMBus0 states, each with a corresponding unique status code. The five most significant bits of the status code vary while the three least-significant bits of a valid status code are fixed at zero when SI = '1'. Therefore, all possible status codes are multiples of eight. This facilitates the use of status codes in software as an index used to branch to appropriate service routines (allowing 8 bytes of code to service the state or jump to a more extensive service routine).

For the purposes of user software, the contents of the SMB0STA register is only defined when the SI flag is logic 1. Software should never write to the SMB0STA register; doing so will yield indeterminate results. The 28 SMBus0 states, along with their corresponding status codes, are given in Table 1.1.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit0	SFR Address:	
								0xC1
Bits7-3:	STA7-STA3: These bits cor responds to a (SMB0CN.3) Writing to the	SMBus0 Sta ntain the SM single SMBu is set to logi SMB0STA	tus Code. Bus0 Status Is state. A va c 1. The con register at ar	Code. There alid status co tent of SMB ny time will y	are 28 possil de is present 0STA is not /ield indetern	ble status coo in SMB0ST defined when ninate result	des; each sta A when the n the SI flag s.	atus code cor- SI flag is logic 0.
Bits2-0:	STA2-STA0: ' is logic 1.	The three lea	st significan	t bits of SME	30STA are al	ways read as	logic 0 whe	en the SI flag

Figure 18.12. SMB0STA: SMBus0 Status Register



19.4. SPI Special Function Registers

SPI0 is accessed and controlled through four special function registers in the system controller: SPI0CN Control Register, SPI0DAT Data Register, SPI0CFG Configuration Register, and SPI0CKR Clock Rate Register. The four special function registers related to the operation of the SPI0 Bus are described in the following section.

Figure 19	9.5. SPIOC	FG: SPI0	Configuration	Register

R/W	R/W	R	R	R	R/W	R/W	R/W	Reset Valu		
СКРНА	CKPOL	BC2	BC1	BC0	SPIFRS2	SPIFRS1	SPIFRS0	0000011		
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Addre		
								0x9A		
D	CUZDU A CD									
Bit/:	: CKPHA: SPI0 Clock Phase. This hit controls the SPI0 clock phase									
	I his bit conti	ols the SPI	clock phase	maniad						
	1: Data samp	led on more	edge of SCK	Period.						
Rit6.										
Dito.	This bit cont	ols the SPI	anty.) clock polari	tv						
	0. SCK line l	ow in idle s	tate	cy.						
	1: SCK line h	nigh in idle s	state.							
Bits5-3:	BC2-BC0: SI	PI0 Bit Cou	nt.							
0.	Indicates whi	ich of the un	to 8 bits of t	he SPI0 word	have been t	ransmitted.				
		I								
		BC2-BC0		BIT Transm	itted					
	0	0	0	Bit 0 (LSI	3)					
	0	0	1	Bit 1						
	0	1	0	Bit 2						
	0	1	1	Bit 3						
	1	0	0	Bit 4						
	1	0	1	Bit 5						
	1	1	0	Bit 6						
	1	1	1	Bit 7 (MS	B)					
Rits2-0.	SPIFR S2-SP	IFRSA: SPI) Frame Size							
2102 01	These three b	oits determin	e the number	of bits to shi	ft in/out of t	he SPI0 shif	t register du	ring a data		
	transfer in ma	aster mode.	They are igno	ored in slave	node.		0	0		
		SPIFRS		Bits Shifte	d					
		0	0	1						
	0									
	0	0	1	2						
	0 0 0	0	1 0	$\frac{2}{3}$						
	0 0 0 0	0 1 1	1 0 1							
	0 0 0 1	0 1 1 0	1 0 1 0							
	0 0 0 1 1	0 1 1 0 0	1 0 1 0 1	2 3 4 5 6						
	0 0 0 1 1 1 1	0 1 1 0 0 1	1 0 1 0 1 0	$ \begin{array}{r} 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \end{array} $						



21.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted from the TX1 pin and received at the RX1 pin. On receive, the eight data bits are stored in SBUF1 and the stop bit goes into RB81 (SCON1.2).

Data transmission begins when an instruction writes a data byte to the SBUF1 register. The TI1 Transmit Interrupt Flag (SCON1.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN1 Receive Enable bit (SCON1.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF1 receive register if the following conditions are met: RI1 must be logic 0, and if SM21 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data are stored in SBUF1, the stop bit is stored in RB81 and the RI1 flag is set. If these conditions are not met, SBUF1 and RB81 will not be loaded and the RI1 flag will not be set. An interrupt will occur if enabled when either TI1 or RI1 is set.



Figure 21.4. UART1 Mode 1 Timing Diagram

The baud rate generated in Mode 1 is a function of timer overflow, shown in Equation 21.1 and Equation 21.2. UART1 can use Timer 1 operating in *8-Bit Auto-Reload Mode*, or Timer 4 operating in *Baud Rate Generator Mode* to generate the baud rate (note that the TX and RX clocks are selected separately). On each timer overflow event (a roll-over from all ones - (0xFF for Timer 1, 0xFFFF for Timer 4) - to zero) a clock is sent to the baud rate logic.

Timer 4 is selected as TX and/or RX baud clock source by setting the TCLK1 (T4CON.4) and/or RCLK1 (T4CON.5) bits, respectively (see Section "22. TIMERS" on page 225 for complete timer configuration details). When either TCLK1 or RCLK1 is set to logic 1, Timer 4 is forced into *Baud Rate Generator Mode*, with SYSCLK / 2 as its clock source. If TCLK1 and/or RCLK1 is logic 0, Timer 1 acts as the baud clock source for the TX and/or RX circuits, respectively.

The Mode 1 baud rate equations are shown below, where T1M is the Timer 1 Clock Select bit (register CKCON), TH1 is the 8-bit reload register for Timer 1, SMOD1 is the UART1 baud rate doubler (register PCON), and [RCAP4H, RCAP4L] is the 16-bit reload register for Timer 4.

Equation 21.1. Mode 1 Baud Rate using Timer 1

$$BaudRate = \left(\frac{2^{SMOD1}}{32}\right) \times \left(\frac{SYSCLK \times 12^{(T1M-1)}}{(256 - TH1)}\right)$$

Equation 21.2. Mode 1 Baud Rate using Timer 4 $BaudRate = \frac{SYSCLK}{[32 \times (65536 - [RCAP4H, RCAP4L])]}$



23.2.4. Frequency Output Mode

Frequency Output Mode produces a programmable-frequency square wave on the module's associated CEXn pin. The capture/compare module high byte holds the number of PCA clocks to count before the output is toggled. The frequency of the square wave is then defined by Equation 23.1.

Equation 23.1. Square Wave Frequency Output

$$F_{CEXn} = \frac{F_{PCA}}{2 \times PCA0CPHn}$$

Note: A value of 0x00 in the PCA0CPHn register is equal to 256 for this equation.

Where F_{PCA} is the frequency of the clock selected by the CPS2-0 bits in the PCA mode register, PCA0MD. The lower byte of the capture/compare module is compared to the PCA0 counter low byte; on a match, CEXn is toggled and the offset held in the high byte is added to the matched value in PCA0CPLn. Frequency Output Mode is enabled by setting the ECOMn, TOGn, and PWMn bits in the PCA0CPMn register.



Figure 23.7. PCA Frequency Output Mode



23.3. Register Descriptions for PCA0

Following are detailed descriptions of the special function registers related to the operation of PCA0.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
						(bit addressable	e) 0xD8
Bit7:	CF: PCA Cou	nter/Timer (Overflow Fla	ıg.				
	Set by hardwa	are when the	PCA0 Coun	ter/Timer ov	erflows from	n 0xFFFF to	0x0000. W	hen the
	Counter/Time	r Overflow (CF) interrup	ot is enabled,	setting this b	oit causes the	CPU to ve	ctor to the CF
	interrupt servi	ice routine. 7	This bit is no	t automatical	ly cleared by	y hardware a	nd must be	cleared by
DLA	software. See	"Important]	Note About	the PCA0CN	Register" of	n page 251.		
Bit6:	CR: PCA0 Co	ounter/Timer	Run Contro	l.				
	I his bit enabl	es/disables t	he PCA0 Co	unter/Timer.				
	1: PCA0 Cou	nter/Timer a	isabled.					
Rit5.	UNUSED Re	ad = 0b Wr	ite – don't ca	are				
Bit4:	CCF4: PCA0	Module 4 C	apture/Com	are Flag.				
2	This bit is set	by hardware	when a mat	ch or capture	e occurs. Wh	en the CCF	interrupt is	enabled, set-
	ting this bit ca	uses the CP	U to vector t	o the CCF in	terrupt servi	ce routine. T	his bit is no	ot automati-
	cally cleared l	by hardware	and must be	cleared by s	oftware.			
Bit3:	CCF3: PCA0	Module 3 C	apture/Comp	oare Flag.				
	This bit is set	by hardware	when a mat	ch or capture	e occurs. Wh	en the CCF	interrupt is	enabled, set-
	ting this bit ca	uses the CP	U to vector t	o the CCF in	terrupt servi	ce routine. T	his bit is no	ot automati-
	cally cleared l	by hardware	and must be	cleared by s	oftware.			
Bit2:	CCF2: PCA0	Module 2 C	apture/Comp	bare Flag.	****1			
	This bit is set	by hardware	when a mat	ch or capture	e occurs. Wh	en the CCF	Interrupt 1s	enabled, set-
	and the second large d	uses the CP	ond must be	o the CCF in	terrupt servi	ce routine. I	nis dit is no	ot automati-
Rit1.	$CCF1 \cdot PCA0$	Module 1 C	and must be	Sore Flag	ontware.			
DITI.	This bit is set	by hardware	when a mat	ch or capture	occurs Wh	en the CCF i	interrunt is	enabled set-
	ting this bit ca	uses the CP	U to vector t	o the CCF in	terrupt servi	ce routine. T	his bit is no	ot automati-
	cally cleared l	by hardware	and must be	cleared by s	oftware.	••••••		<i>i</i> uutomuu
Bit0:	CCF0: PCA0	Module 0 C	apture/Comp	oare Flag.				
	This bit is set	by hardware	when a mat	ch or capture	e occurs. Wh	en the CCF i	interrupt is	enabled, set-
	ting this bit ca	uses the CP	U to vector t	o the CCF in	terrupt servi	ce routine. T	his bit is no	ot automati-
	cally cleared l	by hardware	and must be	cleared by s	oftware.			

Figure 23.10. PCA0CN: PCA Control Register



Notes



Figure 24.4. FLASHADR: JTAG Flash Address Register

	1		[[[[1					[1	Reset Value
D:415														D:40	0X0000
ы115														ыш	
This register holds the address for all JTAG Flash read, write, and erase operations. This register autoincrements after each read or write, regardless of whether the operation succeeded or failed.															
Bits15	Bits15-0: Flash Operation 16-bit Address.														

Figure 24.5. FLASHDAT: JTAG Flash Data Register

				•		•	•		Reset Value		
									0000000000		
Bit9								Bit0	_		
This regis	ster is used to read	d or write da	ta to the	Flash men	nory acros	ss the JTA	G interfa	ce.			
D : 0 0											
Bits9-2:	DATA7-0: Flash Data Byte.										
Bit1:	FAIL: Flash Fai	il Bit.									
	0: Previous Flas	sh memory o	operation	was succe	essful.						
	1: Previous Flas	sh memory of	operation	failed. Us	ually indi	cates the a	associated	1 memory	location		
	was locked.	5	1		5			5			
Bit0:	BUSY: Flash B	usv Bit.									
Bito.	0. Flash interfac	ce logic is n	ot husy								
	1: Flash interfac	ce logic is n	rocessing	a request	Reads or	writes w	aile BUSY	V = 1 will	l not		
		le logic is p	locessing	a request.	Reaus of	writes wi	ine bus	I = I WII	l liot		
	initiate another	operation									

