Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	-
Core Processor	-
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	-
Number of I/O	-
Voltage - Supply	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mm912i637am2ep

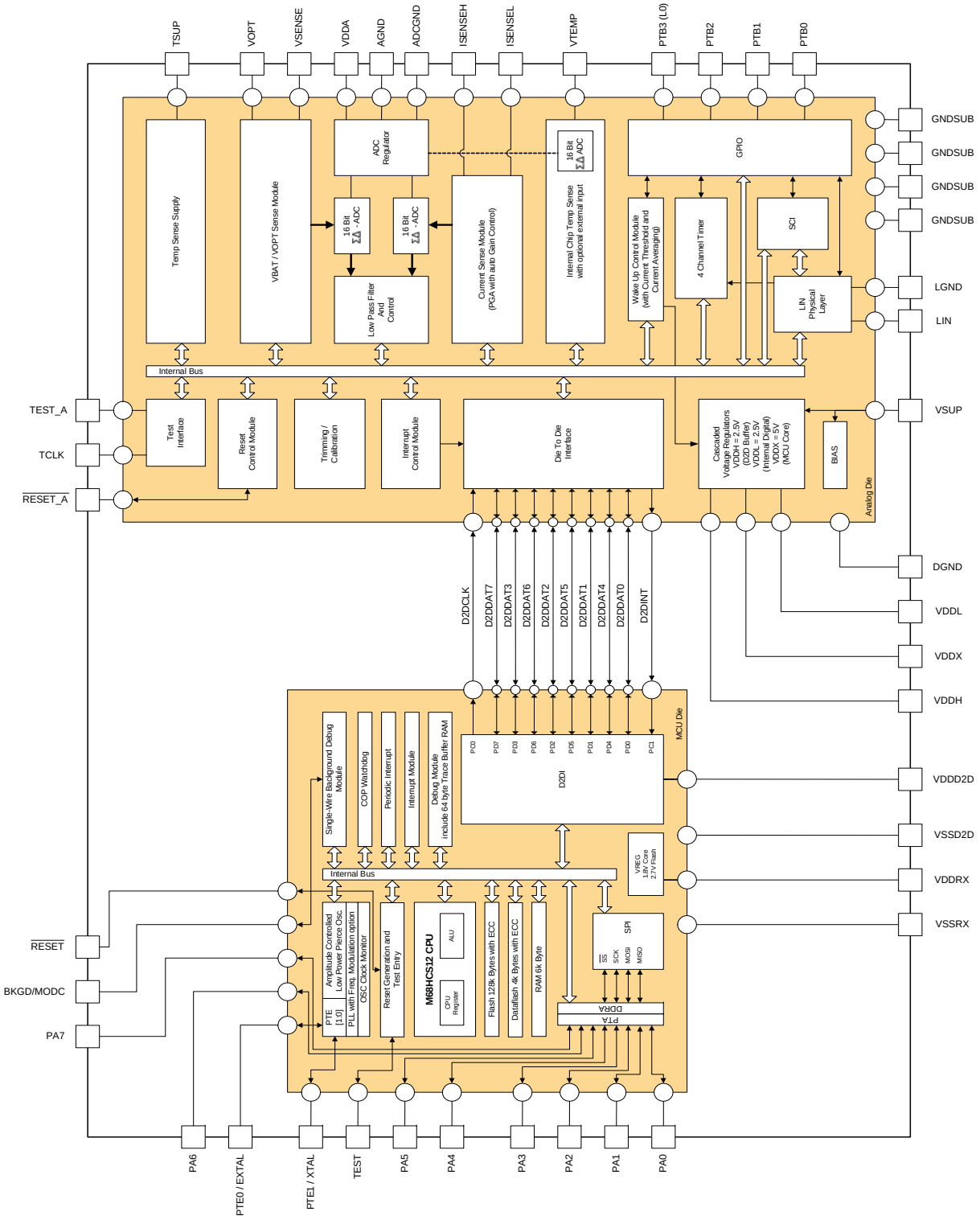


Figure 2. Sample Block Diagram

Table 18. Static Electrical Characteristics - Voltage Regulator Outputs

Ratings	Symbol	Min	Typ	Max	Unit
Analog Voltage Regulator - VDDA[13]					
Output Voltage 1.0 mA ≤ I_{VDDA} ≤ 1.5 mA	V_{DDA}	2.25	2.5	2.75	V
Output Current Limitation	I_{VDDA}			10	mA
Low Power Digital Voltage Regulator - VDDL[13]					
Output Voltage	V_{DDL}	2.25	2.5	2.75	V
High Power Digital Voltage Regulator - VDDH[14]					
Output Voltage 1.0 mA ≤ I_{VDDH} ≤ 30 mA	V_{DDH}	2.4	2.5	2.75	V
Output Current Limitation	I_{VDDH}			65	mA
5.0 V Voltage Regulator - VDDX[14]					
Output Voltage 1.0 mA ≤ I_{VDDX} ≤ 30 mA	V_{DDX}	3.15	5.0	5.9	V
Output Current Limitation	I_{VDDX}	45	60	80	mA

Notes

13.No additional current must be taken from those outputs.

14.The specified current ranges does include the current for the MCU die. No external loads recommended.

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0			mA
Input Leakage Current at the Receiver incl. Pull-up Resistor R_{SLAVE}; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; $V_{BUS} \geq V_{BAT}$	$I_{BUS\_PAS\_REC}$			20	µA
Input Leakage Current; GND Disconnected; GND_{DEVICE} = V_{SUP}; 0 < V_{BUS} < 18 V; V_{BAT} = 12 V	$I_{BUS\_NO\_GND}$	-1.0		1.0	mA
Input Leakage Current; V_{BAT} disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V	$I_{BUS\_NO\_BAT}$			100	µA
Receiver Input Voltage; Receiver Dominant State	V_{BUSDOM}			0.4	V_{SUP}
Receiver Input Voltage; Receiver Recessive State	V_{BUSREC}	0.6			V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{BUS_HYS}			0.175	V_{SUP}
Voltage Drop at the serial Diode	D_{SER_INT}	0.3	0.7	1.0	V
LIN Pull-up Resistor	R_{SLAVE}	20	30	60	kOhm
Low Level Output Voltage, I_{BUS}=40 mA	V_{DOM}			0.3	V_{SUP}
High Level Output Voltage, I_{BUS}=-10 µA, R_L=33 kOhm	V_{REC}	VSUP-1			V
J2602 Detection Deassert Threshold for VSUP level	V_{J2602H}	5.9	6.3	6.7	V
J2602 Detection Assert Threshold for VSUP level	V_{J2602L}	5.8	6.2	6.6	V
J2602 Detection Hysteresis	$V_{J2602HYS}$	70	190	250	mV
BUS Wake-up Threshold	V_{LINWUP}	4.0	5.25	6.0	V

Table 63. Analog die Registers - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset[71]	Name		15 7	14 6	13 5	12 4	11 3	10 2	9 1	8 0
0xAB	COMP_IO	R	COC[7:0]							
	Offset current compensation	W								
0xAC	COMP_VSG Gain voltage compensation vsense channel	R	0	0	0	0	0	0	VSGC[9:8]	
		W								
		R	VSGC[7:0]							
		W								
0xAE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0xAF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0xB0	COMP_IG4 Gain current compensation 4	R	0	0	0	0	0	0	IGC4[9:8]	
		W								
		R	IGC4[7:0]							
		W								
0xB2	COMP_IG8 Gain current compensation 8	R	0	0	0	0	0	0	IGC8[9:8]	
		W								
		R	IGC8[7:0]							
		W								
0xB4	COMP_IG16 Gain current compensation 16	R	0	0	0	0	0	0	IGC16[9:8]	
		W								
		R	IGC16[7:0]							
		W								
0xB6	COMP_IG32 Gain current compensation 32	R	0	0	0	0	0	0	IGC32[9:8]	
		W								
		R	IGC32[7:0]							
		W								
0xB8	COMP_IG64 Gain current compensation 64	R	0	0	0	0	0	0	IGC64[9:8]	
		W								
		R	IGC64[7:0]							
		W								
0xBA	COMP_IG128 Gain current compensation 128	R	0	0	0	0	0	0	IGC128[9:8]	
		W								
		R	IGC128[7:0]							
		W								
0xBC	COMP_IG256 Gain current compensation 256	R	0	0	0	0	0	0	IGC256[9:8]	
		W								
		R	IGC256[7:0]							
		W								
0xBE	COMP_IG512 Gain current compensation 512	R	0	0	0	0	0	0	IGC512[9:8]	
		W								
		R	IGC512[7:0]							
		W								

During Sleep mode, the only active voltage regulator is VDDL, supplying the low power oscillator (LPOSC), and the permanently supplied digital blocks.

When an enabled wake-up condition occurs, the shutdown voltage regulators are re-enabled, and once their outputs are above reset threshold, the RESET_A signal is released, and the microcontroller will start its normal operation. The wake-up source is flagged in the PCR Status Register (PCR_SR (hi)).

The microcontroller has to acknowledge the Normal mode, by writing the OPM=00, to allow a controlled transition into the D2D Clock domain. If the clock domain transition is not required, the microcontroller may issue a sleep / stop mode entry instead (see Section 5.2.5, “Device Clock Tree" for details on the limitations during the intermediate state).

5.2.2.8.2 Stop Mode

Writing the PCR Control Register (PCR_CTL) with OPM=01, the MM912_637 analog die will enter Stop mode with the configured wake-up sources (see Section 5.2.4, “Wake-up Sources"), after the D2DCLK signal has been stopped by the MCU die entering Stop.

NOTE

After writing the PCR Control Register (PCR_CTL) with OPM=01, the register content of the SCI (S08SCIV4) and TIMER (TIM16B4C) module registers are only read until Normal mode is entered again. This is important in case the MCU does not effectively enter STOP, due to an IRQ pending from one of the two blocks. (Having any analog die IRQ allowed when entering Low Power mode is not recommended).

During Stop mode, the MM912_637 has the same behavior as during Sleep mode, except VDDX is still powered by the internal Clamp_5v, to supply the MCU STOP mode current. As this current is limited, the MCU die must be switched into STOP mode after sending the Stop command for the analog die.

If any enabled wake up condition occurs, the shutdown voltage regulators are re-enabled, and once their outputs are above the reset threshold, VDDX is switched to the main regulator, an D2D interrupt (D2DINT) is issued to wake-up the MCU, and the microcontroller will continue its normal operation. The wake-up source is flagged in the PCR Status Register (PCR_SR (hi)).

The microcontroller has to acknowledge the Normal mode by writing the OPM=00. This allows a controlled transition into the D2D Clock domain. If the clock domain transition is not required, the microcontroller may issue a sleep / stop mode entry instead (see Section 5.2.5, “Device Clock Tree" for details on the limitations during the intermediate state).

NOTE

After writing the PCR Control Register (PCR_CTL) with OPM=01, writing OPM=00 (Normal mode) is allowed to wake-up the analog die. The reduced current capability of the MCU regulator supply (VDDX) has to be considered.

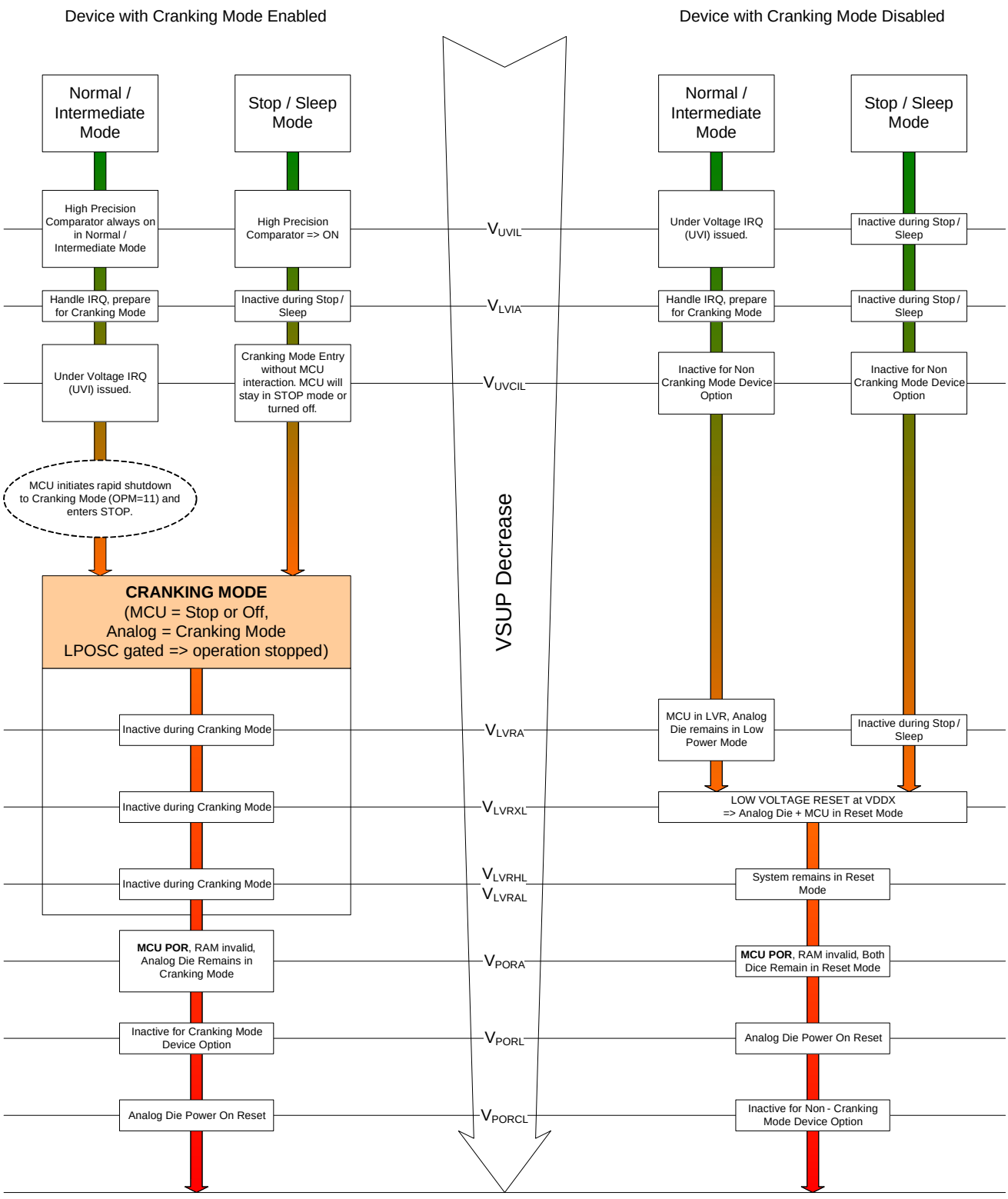


Figure 18. Power Down Sequence

Table 70. Recommended Clock Settings

f_{D2D} / MHz				POSTDIV for (SYNDIV=fVCO in MHz)																Divider for[83] D2DFCLK=512kHz	PRESC[15:9] (dec)[83]
D2DCLKDIV=1 (f_{BUS})	D2DCLKDIV=2	D2DCLKDIV=3	D2DCLKDIV=4	31=65.536	30=63.488	29=61.440	28=59.392	27=57.344	26=55.296	25=53.248	24=51.200	23=49.152	22=47.104	21=45.056	20=43.008	19=40.960	18=38.912	17=36.864	16=34.816	15=32.768		
27.648		9.216							0												54	53;54
26.624	13.312									0											52	51;52
25.600											0										50	49;50
24.576	12.288	8.192	6.144									0									48	47;48
23.552													0								46	45;46
22.528	11.264													0							44	43;44
21.504		7.168													0						42	41;42
20.480	10.240		5.120													0					40	39;40
19.456																	0				48	47;48
18.432	9.216	6.144																0			36	35;36
17.408																			0		34	33;34
16.384	8.192		4.096	1																0	32	31;32
15.360		5.120				1															30	29;30
14.336	7.168							1													28	27;28
13.312										1											26	25;26
12.288	6.144	4.096	3.072									1									24	23;24
11.264														1							22	21;22
10.240	5.120					2										1					20	19;20
9.216		3.072							2									1			18	17;18
8.192	4.096		2.048	3								2								1	16	15;16
7.168								3							2						14	13;14
6.144	3.072	2.048				4						3						2			12	11;12
5.120						5					4					3					10	9;10
4.096	2.048			7				6				5				4				3	8	7;8
3.072						9			8			7			6			5			6	5;6
2.048				15		14		13		12		11		10		9		8		7	4	4

Notes
83.For D2DCLKDIV=1

5.2.6 System Resets

To guarantee safe operation, several RESET sources have been implemented in the MM912_637 device. Both the MCU and the analog die are designed to initiate reset events on internal sources and the MCU is capable of being reset by external events including the analog die reset output. The analog die is capable of being reset by the MCU in stop and cranking mode only.

5.2.6.1 Device Reset Overview

The MM912_637 reset concept includes two external reset signals, $\overline{\text{RESET}}$ (MCU) and $\overline{\text{RESET\_A}}$ (analog Die). Figure 26 illustrates the general configuration.

Table 90. Interrupt Source Register (INT_SRC (hi)) - Register Field Descriptions

Field	Description
1 HTI	High temperature interrupt status 0 - No high temperature interrupt pending 1 - High temperature interrupt pending
0 UVI	Under-voltage interrupt pending or wake-up from Cranking mode status 0 - No under-voltage Interrupt pending or wake-up from Cranking mode 1 - Under-voltage interrupt pending or wake-up from Cranking mode

5.3.5.3.2 Interrupt Source Register (INT_SRC (lo))

Table 91. Interrupt Source Register (INT_SRC (lo))

Offset[101] 0x09 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	CAL	LTC	CVMI	RX	TX	ERR
W								

Notes

101.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 92. Interrupt Source Register (INT_SRC (lo)) - Register Field Descriptions

Field	Description
5 CAL	Calibration request interrupt status 0 - No calibration request interrupt pending 1 - Calibration request interrupt pending
4 LTC	Life time counter interrupt status 0 - No life time counter interrupt pending 1 - Life time counter interrupt pending
3 CVMI	Current / Voltage measurement interrupt status 0 - No Current / Voltage measurement interrupt pending 1 - Current / Voltage measurement interrupt pending
2 RX	SCI receive interrupt status 0 - No SCI receive interrupt pending 1 - SCI receive interrupt pending
1 TX	SCI transmit interrupt status 0 - No SCI transmit interrupt pending 1 - SCI transmit interrupt pending
0 ERR	SCI error interrupt status 0 - No SCI transmit interrupt pending 1 - SCI transmit interrupt pending

Table 97. Interrupt Mask Register (INT_MSK (hi)) - Register Field Descriptions

Field	Description
7 TOVM	Timer overflow interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
6 CH3M	Timer channel 3 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
5 CH2M	Timer channel 2 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 CH1M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CH0M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
2 LTIM	LIN driver over-temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
1 HTIM	High temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
0 UVIM	Under-voltage interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

5.3.5.3.5 Interrupt Mask Register (INT_MSK (lo))

Table 98. Interrupt mask register (INT_MSK (lo))

Offset[104] 0x0D — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	CALM	LTCM	CVMM	RXM	TXM	ERRM
W								
Reset	0	0	0	0	0	0	0	0

Notes
104.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 99. Interrupt Mask Register (INT_MSK (lo)) - Register Field Descriptions

Field	Description
5 CALM	Calibration request interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 LTCM	Life time counter interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CVMM	Current / Voltage measurement interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

5.7.6.3.8 PGA Gain (ACQ_GAIN)

Table 123. PGA Gain (ACQ_GAIN)

Offset[124] 0x62 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	IGAIN[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

Notes
124.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 124. PGA Gain (ACQ_GAIN) - Register Field Descriptions

Field	Description
2-0 IGAIN[2:0]	PGA Gain Register - Writing will select (manually override) the PGA gain if the automatic gain control is disabled (AGEN=0). Reading will return current gain setting (including the auto gain). The register content will also determine the current channel offset compensation buffer accessed through the COC[7:0] register. 000 - PGA Gain = 4 001 - PGA Gain = 8 010 - PGA Gain = 16 011 - PGA Gain = 32 100 - PGA Gain = 64 101 - PGA Gain = 128 110 - PGA Gain = 256 111 - PGA Gain = 512

5.7.6.3.9 GCB Threshold (ACQ_GCB)

Table 125. GCB Threshold (ACQ_GCB)

Offset[125] 0x63 — Access: User read/write

	7	6	5	4	3	2	1	0
R	D (hi)				D (lo)			
W								
Reset	0	0	0	0	0	0	0	0

Notes
125.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 126. GCB Threshold (ACQ_GCB) - Register Field Descriptions

Field	Description
7-4 D[7:4]	Gain Control Block (GCB) - 4 Bit Gain “Up” Threshold. See Section 5.7.3.1.3, “Gain Control Block (GCB)".
3-0 D[3:0]	Gain Control Block (GCB) - 4 Bit Gain “Down” Threshold. See Section 5.7.3.1.3, “Gain Control Block (GCB)".

Table 255. LIN Transmit Line Definition (LIN_TX) - Register Field Descriptions

Field	Description
1 FROMPTB	LIN_TX internally routed from PTB. See Section 5.10, “General Purpose I/O - GPIO" for details.(215) 0 - LIN transmitter disconnected from PTB module. 1 - LIN transmitter connected to the PTB module.
0 FROMSCI	LIN_TX internally routed from SCI(215) 0 - LIN transmitter disconnected from SCI module. 1 - LIN transmitter connected to the SCI module.

Notes

215.In case both, FROMPTB and FROMSCI are selected, the SCI has priority and the PTB signal is ignored. In any case, the signal is logically ORed with the TXD direct transmitter control.

5.11.3.3.5 LIN Receive Line Definition (LIN_RX)

Table 256. LIN Receive Line Definition (LIN_RX)

Offset(216) 0x55 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	TOPTB	TOSCI
W								
Reset	0	0	0	0	0	0	0	0

Notes

216.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 257. LIN Receive Line Definition (LIN_RX) - Register Field Descriptions

Field	Description
1 TOPTB	LIN_RX internally routed to PTB 0 - LIN receiver disconnected from PTB module. 1 - LIN receiver connected to the PTB module.
0 TOSCI	LIN_RX internally routed to SCI 0 - LIN receiver disconnected from SCI module. 1 - LIN receiver connected to the SCI module.

NOTE

In order to route the RX signal to the Timer Input capture, one of the PTBx must be configured as a pass through.

5.13.2.3.3 Life Time Counter status register (LTC_SR)

Table 280. Life Time Counter status register (LTC_SR)

Offset[232] 0x3A — Access: User read/write

	7	6	5	4	3	2	1	0
R	LTCOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Notes
232.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 281. Life Time Counter Status Register (LTC_SR) - Register Field Descriptions

Field	Description
0 LTCOF	Life Time Counter Overflow Flag. Writing 1 will clear the flag. 1 - Life time counter overflow detected. 0 - No life time counter overflow since last clear

5.13.2.3.4 Life Time Counter Register (LTC_CNT1, LTC_CNT0)

Table 282. Life Time Counter Register (LTC_CNT1, LTC_CNT0)

Offset (233),(234) 0x3C, 0x3E — Access: User read/write

	7	6	5	4	3	2	1	0
R W R W	LTC[31:16]							
R W R W	LTC[15:0]							
Reset	0	0	0	0	0	0	0	0

Notes
233.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.
234.Those Registers are 16-Bit access only.

Table 283. Life Time Counter Register (LTC_CNT1, LTC_CNT0) - Register Field Descriptions

Field	Description
0-31 LTC[31:0]	Life Time Counter Register The two 16-Bit words of the 32-Bit Life Time Counter register represent the current counter status. Whenever the microcontroller performs a reading operation on one of the 16Bit registers, the Life Time Counter is stopped until the remaining 16-Bit register is read, to prevent loss of information. After the second part is read, the LTC continues automatically. Write operations should be performed with the Life Time Counter disabled to prevent a loss of data.

5.16 MCU - Port Integration Module (9S12I128PIMV1)

5.16.1 Introduction

The Port Integration Module (PIM) establishes the interface between the S12I128 peripheral modules SPI and Die-To-Die Interface module (D2DI) to the I/O pins of the MCU.

All port A and port E pins support general purpose I/O functionality, if not in use with other functions. The PIM controls the signal prioritization and multiplexing on shared pins.

5.16.1.1 Overview

Figure 52 is a block diagram of the Port Integration Module.

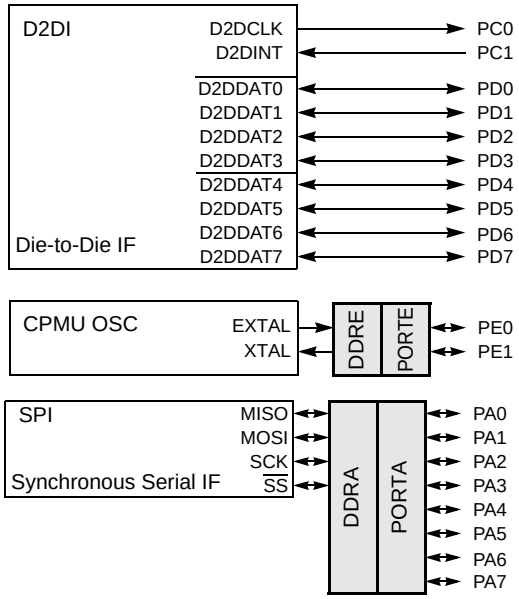


Figure 52. Port Integration Module - Block Diagram

5.16.1.2 Features

- 8-pin port A associated with the SPI module
- 2-pin port C used as D2DI clock output and D2DI interrupt input
- 8-pin port D used as 8 or 4 bit data I/O for the D2DI module
- 2-pin port E associated with the CPMU OSC module
- GPIO function shared on port A and E pins
- Pull-down devices on PC1 and PD7-0 if used as D2DI inputs
- Reduced drive capability on PC0 and PD7-0 on per pin basis

The Port Integration Module includes these distinctive registers:

- Data registers for ports A and E when used as general purpose I/O
- Data direction registers for ports A and E when used as general purpose I/O
- Port input register on ports A and E
- Reduced drive register on port C and D

NOTE

Care must be taken to ensure that all interrupt requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed at all or the result may be a spurious interrupt request (vector at address (vector base + 0x0080)).

5.17.4.3 Reset Exception Requests

The INT module supports three system reset exception request types (Refer to the Clock and Reset generator module for details):

1. Pin reset, power-on reset or illegal address reset, low voltage reset (if applicable)
2. Clock monitor reset request
3. COP watchdog reset request

5.17.4.4 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT module upon request by the CPU is shown in Table 312.

Table 312. Exception Vector Map and Priority

Vector Address[240]	Source
0xFFFE	Pin reset, power-on reset, illegal address reset, low voltage reset (if applicable)
0xFFFC	Clock monitor reset
0xFFFA	COP watchdog reset
(Vector base + 0x00F8)	Unimplemented opcode trap
(Vector base + 0x00F6)	Software interrupt instruction (SWI) or BDM vector request
(Vector base + 0x00F4)	X bit maskable interrupt request (XIRQ or D2D error interrupt)[241]
(Vector base + 0x00F2)	IRQ or D2D interrupt request[242]
(Vector base + 0x00F0–0x0082)	Device specific I bit maskable interrupt sources (priority determined by the low byte of the vector address, in descending order)
(Vector base + 0x0080)	Spurious interrupt

Notes
240.16-bit vector address based
241.D2D error interrupt on MCUs featuring a D2D initiator module, otherwise XIRQ pin interrupt
242.D2D interrupt on MCUs featuring a D2D initiator module, otherwise IRQ pin interrupt

5.17.5 Initialization/Application Information

5.17.5.1 Initialization

After a system reset, the software should:

1. Initialize the interrupt vector base register, if the interrupt vector table is not located at the default location (0xFF80–0xFFF9).
2. Enable I bit maskable interrupts by clearing the I bit in the CCR.
3. Enable the X bit maskable interrupt by clearing the X bit in the CCR.

5.19.4.3.4 Channel Priorities

In case of simultaneous matches, the priority is resolved according to Table 378. The lower priority is suppressed. It is possible to miss a lower priority match, if it occurs simultaneously with a higher priority. The priorities described in Table 378 dictate that in the case of simultaneous matches, the match pointing to Final state has highest priority, followed by the lower channel number (0,1,2).

Table 378. Channel Priorities

Priority	Source	Action
Highest	TRIG	Enter Final State
	Channel pointing to Final State	Transition to next state as defined by state control registers
	Match0 (force or tag hit)	Transition to next state as defined by state control registers
	Match1 (force or tag hit)	Transition to next state as defined by state control registers
Lowest	Match2 (force or tag hit)	Transition to next state as defined by state control registers

5.19.4.4 State Sequence Control

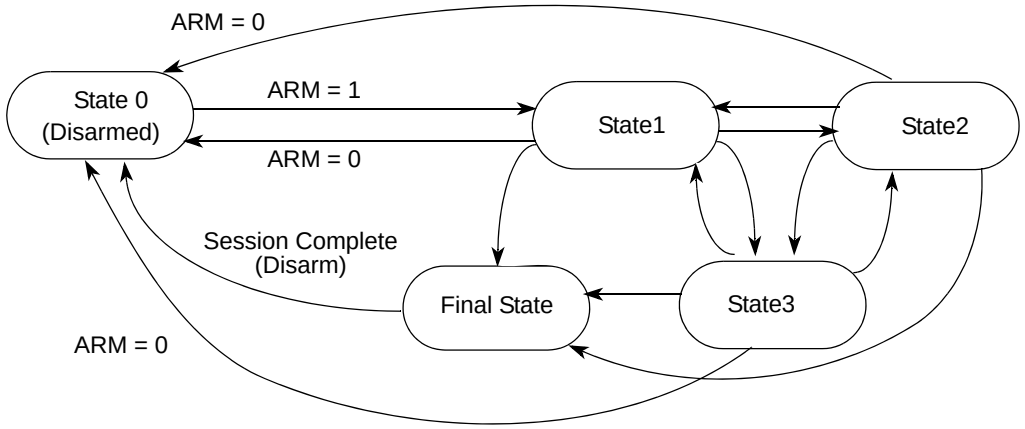


Figure 65. State Sequencer Diagram

The state sequencer allows a defined sequence of events to provide a trigger point for tracing of data in the trace buffer. Once the DBG module has been armed by setting the ARM bit in the DBGC1 register, the state 1 of the state sequencer is entered. Further transitions between the states are then controlled by the state control registers and channel matches. From Final state, the only permitted transition is back to the disarmed state 0. Transition between any of the states 1 to 3 is not restricted. Each transition updates the SSF[2:0] flags in DBGSR accordingly to indicate the current state.

Alternatively, writing to the TRIG bit in DBGSC1, provides an immediate trigger independent of comparator matches.

Independent of the state sequencer, each comparator channel can be individually configured to generate an immediate breakpoint when a match occurs, through the use of the BRK bits in the DBGxCTL registers. It is possible to generate an immediate breakpoint on selected channels, while a state sequencer transition can be initiated by a match on other channels. If a debug session is ended by a match on a channel, the state sequencer transitions through Final state for a clock cycle to state 0. This is independent of tracing and breakpoint activity, and with tracing and breakpoints disabled, the state sequencer enters state 0 and the debug module is disarmed.

5.19.4.4.1 Final State

On entering Final state, a trigger may be issued to the trace buffer according to the trace alignment control, as defined by the TALIGN bit (see Section 5.19.3.2.3, “Debug Trace Control Register (DBGTCR)””). If the TSOURCE bit in DBGTCR is clear, then the trace buffer is disabled and the transition to Final state can only generate a breakpoint request. In this case or upon completion of a tracing session when tracing is enabled, the ARM bit in the DBGC1 register is cleared, returning the module to

5.22.4.6.3 PLL Bypassed External Mode (PBE)

In this mode, the Bus Clock is based on the external oscillator clock. The reference clock for the PLL is based on the external oscillator. The adaptive spike filter and detection logic can be enabled which uses the VCOCLK to filter and qualify the external oscillator clock.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock.

This mode can be entered from default mode PEI by performing the following steps:

1. Make sure the PLL configuration is valid.
2. Optionally, the adaptive spike filter and detection logic can be enabled by calculating the integer value for the OSCFIL[4:0] bits and setting the bandwidth (OSCBW) accordingly.
3. Enable the external Oscillator (OSCE bit)
4. Wait for the PLL being locked (LOCK = 1) and the oscillator to start-up, and additionally being qualified if the Adaptive Oscillator Filter is enabled (UPOSC=1).
5. Clear all flags in the CPMUFLG register to be able to detect any status bit change.
6. Optionally status interrupts can be enabled (CPMUINT register).
7. Select the Oscillator Clock (OSCCLK) as Bus Clock (PLLSEL=0)

Since the Adaptive Oscillator Filter (adaptive spike filter and detection logic) uses the VCOCLK to continuously filter and qualify the external oscillator clock, losing PLL lock status (LOCK=0) means losing the oscillator status information as well (UPOSC=0).

The impact of losing the oscillator status in PBE mode is as follows:

- PLLSEL is set automatically and the Bus Clock is switched back to the PLLCLK.
- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

In the PBE mode, not every noise disturbance can be indicated by bits LOCK and UPOSC (both bits are based on the Bus Clock domain). There are clock disturbances possible, after which UPOSC and LOCK both stay asserted, while occasional pauses on the filtered OSCCLK and resulting Bus Clock occur. The adaptive spike filter is still functional and protects the Bus Clock from frequency overshoot due to spikes on the external oscillator clock. The filtered OSCCLK and resulting Bus Clock will pause until the PLL has stabilized again.

5.22.5 Resets

5.22.5.1 General

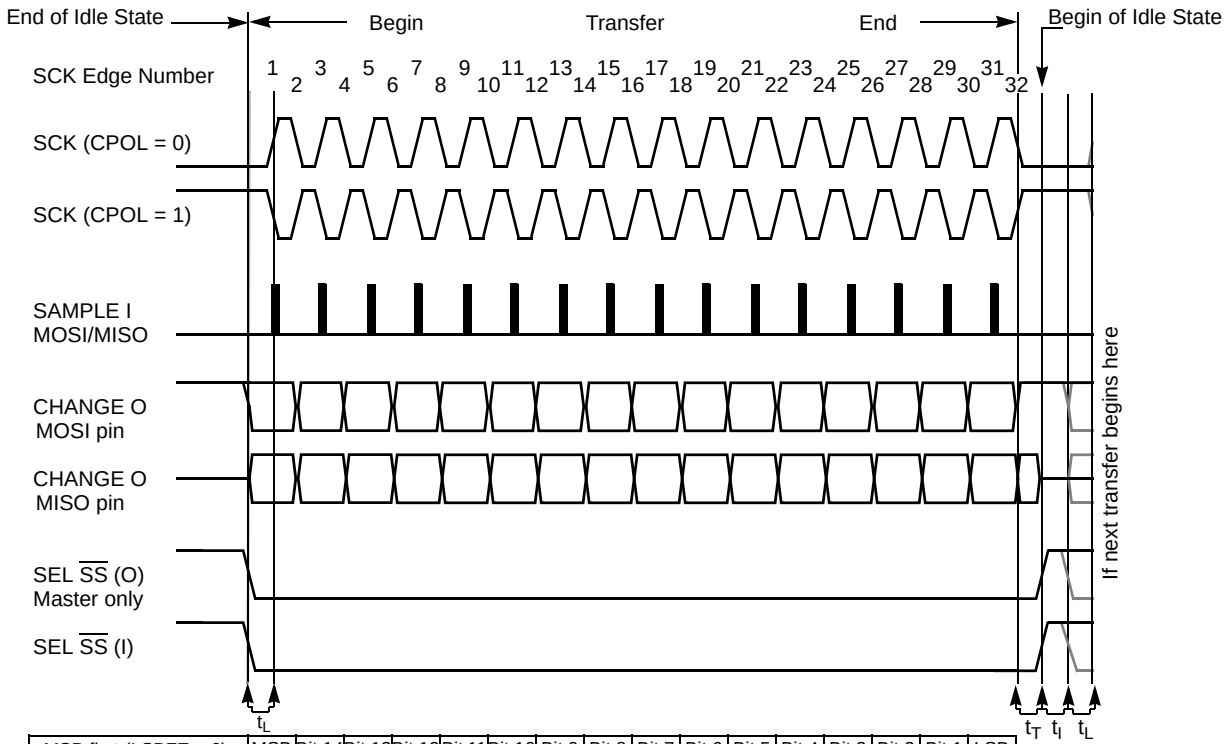
All reset sources are listed in Table 441. Refer to MCU specification for related vector addresses and priorities.

Table 441. Reset Summary

Reset Source	Local Enable
Power-On Reset (POR)	None
Low Voltage Reset (LVR)	None
External pin $\overline{\text{RESET}}$	None
Illegal Address Reset	None
Clock Monitor Reset	OSCE Bit in CPMUOSC register
COP Reset	CR[2:0] in CPMUCOP register

5.22.5.2 Description of Reset Operation

Upon detection of any reset in Table 441, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles, the $\overline{\text{RESET}}$ pin is released. The reset generator of the S12CPMU waits for additional 256 PLLCLK cycles and then samples the $\overline{\text{RESET}}$ pin to determine the originating source. Table 442 shows which vector will be fetched.



MSB first (LSBFE = 0)	MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
LSB first (LSBFE = 1)	LSB	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	MSB

t_L = Minimum leading time before the first SCK edge

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time)

t_L, t_T, and t_I are guaranteed for the master mode and required for the slave mode.

Figure 106. SPI Clock Format 0 (CPHA = 0), with 16-Bit Transfer Width Selected (XFRW = 1)

In slave mode, if the $\overline{SS}$ line is not deasserted between the successive transmissions, then the content of the SPI data register is not transmitted; instead the last received data is transmitted. If the $\overline{SS}$ line is deasserted for at least minimum idle time (half SCK cycle) between successive transmissions, then the content of the SPI data register is transmitted.

In master mode, with slave select output enabled, the $\overline{SS}$ line is always deasserted and reasserted between successive transfers for at least minimum idle time.

5.23.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the n[(278)]-cycle transfer operation.

Notes

278.n depends on the selected transfer width, refer to Section 5.23.3.2.2, “SPI Control Register 2 (SPICR2)"

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

When the third edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the SPI shift register, depending on LSBFE bit. After this edge, the next bit of the master data is coupled out of the serial data output pin of the master to the serial input pin on the slave.

This process continues for a total of n^4 edges on the SCK line with data being latched on even numbered edges and shifting taking place on odd numbered edges.

5.24.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Table 479. Flash Error Configuration Register (FERCNFG)

Address: 0x0105

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All assigned bits in the FERCNFG register are readable and writable.

Table 480. FERCNFG Field Descriptions

Field	Description
1 DFDIE	**Double Bit Fault Detect Interrupt Enable** — The DFDIE bit controls interrupt generation when a double bit fault is detected during a Flash block read operation. 0 DFDIF interrupt disabled 1 An interrupt will be requested whenever the DFDIF flag is set (see Section 5.24.3.2.8, “Flash Error Status Register (FERSTAT)”)
0 SFDIE	**Single Bit Fault Detect Interrupt Enable** — The SFDIE bit controls interrupt generation when a single bit fault is detected during a Flash block read operation. 0 SFDIF interrupt disabled whenever the SFDIF flag is set (see Section 5.24.3.2.8, “Flash Error Status Register (FERSTAT)”) 1 An interrupt will be requested whenever the SFDIF flag is set (see Section 5.24.3.2.8, “Flash Error Status Register (FERSTAT)”)

5.24.3.2.7 Flash Status Register (FSTAT)

The FSTAT register reports the operational status of the Flash module.

Table 481. Flash Status Register (FSTAT)

Address: 0x0106

	7	6	5	4	3	2	1	0
R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT[1:0]	
W								
Reset	1	0	0	0	0	0	0[286]	0[286]

= Unimplemented or Reserved

Notes

286.Reset value can deviate from the value shown if a double bit fault is detected during the reset sequence (see Section 5.24.6, “Initialization”).

CCIF, ACCERR, and FPVIOL bits are readable and writable, MGBUSY and MGSTAT bits are readable but not writable, while remaining bits read 0 and are not writable.

5.24.3.2.17 Flash Reserved5 Register (FRSV5)

This Flash register is reserved for factory testing.

Table 503. Flash Reserved5 Register (FRSV5)

Address: 0x0111

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV5 register read 0 and are not writable.

5.24.3.2.18 Flash Reserved6 Register (FRSV6)

This Flash register is reserved for factory testing.

Table 504. Flash Reserved6 Register (FRSV6)

Address: 0x0112

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV6 register read 0 and are not writable.

5.24.3.2.19 Flash Reserved7 Register (FRSV7)

This Flash register is reserved for factory testing.

Table 505. Flash Reserved7 Register (FRSV7)

Address: 0x0113

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV7 register read 0 and are not writable.

5.24.4 Functional Description

5.24.4.1 Modes of Operation

The FTMRC128K1 module provides the modes of operation, as shown in Table 506. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and DFPROT registers, Scratch RAM writes, and the command set availability (see Table 508).

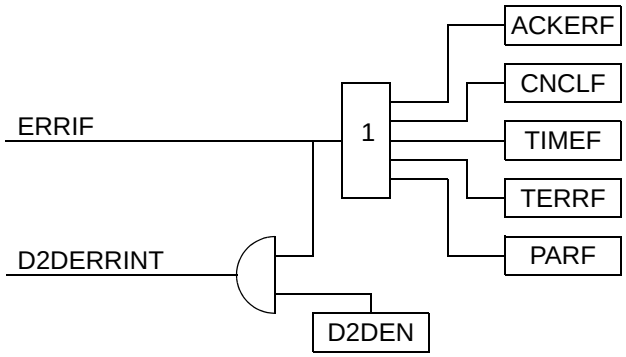


Figure 120. D2D Internal Interrupts

5.25.5 Initialization Information

During initialization, the transfer width, clock divider, and timeout value must be set according to the capabilities of the target device before starting any transaction. See the D2D Target specification for details.

5.25.6 Application Information

5.25.6.1 Entering Low Power Mode

The D2DI module is typically used on a microcontroller along with an analog companion device containing the D2D target interface and supplying the power. Interface specification does not provide special wires for signalling low power modes to the target device. The CPU should determine when it is time to enter one of the above power modes.The basic flow is as follows:

1. CPU determines there is no more work pending.
2. CPU writes a byte to a register on the analog die using blocking write configuring which mode to enter.
3. Analog die acknowledges that write sending back an acknowledge symbol on the interface.
4. CPU executes WAIT or STOP command.
5. Analog die can enter low power mode - (S12 needs some more cycles to stack data!)

```
; Example shows S12 code
SEI         ; disable interrupts during test
; check is there is work pending?
; if yes, branch off and re-enable interrupt
; else
LDAA        #STOP_ENTRY
STAA        MODE_REG            ; store to the analog die mode reg (use blocking write here)
CLI         ; re-enable right before the STOP instruction
STOP        ; stack and turn off all clocks inc. interface clock
```

For wake-up from STOP the basic flow is as follows:

1. Analog die detects a wake-up condition e.g. on a switch input or start bit of a LIN message.
2. Analog die exits Voltage Regulator low power mode.
3. Analog die asserts the interrupt signal D2DINT.
4. CPU starts clock generation.
5. CPU enters interrupt handler routine.
6. CPU services interrupt and acknowledges the source on the analog die.

NOTE

Entering STOP mode or WAIT mode with D2DSWAI asserted, the clock will complete the high duty cycle portion and settle at a low level.

6.2.2.7 Temperature Sense Module Trimming (COMP_ITO, COMP_ITG)

To achieve the specified accuracy of the internal temperature sense module, the optimum trim information is determined during final test at hot / cold temperature and stored into the IFR register block of the MCU FLASH memory. On device every power up, the corresponding trim value needs to be copied into the desired analog register via D2D interface.

6.2.2.8 Band Gap Reference - Diagnostic Measurements (GAIN_CAL_X_X)

To achieve the specified accuracy of the voltage and current channels, reference measurements are performed during final test and stored for different temperatures into the IFR register block of the MCU FLASH memory. The information is used during the calibration procedure described in Section 5.7.5, “Calibration".

6.2.2.9 HOT / COLD Gain Compensation Data (0x0_40EC...0x0_40FF)

To achieve the specified accuracy of the voltage and current channels, reference measurements are performed during final test and stored for different temperatures into the IFR register block of the MCU FLASH memory. The information is used during the calibration procedure described in Section 5.7.5, “Calibration".

6.3 Memory Map and Registers

6.3.1 Overview

This section provides a detailed description of the memory map and registers for the analog die trimming excluding registers used for calibration located from offset 0xE0 to 0xEF. Refer to Section 5.7.5, “Calibration" for details on Current Channel Gain Compensation Trim (COMP_IG4-COMP_IG512), Voltage Channel Compensation (COMP_VOx, COMP_VSG, COMP_VOG), Temperature Sense Module Trimming (COMP_ITO, COMP_ITG), Band Gap Reference - Diagnostic Measurements (GAIN_CAL_X_X) and HOT / COLD Gain Compensation Data (0x0_40EC...0x0_40FF).

6.3.2 Module Memory Map

The memory map for the Compensation module is given below in Table 565.

Table 565. Module Memory Map

Offset[308]	Name		7	6	5	4	3	2	1	0
0xE0	TRIM_BG0 (hi)	R	0	0	TCIBG2[2:0]			TCIBG1[2:0]		
	Trim bandgap 0	W								
0xE1	TRIM_BG0 (lo)	R	0	0	IBG2[2:0]			IBG1[2:0]		
	Trim bandgap 0	W								
0xE2	TRIM_BG1 (hi)	R	UBG3	DBG3	TCBG2[2:0]			TCBG1[2:0]		
	Trim bandgap 1	W								
0xE3	TRIM_BG1 (lo)	R	0	0	0	0	0	SLPBG[2:0]		
	Trim bandgap 1	W								
0xE4	TRIM_BG2 (hi)	R	V1P2BG2[3:0]				V1P2BG1[3:0]			
	Trim bandgap 2	W								
0xE5	TRIM_BG2 (lo)	R	V2P5BG2[3:0]				V2P5BG1[3:0]			
	Trim bandgap 2	W								
0xE6	TRIM_LIN	R	0	0	0	0	0	0	0	LIN
	Trim LIN	W								