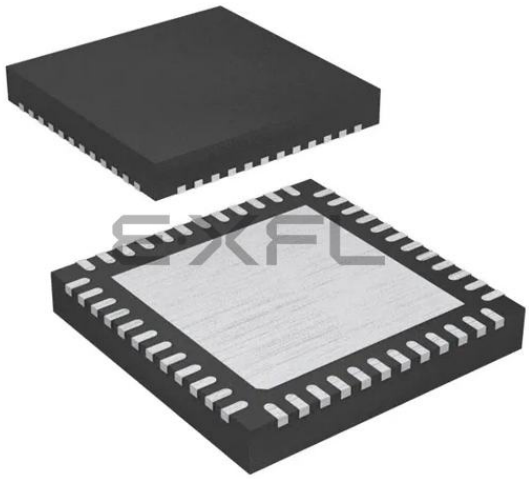


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Battery Monitor
Core Processor	S12
Program Memory Type	FLASH (96KB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI, SPI
Number of I/O	8
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912i637am2epr2

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
3	PE1/XTAL	MCU Oscillator	XTAL is one of the optional crystal/resonator drivers and external clock pins, and the PE1 port may be used as a general purpose I/O. On reset all the device clocks are derived from the internal reference clock. See Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)".
4	TEST	MCU Test	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to VSSRX in user mode.
5	PA5	MCU PA5	General purpose port A input or output pin 5. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
6	PA4	MCU PA4	General purpose port A input or output pin 4. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
7	PA3	MCU PA3 / $\overline{SS}$	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
8	PA2	MCU PA2 / SCK	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
9	PA1	MCU PA1 / MOSI	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
10	PA0	MCU PA0 / MISO	General purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
11	VSSRX	MCU 5.0 V Ground	External ground for the MCU - VDDRX return path.
12	VDDRX	MCU 5.0 V Supply	5.0 V MCU power supply. MCU core- (internal 1.8 V regulator) and flash (internal 2.7 V regulator) supply.
13	VSSD2D	MCU 2.5 V Ground	External ground for the MCU - VDDD2D return path.
14	VDDD2D	MCU 2.5 V Supply	2.5 V MCU power supply. Die to die buffer supply.
15	NC	Not connected	This pin must be grounded in the application.
16	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
17	VDDX	Voltage Regulator Output 5.0 V	5.0 V main voltage regulator output pin. An external capacitor (C_{VDDX}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
18	DGND	Digital Ground	This pin is the device digital ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
19	VDDH	Voltage Regulator Output 2.5 V	2.5 V high power main voltage regulator output pin to be connected with the VDDD2D MCU pin. An external capacitor (C_{VDDH}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
20	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
21	VSUP	Power Supply	This pin is the device power supply pin. A reverse battery protection diode is required. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
22	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See Section 5.11, “LIN".
23	LGND	LIN Ground Pin	This pin is the device LIN ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
24	NC	Not connected (reserved)	This pin must be grounded in the application.
25	NC	Not connected	This pin must be grounded in the application.
26	VDDA	Analog Voltage Regulator Output	Low power analog voltage regulator output pin, permanently supplies the analog front end. An external capacitor (C_{VDDA}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
27	AGND	Analog Ground	This pin is the device analog voltage regulator and LP oscillator ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".

Table 5. Required / Recommended External Components

Name	Description	Value	Connection	Comment
C_{VDDH}	Blocking Capacitor	1.0 µF	VDDH-GND	
C_{VDDX}	Blocking Capacitor	220 nF	VDDX-GND	
C_{VDDA}	Blocking Capacitor	47 nF	VDDA-GND	
C_{VDDL}	Blocking Capacitor	n.a.	VDDL-GND	not required
C_{LIN}	LIN Bus Filter	n.a.	LIN-LGND	not required
R_{L0}	PTB3 / L0 Current Limitation	47 kΩ	L0	
C_{L0}	PTB3 / L0 ESD Protection	47 nF	L0-GND	
C_{TSUP}	Blocking Capacitor	220 pF	TSUP-GND	not required(2)
R_{VTEMP}	VTEMP Current Limitation	20 kΩ	VTEMP-signal	optional(1)

Notes

1.Required if extended EMC protection is needed

2.If an external temperature sensor is used, EMC compliance may require the addition of CTSUP. In this case the ECAP bit must be set to ensure the stability of the TSUP power supply circuit. See Section 5.6.1.2, “Block Diagram".

3.3 Pin Structure

Table 6 documents the individual pin characteristic.

Table 6. Pin Type / Structure

Pin #	Pin Name	Alternative Pin Function	Power Supply	Structure
1	PA6	n.a.	VDDRX	n.a.
2	PE0	EXTAL	VDDRX	PUPEE / OSCPINS_EN
3	PE1	XTAL	VDDRX	PUPEE / OSCPINS_EN
4	TEST	n.a.	n.a.	n.a.
5	PA5	n.a.	VDDRX	n.a.
6	PA4	n.a.	VDDRX	n.a.
7	PA3	SS	VDDRX	n.a.
8	PA2	SCK	VDDRX	n.a.
9	PA1	MOSI	VDDRX	n.a.
10	PA0	MISO	VDDRX	n.a.
11	VSSRX	n.a.		GND
12	VDDRX	n.a.		
13	VSSD2D	n.a.		GND
14	VDDD2D	n.a.		
15	NC	n.a.		
16	GNDSUB	n.a.		GND
17	VDDX	n.a.	VDDX	
18	DGND	n.a.	GND	B2B-Diode to GNDSUB
19	VDDH	n.a.	VDDH	Negative Clamp Diode, Dynamic ESD (transient protection)
20	GNDSUB	n.a.	GND	GNDSUB
21	VSUP	n.a.	VSUP	Negative Clamp Diode, >42 V ESD
22	LIN	n.a.	VSUP	No Negative Clamping Diode (-40 V), >42 V ESD
23	LGND	n.a.	GND	B2B-Diode to GNDSUB

5.1.2.3.2 Register Considerations

Table 66. Acquisition Control Register (ACQ_CTL)

Offset [73],[74] 0x58 Access: User read/write

	15	14	13	12	11	10	9	8
R	0	0	0	0	0	0	0	0
W	AHCRM	OPTEM	OPENEM	CVMIEM	ETMENM	ITMENM	VMENM	CMENM
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R	0	OPTE	OPENE	CVMIE	ETMEN	ITMEN	VMEN	CMEN
W	AHCR							
Reset	0	0	0	0	0	0	0	0

Notes
73.Offset related to 0x0200 for blocking access and 0x300 for non-blocking access within the global address space.
74.This register is 16-bit access only.

For Analog Option 1 devices, ETMEN must be set to 0 (external temperature measurement disabled).

5.1.2.4 Optional 2nd External Voltage Sense Input (VOPT)

For devices with Analog Option 1 (Optional 2nd External Voltage Sense Input not available), the following considerations are to be made:

5.1.2.4.1 Pinout Considerations

Pin	Pin Name for Option 2	Pin Name for Option 1	Comment
28	VOPT	NC	NC pin should be connected to GND

5.1.2.4.2 Register Considerations

Table 67. Acquisition Control Register (ACQ_CTL)

Offset [75],[76] 0x58 Access: User read/write

	15	14	13	12	11	10	9	8
R	0	0	0	0	0	0	0	0
W	AHCRM	OPTEM	OPENEM	CVMIEM	ETMENM	ITMENM	VMENM	CMENM
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R	0	OPTE	OPENE	CVMIE	ETMEN	ITMEN	VMEN	CMEN
W	AHCR							
Reset	0	0	0	0	0	0	0	0

Notes
75.Offset related to 0x0200 for blocking access and 0x300 for non-blocking access within the global address space.
76.This register is 16-bit access only.

For Analog Option 1 devices, OPTE must be set to 0 (VSENSE routed to ADC).

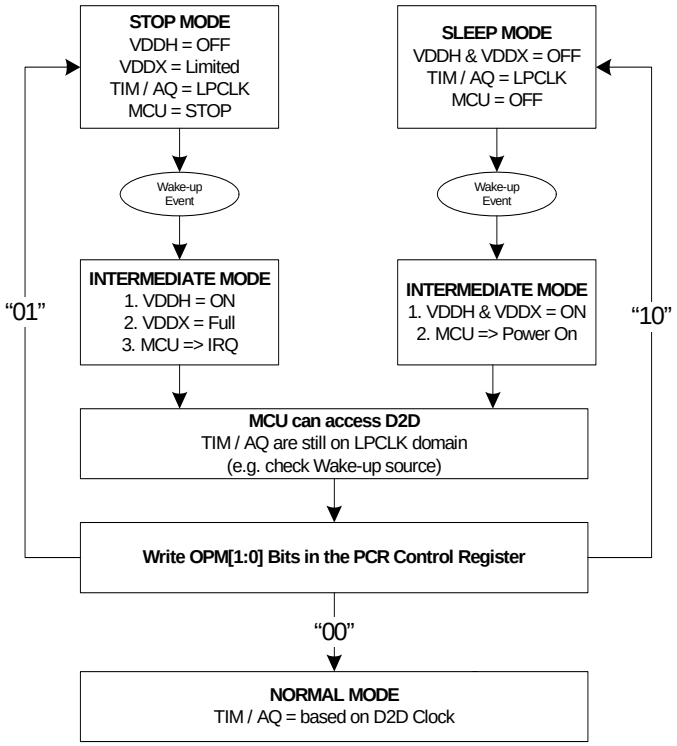


Figure 16. Low Power Mode to Normal Mode Transition through the Intermediate Mode

5.2.2.8 Low Power Modes

In low power mode, the MM912_637 is still active to monitor the battery current (triggered current measurement for current threshold detection and current accumulator function), and activities on the LIN interface and wake-up inputs. A cyclic wake-up using timer module is implemented for timed wake-up. Temperature measurements are optional to detect an out of calibration condition.

The Life Time counter is also incremented during Low Power mode, to issue a Wake-up on overflow. See Section 5.13, “Life Time Counter (LTC)" for additional details.

The average current consumption is reduced, and based on the actual low power mode, the active modules, and the wake-up timing.

NOTE

To avoid any lock condition, no analog die interrupt should be enabled or pending when entering LPM. To accomplish that condition, the analog die interrupts should be masked and served before writing the PCR_CTL register.

The MCU interrupts should be enabled right before the STOP command, to avoid any interrupt to be handled in between.

A wake-up from any of the low power modes will reset the window watchdog equal to a standard reset.

5.2.2.8.1 Sleep Mode

Writing the PCR Control Register (PCR_CTL) with OPM=10, the MM912_637 will enter Sleep mode with the configured wake-up sources (see Section 5.2.4, “Wake-up Sources").

NOTE

The power supply to the MCU will be turned off during Sleep mode. To safely approach this condition, the MCU should be put into a safe state (e.g STOP).

5.2.3 Power Management

To support the various operating modes and modules in the MM912_637, the following power management architecture has been implemented.

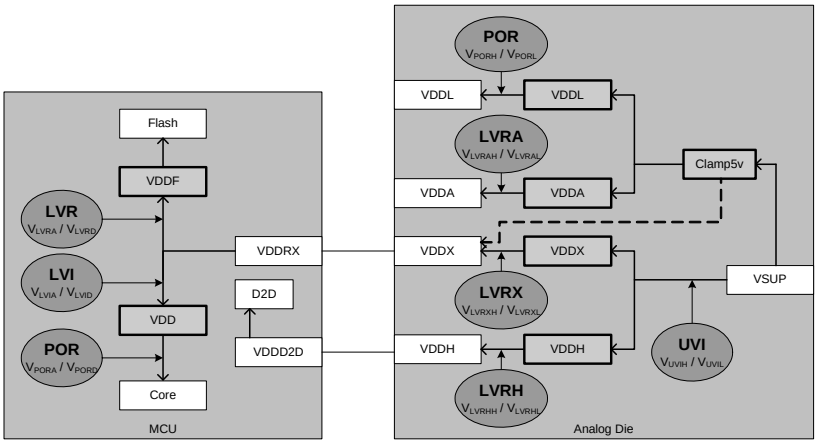


Figure 17. System Voltage Monitoring

5.2.3.1 Detailed Power Block Description

See recommended external components under Section 3.2, “Recommended External Components"".

5.2.3.1.1 VSUP

VSUP is the system power supply input, and must be reverse battery protected by an external diode. VSUP is monitored for under-voltage conditions (UVI). Once VSUP drops below V_{UVIL} an under-voltage interrupt (LVI) is issued.

NOTE

If the device has the cranking mode feature enabled, the under-voltage threshold would be V_{UVCIL} instead of V_{UVIL}.

5.2.3.1.2 VDDL

VDDL is the low power 2.5 V digital supply voltage, supplying the permanently active blocks. It is based on the internal Clamp5v voltage and always on. It is available externally, but must not be connected to any load.

5.2.3.1.3 VDDX

VDDX is the Normal mode 5.0 V regulator output, suppling the LIN block and the microcontroller via the VDDX pin. During STOP and SLEEP mode operation, the VDDX regulator is shut down (Clamp5v does supply the MCU during STOP mode).

5.2.3.1.4 VDDH

VDDH is the Normal mode 2.5 V regulator output, suppling only active blocks during Normal mode and the MCU Die to Die Interface, via the VDDH terminal. The VDDH regulator is shut down during both low power modes.

5.2.3.1.5 VDDA

VDDA is the 2.5 V analog supply voltage, active during Normal mode and I/T acquisitions. No external load must be connected to the VDDA terminal.

With the exception of the WDR, HWR, and TSDR, the $\overline{\text{RESET\_A}}$ pin is driven active as long the condition is pending. The WDR, HWR, and TSDR will issue a 2 x LPCLK cycle active at the pin. During cranking mode(84), only the VDDLR is active. During Low Power modes, only VDDXR and VDDAR are active reset sources. VDDAR is only active during active measurement in LPM. VDDXR and VDDAR are not active in Normal mode.

Notes
84.Not available on all device derivatives

5.2.6.3 Reset Source Summary

- HWR - Hardware Reset
  - Forced internal reset caused by writing the HWR bin in the PCR_CTL register. The source will be indicated by the HWRF bit.
- WDR - Watchdog Reset
  - Window watchdog failure. The source will be indicated by the WDRF bit.
- LVR - Low Voltage Reset
  - The Voltage at the VDDL, VDDH, VDDX, or VDDA has dropped below its reset threshold level. The source will be indicated for the VDDL by the LVRF + HVRF, for the VDDA by the AVRF, and for the VDDH by the HVRF bit. VDDX resets are not indicated via individual reset flags. See Figure 27 for dependencies.
- TSDR - Temperature Shutdown Reset
  - The critical shutdown temperature threshold has been reached. VDDA, VDDX, and VDDH will be disabled as long as the over-temperature condition is pending(85) and the reset source is indicated by the HTF bit.
- External Reset
  - During stop and cranking(85) mode, a low signal at the $\overline{\text{RESET\_A}}$ pin will reset the analog die. Since this condition can only be initiated by the microcontroller, no specific indicator flag is implemented.

Notes
85.Resulting in a VDDH Low Voltage Reset taking over the reset after the 2 LPCLK reset pulse

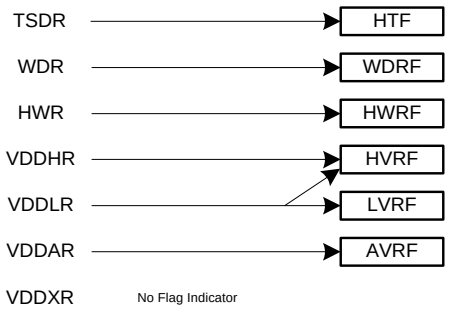


Figure 28. Reset Status Information

5.2.7 PCR - Memory Map and Registers

5.2.7.1 Overview

This section provides a detailed description of the memory map and registers.

5.2.7.2 Module Memory Map

The memory map for the Analog Die - Power, Clock and Resets - PCR module is given in Table 71

Table 90. Interrupt Source Register (INT_SRC (hi)) - Register Field Descriptions

Field	Description
1 HTI	High temperature interrupt status 0 - No high temperature interrupt pending 1 - High temperature interrupt pending
0 UVI	Under-voltage interrupt pending or wake-up from Cranking mode status 0 - No under-voltage Interrupt pending or wake-up from Cranking mode 1 - Under-voltage interrupt pending or wake-up from Cranking mode

5.3.5.3.2 Interrupt Source Register (INT_SRC (lo))

Table 91. Interrupt Source Register (INT_SRC (lo))

Offset(101) 0x09 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	CAL	LTC	CVMI	RX	TX	ERR
W								

Notes

101.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 92. Interrupt Source Register (INT_SRC (lo)) - Register Field Descriptions

Field	Description
5 CAL	Calibration request interrupt status 0 - No calibration request interrupt pending 1 - Calibration request interrupt pending
4 LTC	Life time counter interrupt status 0 - No life time counter interrupt pending 1 - Life time counter interrupt pending
3 CVMI	Current / Voltage measurement interrupt status 0 - No Current / Voltage measurement interrupt pending 1 - Current / Voltage measurement interrupt pending
2 RX	SCI receive interrupt status 0 - No SCI receive interrupt pending 1 - SCI receive interrupt pending
1 TX	SCI transmit interrupt status 0 - No SCI transmit interrupt pending 1 - SCI transmit interrupt pending
0 ERR	SCI error interrupt status 0 - No SCI transmit interrupt pending 1 - SCI transmit interrupt pending

5.7.3 Current and Voltage Measurement

To guarantee synchronous voltage and current acquisition, both channels are implemented equal in terms of digital signal conditioning and timing. The analog signal conditioning, before the Sigma Delta Converter, is different to match the different sources.

5.7.3.1 Shunt Sense, PGA, and GCB (Current Channel only)

Current Channel specific analog signal conditioning.

5.7.3.1.1 Shunt Sense

An optional current sense feature is implemented to sense the presence of the current shunt resistor. Setting the OPEN bit (ACQ_CTL register), will activate the feature. The OPEN bit (ACQ_SR register) will indicate the shunt resistor open.

The sense feature will detect an open condition for a shunt resistance R_{SHUNT} > ROPEN.

5.7.3.1.2 Programmable Gain Amplifier (PGA)

To allow a wide range of current levels to be measured, a programmable gain amplifier is implemented. Following the input chopper (see Section 5.7.3.5, “IIR / Decimation / Chopping Stage"), the differential voltage is amplified by one of the 8 gains controlled by the Gain Control Block.

The PGA has an internal offset compensation feature - see Section 5.7.4.1, “Compensation" and Section 5.7.5, “Calibration" for details.

5.7.3.1.3 Gain Control Block (GCB)

To allow a transparent Gain adjustment with minimum MCU load, an automatic gain control has been implemented. The absolute output of the PGA is constantly compared with a programmable up and down threshold (ACQ_GCB register). The threshold is a D/A output according Table 100.

Table 100. Gain Control Block - Register

ACQ_GCB D[7:0]	GCB High (up) Threshold	ACQ_GCB D[7:0]	GCB Low (down) Threshold
0000xxxx	1/16 V_{REF}	xxxx0000	0
0001xxxx	2/16 V_{REF}	xxxx0001	1/16 V_{REF}
0010xxxx	3/16 V_{REF}	xxxx0010	2/16 V_{REF}
0011xxxx	4/16 V_{REF}	xxxx0011	3/16 V_{REF}
0100xxxx	5/16 V_{REF}	xxxx0100	4/16 V_{REF}
0101xxxx	6/16 V_{REF}	xxxx0101	5/16 V_{REF}
0110xxxx	7/16 V_{REF}	xxxx0110	6/16 V_{REF}
0111xxxx	8/16 V_{REF}	xxxx0111	7/16 V_{REF}
1000xxxx	9/16 V_{REF}	xxxx1000	8/16 V_{REF}
1001xxxx	10/16 V_{REF}	xxxx1001	9/16 V_{REF}
1010xxxx	11/16 V_{REF}	xxxx1010	10/16 V_{REF}
1011xxxx	12/16 V_{REF}	xxxx1011	11/16 V_{REF}
1100xxxx	13/16 V_{REF}	xxxx1100	12/16 V_{REF}
1101xxxx	14/16 V_{REF}	xxxx1101	13/16 V_{REF}
1110xxxx	15/16 V_{REF}	xxxx1110	14/16 V_{REF}
1111xxxx	16/16 V_{REF}	xxxx1111	15/16 V_{REF}

Once the programmed threshold is reached, the gain is adjusted to the next level. The currently active gain setting can be read in the IGAIN[2:0] register. Once the gain has been adjusted by the GCB, the PGAG bit will be set.

5.9.3.3.6 Timer System Control Register 1 (TSCR1)

Table 201. Timer System Control Register 1 (TSCR1)

Offset[180] 0x26 — Access: User read/write

	7	6	5	4	3	2	1	0
R	TEN	0	0	TFFCA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Notes
180.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 202. TSCR1 - Register Field Descriptions

Field	Description
7 TEN	Timer Enable 1 = Enables the timer. 0 = Disables the timer. (Used for reducing power consumption).
4 TFFCA	Timer Fast Flag Clear All 1 = For TFLG1 register, a read from an input capture or a write to the output compare channel [TC 3:0] causes the corresponding channel flag, CnF, to be cleared. For TFLG2 register, any access to the TCNT register clears the TOF flag. This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses. 0 = Allows the timer flag clearing.

5.9.3.3.7 Timer Toggle On Overflow Register 1 (TTOV)

Table 203. Timer Toggle On Overflow Register 1 (TTOV)

Offset[181] 0x27 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	TOV3	TOV2	TOV1	TOV0
W								
Reset	0	0	0	0	0	0	0	0

Notes
181.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 204. TTOV - Register Field Descriptions

Field	Description
3-0 TOV[3-0]	Toggle On Overflow Bits 1 = Toggle output compare pin on overflow feature enabled. 0 = Toggle output compare pin on overflow feature disabled.

NOTE

TOVn toggles the output compare pin on overflow. This feature only takes effect when the corresponding channel is configured for an output compare mode. When set, an overflow toggle on the output compare pin takes precedence over forced output compare events.

5.9.3.3.13 Main Timer Interrupt Flag 2 (TFLG2)

Table 218. Main Timer Interrupt Flag 2 (TFLG2)

Offset[188] 0x2D — Access: User read/write

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Notes
188.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 219. TFLG2 - Register Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag 1 = Indicates that an interrupt has occurred (Set when 16-bit free-running timer counter overflows from $FFFF to $0000) 0 = Flag indicates an interrupt has not occurred.

NOTE

The TFLG2 register indicates when an interrupt has occurred. Writing a one to the TOF bit will clear it. Any access to TCNT will clear TOF bit of TFLG2 register if the TFFCA bit in TSCR register is set.

5.9.3.3.14 Timer Input Capture/Output Compare Registers (TC3 - TC0)

Table 220. Timer Input Capture/Output Compare Register 0 (TC0)

Offset[189] 0x2E, 0x2F — Access: User read/write

	15	14	13	12	11	10	9	8
R W	tc0_15	tc0_14	tc0_13	tc0_12	tc0_11	tc0_10	tc0_9	tc0_8
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R W	tc0_7	tc0_6	tc0_5	tc0_4	tc0_3	tc0_2	tc0_1	tc0_0
Reset	0	0	0	0	0	0	0	0

Notes
189.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 310. Interrupt Vector Base Register (IVBR)

Address: 0x001F

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Read: Anytime.
Write: Anytime.

Table 311. IVBR Field Descriptions

Field	Description
7–0 IVB_ADDR[7:0]	**Interrupt Vector Base Address Bits** — These bits represent the upper byte of all vector addresses. Out of reset, these bits are set to 0xFF (i.e., vectors are located at 0xFF80–0xFFFE) to ensure compatibility to HCS12. **Note:** A system reset will initialize the interrupt vector base register with “0xFF” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the three reset vectors (0xFFFA–0xFFFE). **Note:** If the BDM is active (i.e., the CPU is in the process of executing BDM firmware code), the contents of IVBR are ignored and the upper byte of the vector address is fixed as “0xFF”. This is done to enable handling of all non-maskable interrupts in the BDM firmware.

5.17.4 Functional Description

The INT module processes all exception requests to be serviced by the CPU module. These exceptions include interrupt vector requests and reset vector requests. Each of these exception types and their overall priority level is discussed in the following subsections.

5.17.4.1 S12S Exception Requests

The CPU handles both reset requests and interrupt requests. A priority decoder is used to evaluate the priority of pending interrupt requests.

5.17.4.2 Interrupt Prioritization

The INT module contains a priority decoder to determine the priority for all interrupt requests pending for the CPU. If more than one interrupt request is pending, the interrupt request with the higher vector address wins the prioritization.

The following conditions must be met for an I bit maskable interrupt request to be processed.

1. The local interrupt enabled bit in the peripheral module must be set.
2. The I bit in the condition code register (CCR) of the CPU must be cleared.
3. There is no SWI, TRAP, or X bit maskable request pending.

NOTE

All non I bit maskable interrupt requests always have higher priority than the I bit maskable interrupt requests. If the X bit in the CCR is cleared, it is possible to interrupt an I bit maskable interrupt by an X bit maskable interrupt. It is possible to nest non maskable interrupt requests, e.g., by nesting SWI or TRAP calls.

Since an interrupt vector is only supplied at the time when the CPU requests it, it is possible that a higher priority interrupt request could override the original interrupt request that caused the CPU to request the vector. In this case, the CPU will receive the highest priority vector and the system will process this interrupt request first, before the original interrupt request is processed.

If the interrupt source is unknown (for example, in the case where an interrupt request becomes inactive after the interrupt has been recognized, but prior to the CPU vector request), the vector address supplied to the CPU will default to that of the spurious interrupt vector.

5.19.3.2.3 Debug Trace Control Register (DBGTCR)

Table 331. Debug Trace Control Register (DBGTCR)

Address: 0x0022

	7	6	5	4	3	2	1	0
R	0	TSOURCE	0	0	TRCMOD		0	TALIGN
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime
Write: Bit 6 only when DBG is neither secure nor armed.Bits 3,2,0 anytime the module is disarmed.

Table 332. DBGTCR Field Descriptions

Field	Description
6 TSOURCE	**Trace Source Control Bit** — The TSOURCE bit enables a tracing session given a trigger condition. If the MCU system is secured, this bit cannot be set and tracing is inhibited. This bit must be set to read the trace buffer. 0 Debug session without tracing requested 1 Debug session with tracing requested
3–2 TRCMOD	**Trace Mode Bits** — See Section 5.19.4.5.2, “Trace Modes" for detailed Trace mode descriptions. In Normal mode, change of flow information is stored. In Loop1 mode, change of flow information is stored but redundant entries into trace memory are inhibited. In Detail mode, address and data for all memory and register accesses is stored. In Compressed Pure PC mode the program counter value for each instruction executed is stored. See Table 333.
0 TALIGN	**Trigger Align Bit** — This bit controls whether the trigger is aligned to the beginning or end of a tracing session. 0 Trigger at end of stored data 1 Trigger before storing data

Table 333. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1
10	Detail
11	Compressed Pure PC

5.19.3.2.4 Debug Control Register2 (DBGC2)

Table 334. Debug Control Register2 (DBGC2)

Address: 0x0023

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	ABCM	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime
Write: Anytime the module is disarmed

This register configures the comparators for range matching.

If no taghit points to Final state, then the lowest channel number has priority. With the above encoding from State3, the CPU and DBG would break on a simultaneous M0/M2.

5.19.5.6 Scenario 5

Trigger if following event A, event C precedes event B. i.e... the expected execution flow is A->B->C.

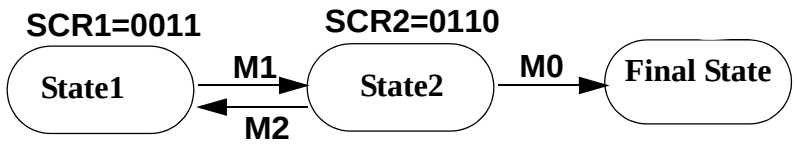


Figure 73. Scenario 5

Scenario 5 is possible with the S12SDBGV1 SCR encoding.

5.19.5.7 Scenario 6

Trigger if event A occurs twice in succession before any of 2 other events (BC) occur. This scenario is not possible using the S12SDBGV1 SCR encoding. S12SDBGV2 includes additions shown in red. The change in SCR1 encoding also has the advantage that a State1->State3 transition using M0 is now possible. This is advantageous because range and data bus comparisons use channel 0 only.

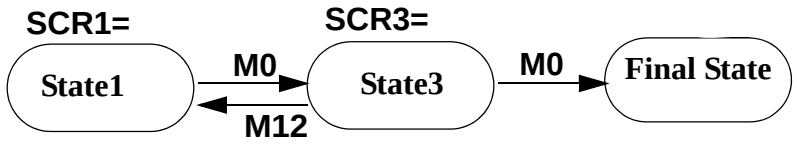


Figure 74. Scenario 6

5.19.5.8 Scenario 7

Trigger when a series of 3 events are executed out of order. Specifying the event order as M1, M2, M0 to run in loops (120120120). Any deviation from that order should trigger. This scenario is not possible using the S12SDBGV1 SCR encoding, because OR possibilities are very limited in the channel encoding. By adding OR forks as shown in red, this scenario is possible.

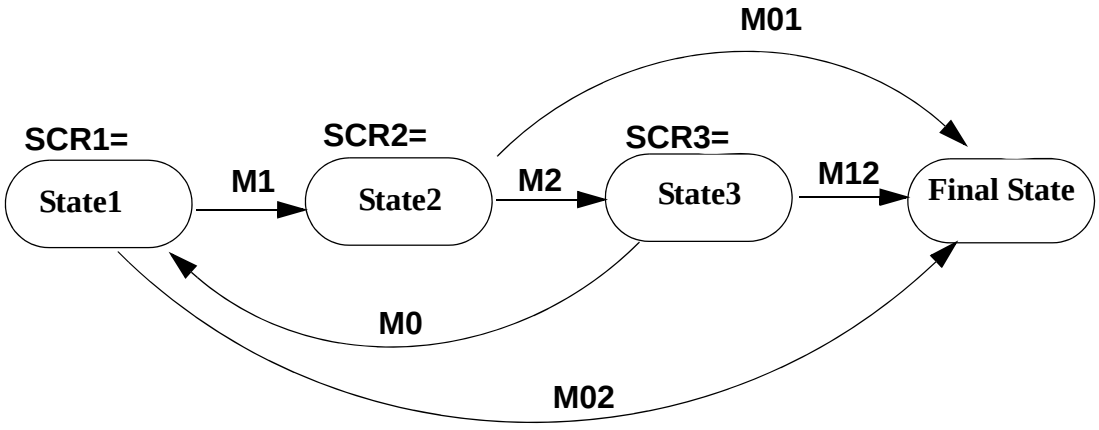


Figure 75. Scenario 7

5.21.4.10 Instruction Tracing

When a TRACE1 command is issued to the BDM in active BDM, the CPU exits the standard BDM firmware and executes a single instruction in the user code. Once this has occurred, the CPU is forced to return to the standard BDM firmware, the BDM is active, and ready to receive a new command. If the TRACE1 command is issued again, the next user instruction will be executed. This facilitates stepping or tracing through the user code one instruction at a time.

If an interrupt is pending when a TRACE1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. Once back in standard BDM firmware execution, the program counter points to the first instruction in the interrupt service routine.

Be aware when tracing through the user code that the execution of the user code is done step by step, but peripherals are free running. Hence possible timing relations between CPU code execution and occurrence of events of other peripherals no longer exist.

Do not trace the CPU instruction BGND used for soft breakpoints. Tracing over the BGND instruction will result in a return address pointing to BDM firmware address space.

When tracing through user code which contains stop or wait instructions the following will happen when the stop or wait instruction is traced:

The CPU enters stop or wait mode and the TRACE1 command can not be finished before leaving the low power mode. This is the case because BDM active mode can not be entered after the CPU executed the stop instruction. However, all BDM hardware commands except the BACKGROUND command are operational after tracing a stop or wait instruction, and still being in stop or wait mode. If system stop mode is entered (all bus masters are in stop mode), no BDM command is operational.

As soon as stop or wait mode is exited, the CPU enters BDM active mode and the saved PC value points to the entry of the corresponding interrupt service routine.

If the handshake feature is enabled, the corresponding ACK pulse of the TRACE1 command will be discarded when tracing a stop or wait instruction. Hence, there is no ACK pulse when BDM active mode is entered as part of the TRACE1 command, after CPU exited from stop or wait mode. All valid commands sent during CPU being in stop or wait mode or after CPU exited from stop or wait mode will have an ACK pulse. The handshake feature becomes disabled only when system stop mode has been reached. After a system stop mode, the handshake feature must be enabled again by sending the ACK_ENABLE command.

5.21.4.11 Serial Communication Timeout

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD, to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any timeout limit.

Consider now the case where the host returns BKGD to a logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge, marking the start of a new bit. If, a new falling edge is not detected by the target within 512 clock cycles, since the last falling edge, a timeout occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued, but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the timeout has occurred. This is expected behavior if the handshake protocol is not enabled. To allow the data to be retrieved, even with a large clock frequency mismatch (between BDM and CPU) when the hardware handshake protocol is enabled, the timeout between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles, and still be able to retrieve the data from an issued read command. However, once the handshake pulse (ACK pulse) is issued, the timeout feature is re-activated, meaning that the target will timeout after 512 clock cycles. The host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any negative edge in the BKGD pin after the timeout period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data has occurred, the timeout in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next negative edge in the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

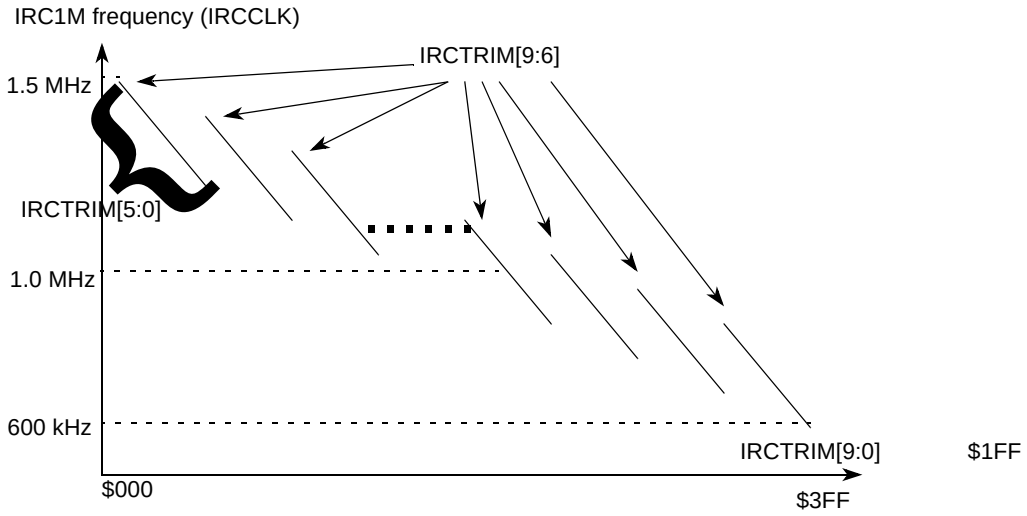


Figure 92. IRC1M Frequency Trimming Diagram

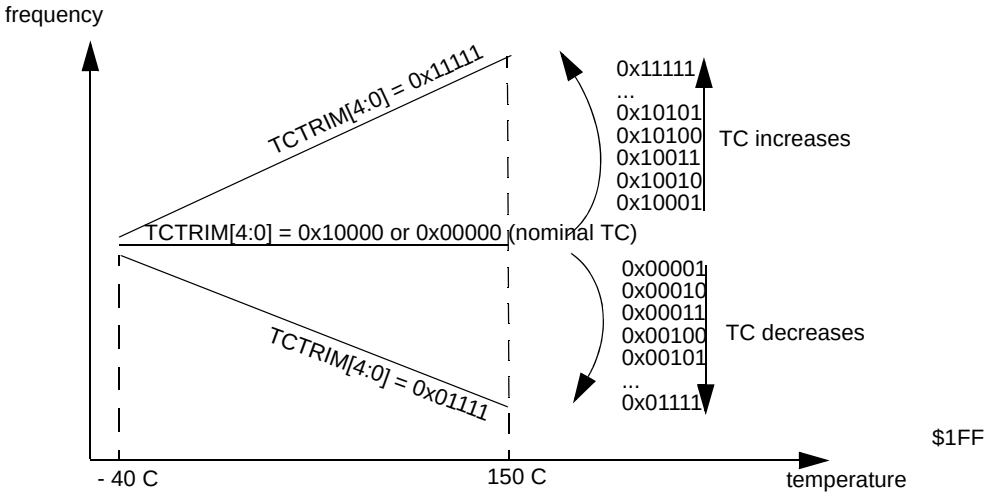


Figure 93. Influence of TCTRIM[4:0] on the Temperature Coefficient

NOTE

The frequency is not necessarily linear with the temperature (in most cases it will not be). The above diagram is meant only to give the direction (positive or negative) of the variation of the TC, relative to the nominal TC.

Setting TCTRIM[4:0] at 0x00000 or 0x10000 does not mean that the temperature coefficient will be zero. These two combinations basically switch off the TC compensation module, which result in the nominal TC of the IRC1M.

Table 433. TC Trimming of the Frequency of the IRC1M

TCTRIM[4:0]	IRC1M indicative relative TC variation	IRC1M indicative frequency drift for relative TC variation
00000	0 (nominal TC of the IRC)	0%
00001	-0.27%	-0.5%
00010	-0.54%	-0.9%

5.22.4.2 Startup from Reset

An example of startup of clock system from Reset is given in Figure 94.

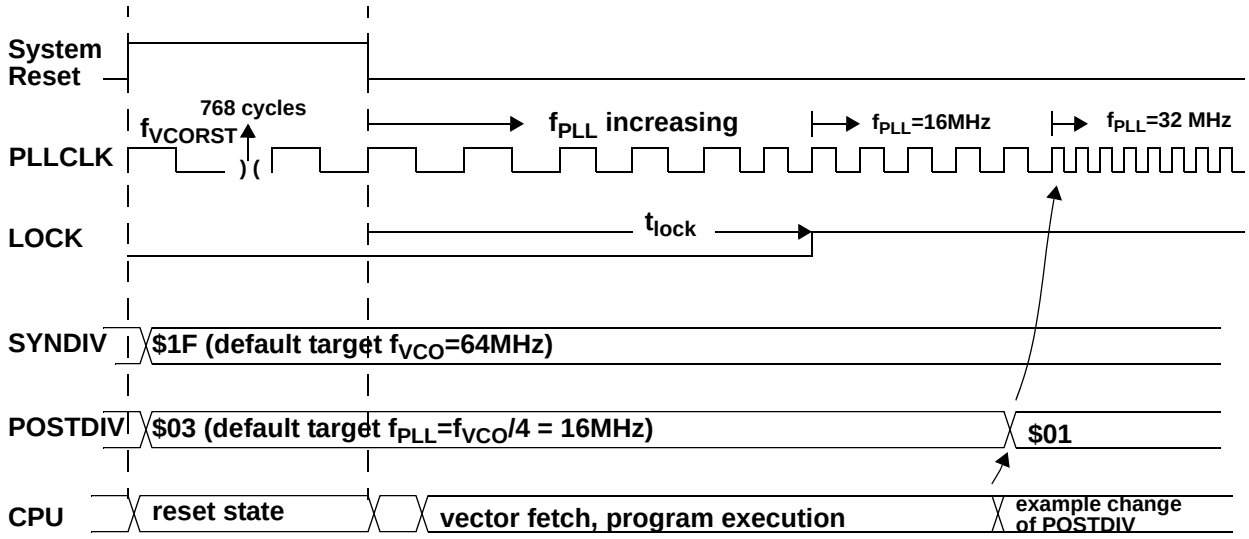


Figure 94. Startup of Clock System After Reset

5.22.4.3 Stop Mode using PLLCLK as Bus Clock

An example of what happens going into Stop mode and exiting Stop mode after an interrupt is shown in Figure 95. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop mode.

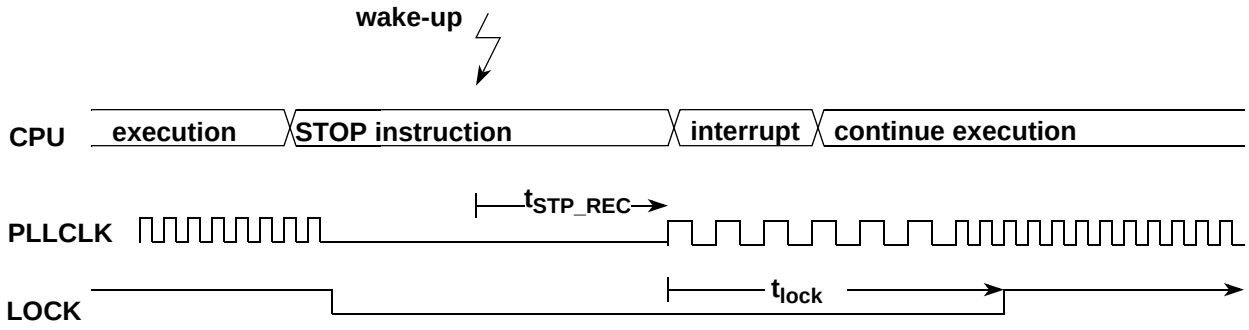


Figure 95. Stop Mode using PLLCLK as Bus Clock

5.22.4.4 Full Stop Mode Using Oscillator Clock as Bus Clock

An example of what happens going into Full Stop mode and exiting Full Stop mode after an interrupt is shown in Figure 96. Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop mode.

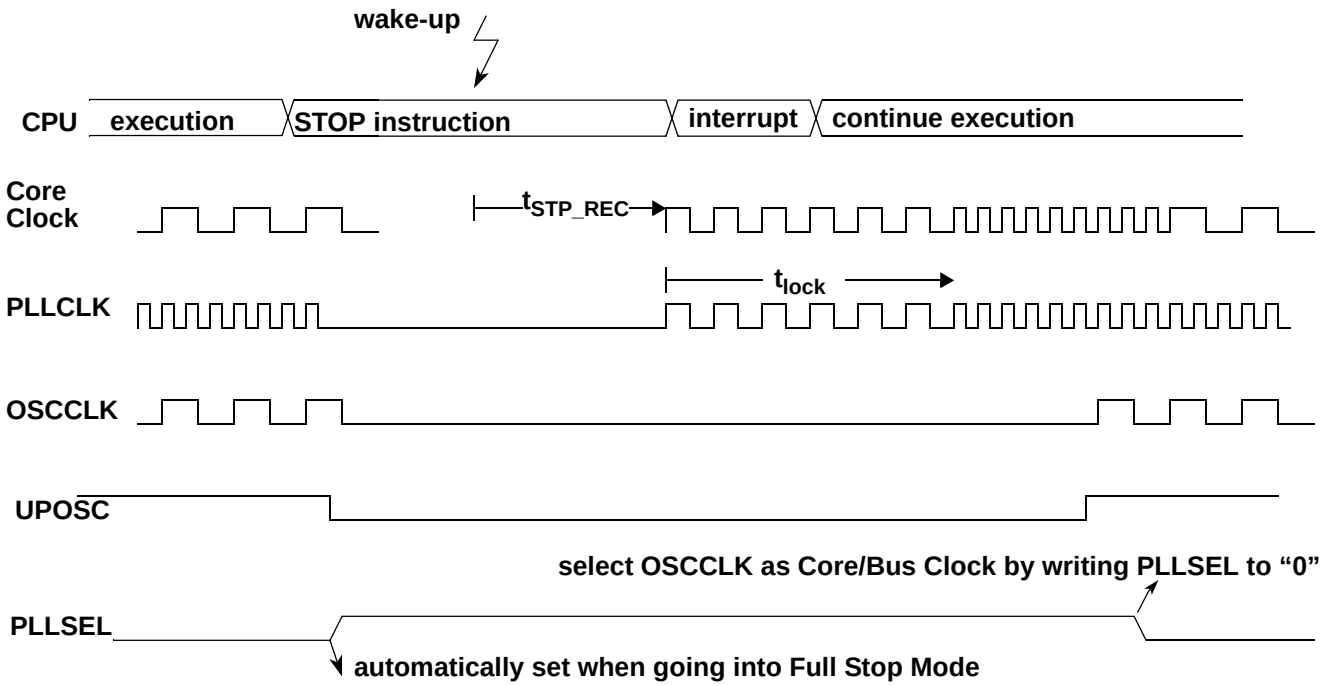


Figure 96. Full Stop Mode Using Oscillator Clock as Bus Clock

5.22.4.5 External Oscillator

5.22.4.5.1 Enabling the External Oscillator

An example of how to use the oscillator as Bus Clock is shown in Figure 97.

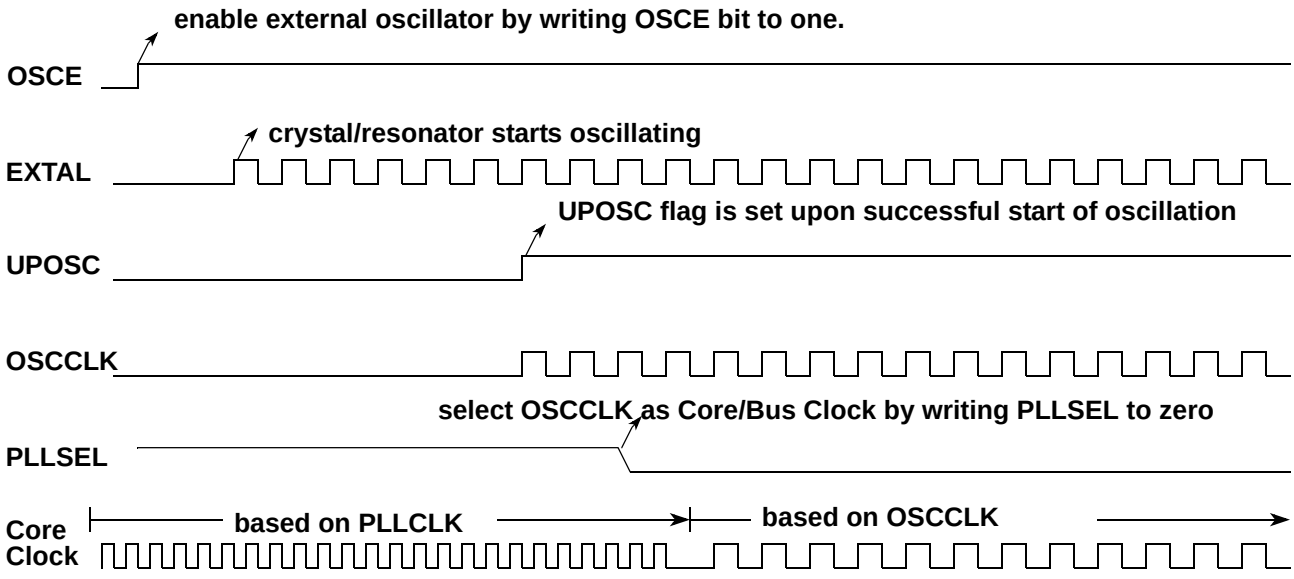


Figure 97. Enabling the external oscillator

5.23.3.2.2 SPI Control Register 2 (SPICR2)

Table 449. SPI Control Register 2 (SPICR2)

0x00E9

	7	6	5	4	3	2	1	0
R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 450. SPICR2 Field Descriptions

Field	Description
6 XFRW	**Transfer Width —** This bit is used for selecting the data transfer width. If 8-bit transfer width is selected, SPIDRL becomes the dedicated data register and SPIDRH is unused. If 16-bit transfer width is selected, SPIDRH and SPIDRL form a 16-bit data register. Refer to Section 5.23.3.2.4, “SPI Status Register (SPISR)" for information about transmit/receive data handling and the interrupt flag clearing mechanism. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 8-bit Transfer Width (n = 8)(269) 1 16-bit Transfer Width (n = 16)(269)
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure to be detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration, refer to Table 448. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI. 1 $\overline{SS}$ port pin with MODF feature.
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode, this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled. 1 Output buffer enabled.
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode. 1 Stop SPI clock generation when in wait mode.
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 451. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.

Notes

269.n is used later in this document as a placeholder for the selected transfer width.

Table 451. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In

5.24.1.2 Features

5.24.1.2.1 P-Flash Features

- 128 kbytes of P-Flash memory composed of one 128 kbyte Flash block divided into 256 sectors of 512-bytes
- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the D-Flash memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

5.24.1.2.2 D-Flash Features

- 4.0 kbytes of D-Flash memory composed of one 4.0 kbyte Flash block divided into 16 sectors of 256-bytes
- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of D-Flash memory
- Ability to program up to four words in a burst sequence

5.24.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

5.24.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 109.

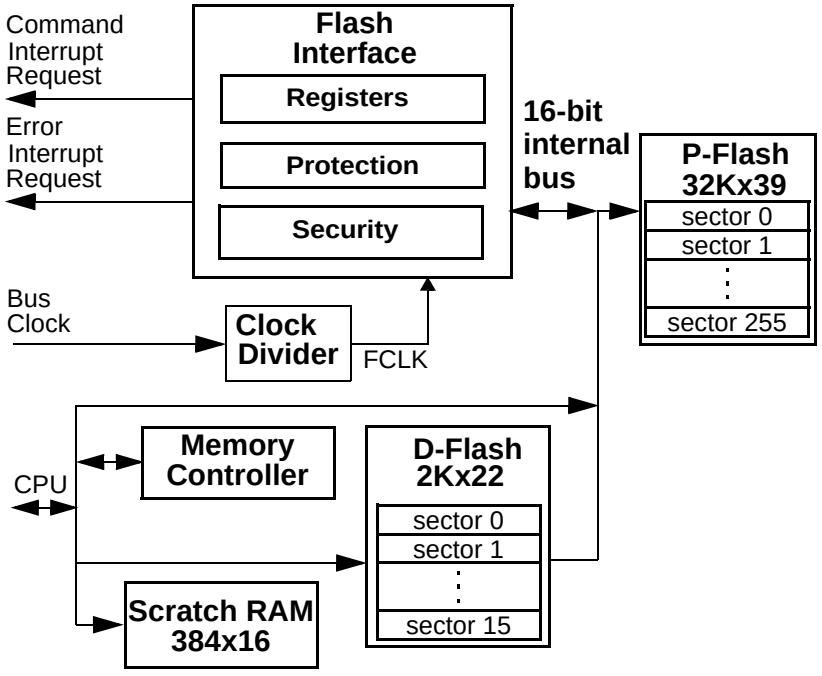
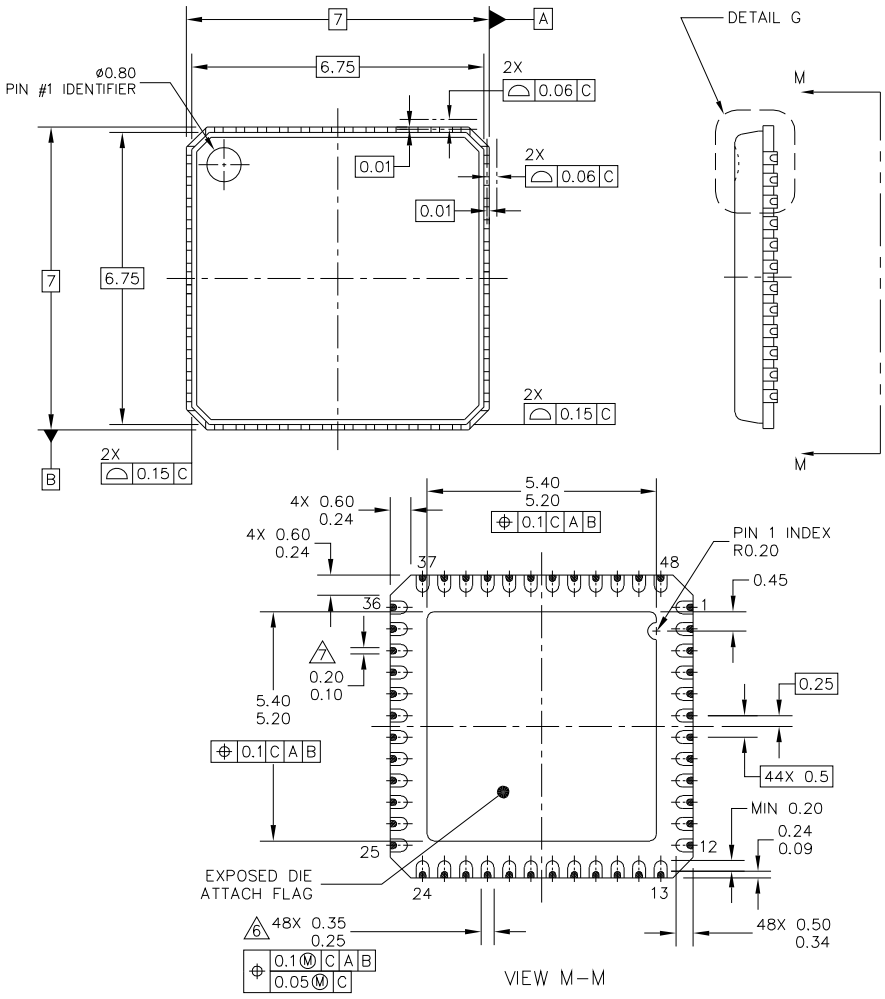


Figure 109. FTMRC128K1 Block Diagram

7 Packaging

7.1 Package dimensions

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED PUNCH QUAD FLAT NON–LEADED (QFN) PACKAGE WITH WETTABLE FLANKS 48 TERMINAL, 7 X 7 X 0.85, 0.5 PITCH	DOCUMENT NO: 98ASA00343D	REV: A
	CASE NUMBER: 2095–01	13 JUL 2011
	STANDARD: NON–JEDEC	

EP SUFFIX
48 PIN QFN
QFN48LD-EP
REVISION D