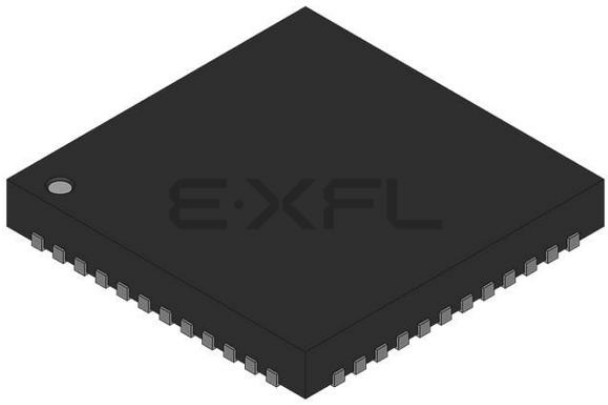

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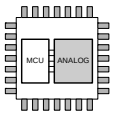
Details	
Product Status	Active
Applications	Battery Monitor
Core Processor	S12
Program Memory Type	FLASH (96KB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI, SPI
Number of I/O	8
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mm912i637av1ep

Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
3	PE1/XTAL	MCU Oscillator	XTAL is one of the optional crystal/resonator drivers and external clock pins, and the PE1 port may be used as a general purpose I/O. On reset all the device clocks are derived from the internal reference clock. See Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)".
4	TEST	MCU Test	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to VSSRX in user mode.
5	PA5	MCU PA5	General purpose port A input or output pin 5. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
6	PA4	MCU PA4	General purpose port A input or output pin 4. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
7	PA3	MCU PA3 / $\overline{SS}$	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
8	PA2	MCU PA2 / SCK	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
9	PA1	MCU PA1 / MOSI	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
10	PA0	MCU PA0 / MISO	General purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI interface. See Section 5.16, “MCU - Port Integration Module (9S12I128PIMV1)".
11	VSSRX	MCU 5.0 V Ground	External ground for the MCU - VDDRX return path.
12	VDDRX	MCU 5.0 V Supply	5.0 V MCU power supply. MCU core- (internal 1.8 V regulator) and flash (internal 2.7 V regulator) supply.
13	VSSD2D	MCU 2.5 V Ground	External ground for the MCU - VDDD2D return path.
14	VDDD2D	MCU 2.5 V Supply	2.5 V MCU power supply. Die to die buffer supply.
15	NC	Not connected	This pin must be grounded in the application.
16	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
17	VDDX	Voltage Regulator Output 5.0 V	5.0 V main voltage regulator output pin. An external capacitor (C_{VDDX}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
18	DGND	Digital Ground	This pin is the device digital ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
19	VDDH	Voltage Regulator Output 2.5 V	2.5 V high power main voltage regulator output pin to be connected with the VDDD2D MCU pin. An external capacitor (C_{VDDH}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
20	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
21	VSUP	Power Supply	This pin is the device power supply pin. A reverse battery protection diode is required. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
22	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See Section 5.11, “LIN".
23	LGND	LIN Ground Pin	This pin is the device LIN ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
24	NC	Not connected (reserved)	This pin must be grounded in the application.
25	NC	Not connected	This pin must be grounded in the application.
26	VDDA	Analog Voltage Regulator Output	Low power analog voltage regulator output pin, permanently supplies the analog front end. An external capacitor (C_{VDDA}) is needed. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
27	AGND	Analog Ground	This pin is the device analog voltage regulator and LP oscillator ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".

5 Functional Description and Application Information

This chapter describes the MM912_637 dual die device functions on a block by block base. The following symbols are shown on all module cover pages to distinguish between the module location being the MCU die or the analog die:



The documented module is physically located on the Analog die. This applies to Section 5.1, “MM912_637 - Analog Die Overview" through Section 5.14, “Die to Die Interface - Target".

The documented module is physically located on the Microcontroller die. This applies to Section 5.1, “MM912_637 - Analog Die Overview" through Section 5.25, “MCU - Die-to-Die Initiator (D2DIV1)".

Sections concerning both die or the complete device will not have a specific indication (e.g. Section 6, “MM912_637 - Trimming").

5.0.1 Introduction

Many types of electronic control units (ECUs) are connected to and supplied from the main car battery in modern cars. Depending on the cars mode of operation (drive, start, stop, standby), the battery must deliver different currents to the different ECUs. The vehicle power management has several sub-functions, like control of the set-point value of the power generator, dynamic load management during drive, start, stop, and standby mode.

The Application Specific Integrated Circuit (ASIC) allows for two application circuits, depending on whether the bias current of the MM912_637 itself shall be included into the current measurement.

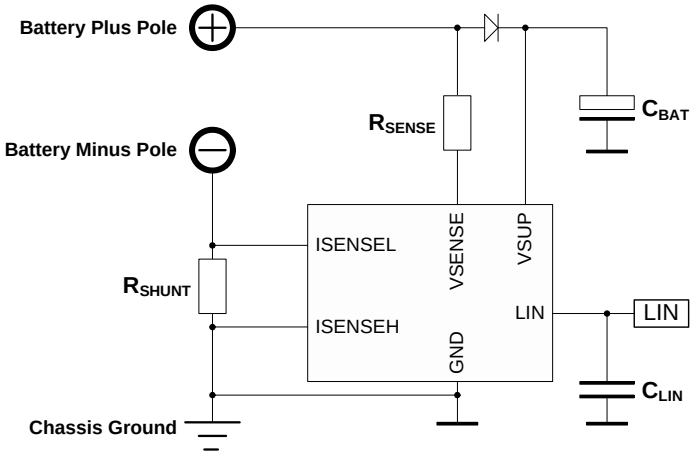


Figure 12. Typical IBS Application (Device GND = Chassis GND)

Table 97. Interrupt Mask Register (INT_MSK (hi)) - Register Field Descriptions

Field	Description
7 TOVM	Timer overflow interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
6 CH3M	Timer channel 3 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
5 CH2M	Timer channel 2 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 CH1M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CH0M	Timer channel 1 interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
2 LTIM	LIN driver over-temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
1 HTIM	High temperature interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
0 UVIM	Under-voltage interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

5.3.5.3.5 Interrupt Mask Register (INT_MSK (lo))

Table 98. Interrupt mask register (INT_MSK (lo))

Offset[104] 0x0D — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	CALM	LTCM	CVMM	RXM	TXM	ERRM
W								
Reset	0	0	0	0	0	0	0	0

Notes
104.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 99. Interrupt Mask Register (INT_MSK (lo)) - Register Field Descriptions

Field	Description
5 CALM	Calibration request interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
4 LTCM	Life time counter interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled
3 CVMM	Current / Voltage measurement interrupt mask 0 - Interrupt enabled 1 - Interrupt disabled

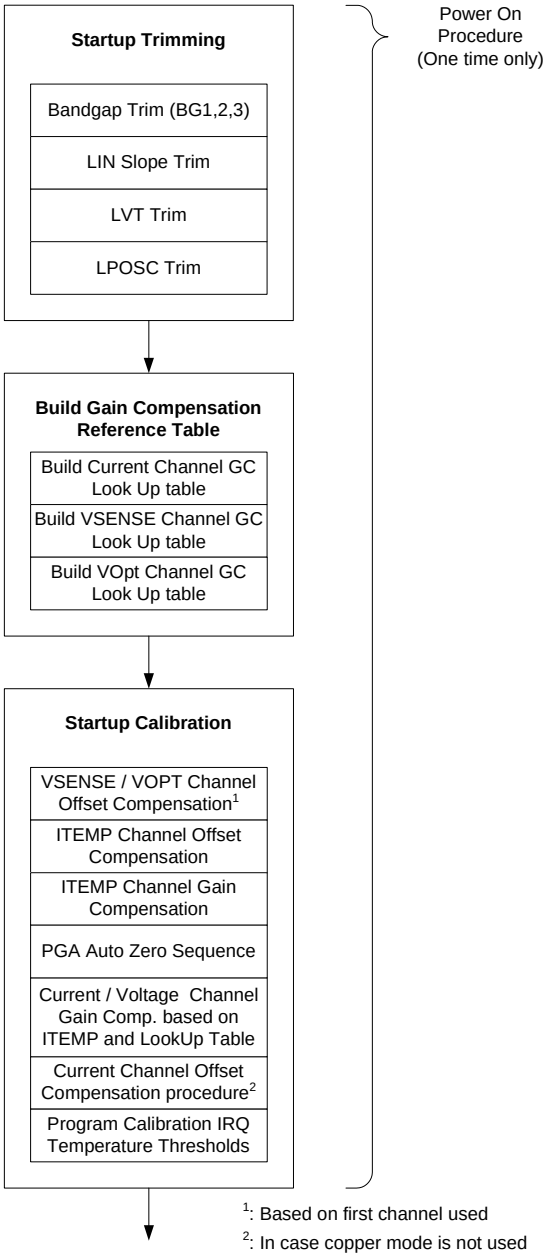


Figure 36. Power On Procedure

5.7.5.1.1 Startup Trimming

To ensure all analog die modules are being trimmed properly, the following FLASH information (located in the MCU IFR from 0x0_40D0 to 0x0_40D9) has to be copied to the analog die register 0xE0 to 0xE9. This trimming includes the Band Gap Reference adjustment for the 3 system Band Gap circuits, The LIN slope adjustment (TRIM_LIN), the Low Voltage Threshold (TRIM_LVT), and the Low Power Oscillator (TRIM_OSC). See Section 6, “MM912_637 - Trimming".

NOTE

The LPOSC[12:0] trim will adjust the low power oscillator to its specified accuracy. This will result in the dependent Watchdog timing to be accurate after writing the trimming information.

5.7.6.3.34 Internal Temp. Offset Compensation (COMP_ITO)

Table 175. Internal Temp. Offset Compensation (COMP_ITO)

Offset[160] 0xD0 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	ITOC[7:0]							
Reset	0	0	0	0	0	0	0	0

Notes
160.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 176. Internal Temp. Offset Compensation (COMP_ITO) - Register Field Descriptions

Field	Description
7-0 ITOC[7:0]	Internal Temperature Offset Compensation Buffer. This register contains the Internal Temperature Offset compensation as 8-bit signed char (two complement). Refer to Section 5.7.3.4, “Compensation" for details.

5.7.6.3.35 Internal Temp. Gain Compensation (COMP_ITG)

Table 177. Internal Temp. Gain Compensation (COMP_ITG)

Offset[161] 0xD1 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	ITGC[7:0]							
Reset	1	0	0	0	0	0	0	0

Notes
161.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 178. Internal Temp. Gain Compensation (COMP_ITG) - Register Field Descriptions

Field	Description
7-0 ITGC[7:0]	Internal Temperature Gain Compensation Buffer. This register contains the Internal Temperature Gain compensation as 8-bit special coded value. Refer to Section 5.7.3.4, “Compensation" for details.

5.7.6.3.36 External Temp. Offset Compensation (COMP_ETO)

Table 179. External Temp. Offset Compensation (COMP_ETO)

Offset[162] 0xD2 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	ETOC[7:0]							
Reset	0	0	0	0	0	0	0	0

Notes
162.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.8.1.3.1 Watchdog Control Register (WD_CTL)

Table 184. Watchdog Control Register (WD_CTL)

Offset (167),(168) 0x10 — Access: User write

	15	14	13	12	11	10	9	8
R	0	0	0	0	0	0	0	0
W	WDTSTM					WDTOM		
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R	WDTST	0	0	0	0	WDTO		
W								
Reset	1	0	0	0	0	1	0	0

Notes
167.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.
168.This Register is 16 Bit access only.

Table 185. Watchdog Control Register (WD_CTL) - Register Field Descriptions

Field	Description
15 WDTSTM	Watchdog Test - Mask 0 - writing the WDTST bit will have no effect 1 - writing the WDTST bit will be effective
10-8 WDTOM[2:0]	Watchdog Timeout - Mask 0 - writing the WDTO bits will have no effect 1 - writing the WDTO bits will be effective
7 WDTST	Watchdog Test This bit is implemented for test purpose and has no function in Normal mode.
2-0 WDTO[2:0]	Watchdog Timeout Configuration - configuring the watchdog timeout duration t_{WDTO}. 000 - Watchdog OFF 001 - 4.0 ms 010 - 16.0 ms 011 - 64.0 ms 100 - 256 ms (default) 101 - 512 ms 110 - 1024 ms 111 - 2048 ms

5.8.1.3.2 Watchdog status register (WD_SR)

Table 186. Watchdog Status Register (WD_SR)

Offset(169) 0x12 — Access: User read

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	WDOFF	WDWO
W								

Notes
169.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.11 LIN

5.11.1 Introduction

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer version 2.0 / 2.1 and J2602 specification, and has the following features:

- LIN physical layer 2.0 / 2.1 / J2602 compliant
- Slew rate selection 20 kBit, 10 kBit, and fast Mode (100 kBit)
- Over-temperature Shutdown - HTI
- Permanent Pull-up in Normal mode 30 kΩ, 1.0 MΩ in low power
- Current limitation
- Special J2602 compliant configuration
- Direct Rx / Tx access
- Optional external Rx / Tx access and routing to the TIMER Input through PTBx

The LIN driver is a low side MOSFET with current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

5.11.2 Overview

5.11.2.1 Block Diagram

Figure 44 shows the basic function of the LIN module.

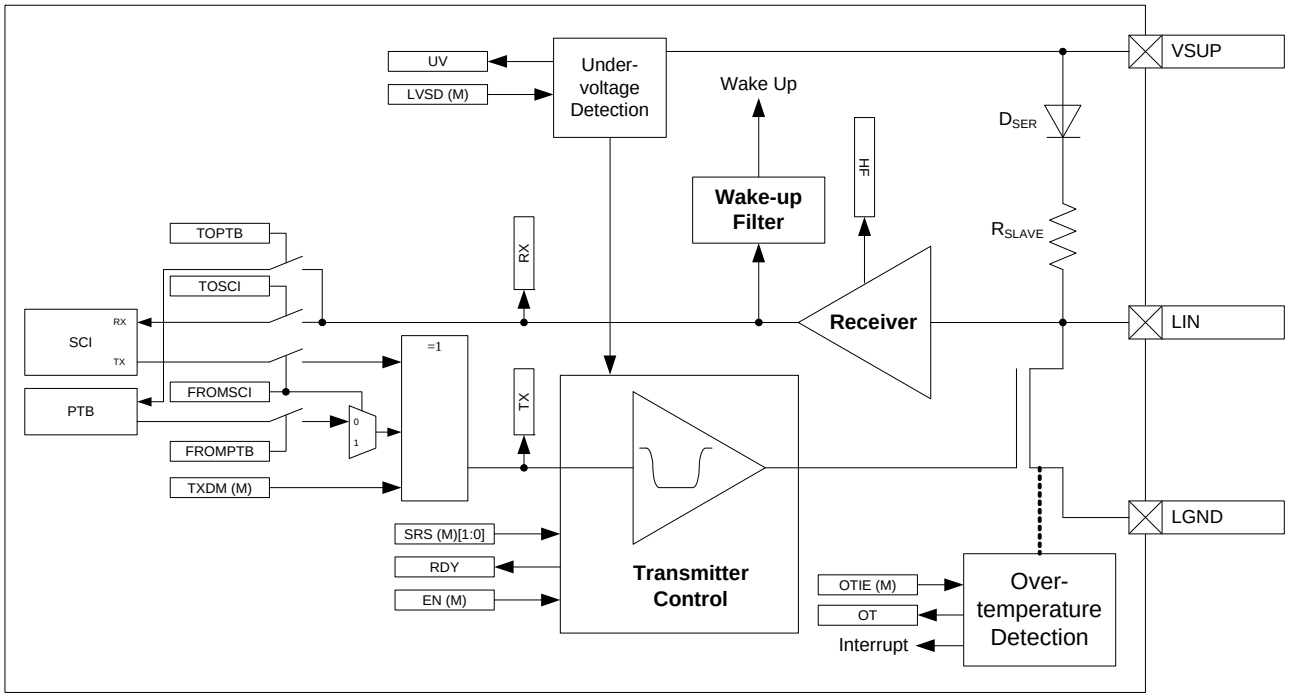


Figure 44. LIN Module Block Diagram

5.17.5.2 Interrupt Nesting

The interrupt request scheme makes it possible to nest I bit maskable interrupt requests handled by the CPU.

I bit maskable interrupt requests can be interrupted by an interrupt request with a higher priority.

I bit maskable interrupt requests cannot be interrupted by other I bit maskable interrupt requests per default. In order to make an interrupt service routine (ISR) interruptible, the ISR must explicitly clear the I bit in the CCR (CLI). After clearing the I bit, other I bit maskable interrupt requests can interrupt the current ISR.

An ISR of an interruptible I bit maskable interrupt request could basically look like this:

1. Service interrupt, e.g., clear interrupt flags, copy data, etc.
2. Clear I bit in the CCR by executing the instruction CLI (thus allowing other I bit maskable interrupt requests)
3. Process data
4. Return from interrupt by executing the instruction RTI

5.17.5.3 Wake-up from Stop or Wait Mode

5.17.5.3.1 CPU Wake-up from Stop or Wait Mode

Every I bit maskable interrupt request is capable of waking the MCU from Stop or Wait mode. To determine whether an I bit maskable interrupts is qualified to wake-up the CPU, the same conditions as in normal run mode are applied during Stop or Wait mode:

If the I bit in the CCR is set, all I bit maskable interrupts are masked from waking up the MCU.

Since there are no clocks running in Stop mode, only interrupts which can be asserted asynchronously can wake-up the MCU from Stop mode.

NOTE

The only asynchronously asserted, I bit maskable interrupt for the MM912_637 would be the “D2D External Interrupt”.

The X bit maskable interrupt request can wake-up the MCU from Stop or Wait mode at anytime, even if the X bit in CCR is set.

If the X bit maskable interrupt request is used to wake-up the MCU with the X bit in the CCR set, the associated ISR is not called. The CPU then resumes program execution with the instruction following the WAI or STOP instruction. This features works the same rules as with any interrupt request, i.e. care must be taken that the X interrupt request used for wake-up remains active at least until the system begins execution of the instruction following the WAI or STOP instruction; otherwise, wake-up may not occur.

NOTE

The only X bit maskable interrupt for the MM912_637 would be the D2D Error Interrupt. As the D2D Initiator module is not active during STOP and WAIT mode, no X bit maskable interrupt source is existing for the MM912_637.

5.19.3.2.3 Debug Trace Control Register (DBGTCR)

Table 331. Debug Trace Control Register (DBGTCR)

Address: 0x0022

	7	6	5	4	3	2	1	0
R	0	TSOURCE	0	0	TRCMOD		0	TALIGN
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime
Write: Bit 6 only when DBG is neither secure nor armed.Bits 3,2,0 anytime the module is disarmed.

Table 332. DBGTCR Field Descriptions

Field	Description
6 TSOURCE	**Trace Source Control Bit** — The TSOURCE bit enables a tracing session given a trigger condition. If the MCU system is secured, this bit cannot be set and tracing is inhibited. This bit must be set to read the trace buffer. 0 Debug session without tracing requested 1 Debug session with tracing requested
3–2 TRCMOD	**Trace Mode Bits** — See Section 5.19.4.5.2, “Trace Modes" for detailed Trace mode descriptions. In Normal mode, change of flow information is stored. In Loop1 mode, change of flow information is stored but redundant entries into trace memory are inhibited. In Detail mode, address and data for all memory and register accesses is stored. In Compressed Pure PC mode the program counter value for each instruction executed is stored. See Table 333.
0 TALIGN	**Trigger Align Bit** — This bit controls whether the trigger is aligned to the beginning or end of a tracing session. 0 Trigger at end of stored data 1 Trigger before storing data

Table 333. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1
10	Detail
11	Compressed Pure PC

5.19.3.2.4 Debug Control Register2 (DBGC2)

Table 334. Debug Control Register2 (DBGC2)

Address: 0x0023

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	ABCM	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime
Write: Anytime the module is disarmed

This register configures the comparators for range matching.

Table 361. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator compares the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

5.19.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Table 362. Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Read: Anytime. See Table 360 for visible register encoding.
Write: If DBG not armed. See Table 360 for visible register encoding.

Table 363. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

5.19.3.2.8.4 Debug Comparator Address Low Register (DBGXAL)

Table 364. Debug Comparator Address Low Register (DBGXAL)

Address: 0x002B

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: Anytime. See **Table** for visible register encoding
Write: If DBG not armed. See **Table** for visible register encoding

Table 365. DBGXAL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Address Low Compare Bits** — The Comparator address low compare bits control whether the selected comparator compares the address bus bits [7:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

5.19.3.2.8.7 Debug Comparator Data High Mask Register (DBGADHM)

Table 370. Debug Comparator Data High Mask Register (DBGADHM)

Address: 0x002E

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00
Write: If COMRV[1:0] = 00 and DBG not armed

Table 371. DBGADHM Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Mask Bits** — The Comparator data high mask bits control whether the selected comparator compares the data bus bits [15:8] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit Any value of corresponding data bit allows match. 1 Compare corresponding data bit

5.19.3.2.8.8 Debug Comparator Data Low Mask Register (DBGADLM)

Table 372. Debug Comparator Data Low Mask Register (DBGADLM)

Address: 0x002F

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00
Write: If COMRV[1:0] = 00 and DBG not armed

Table 373. DBGADLM Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Mask Bits** — The Comparator data low mask bits control whether the selected comparator compares the data bus bits [7:0] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit. Any value of corresponding data bit allows match 1 Compare corresponding data bit

5.19.4 Functional Description

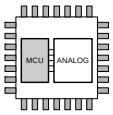
This section provides a complete functional description of the DBG module. If the part is in secure mode, the DBG module can generate breakpoints, but tracing is not possible.

5.19.4.1 S12SDBG Operation

Arming the DBG module by setting ARM in DBGC1 allows triggering the state sequencer, storing of data in the trace buffer, and generation of breakpoints to the CPU. The DBG module is made up of four main blocks, the comparators, control logic, the state sequencer, and the trace buffer.

The comparators monitor the bus activity of the CPU. All comparators can be configured to monitor address bus activity. Comparator A can also be configured to monitor data bus activity and mask out individual data bus bits during a compare.

5.20 MCU - Security (S12XS9SECV2)



5.20.1 Introduction

This specification describes the function of the security mechanism in the S12I chip family (9SEC).

NOTE

No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH and/or EEPROM difficult for unauthorized users.

5.20.1.1 Features

The user must be reminded that part of the security must lie with the application code. An extreme example would be application code that dumps the contents of the internal memory. This would defeat the purpose of security. At the same time, the user may also wish to put a backdoor in the application program. An example of this is the user downloads a security key through the SCI, which allows access to a programming routine that updates parameters stored in another section of the Flash memory.

The security features of the S12I chip family (in secure mode) are:

- Protect the content of non-volatile memories (Flash, EEPROM)
- Execution of NVM commands is restricted
- Disable access to internal memory via background debug module (BDM)

5.20.1.2 Modes of Operation

Table 388 gives an overview over availability of security relevant features in unsecure and secure modes.

Table 388. Feature Availability in Unsecure and Secure Modes on S12XS

	Unsecure Mode						Secure Mode					
	NS	SS	NX	ES	EX	ST	NS	SS	NX	ES	EX	ST
Flash Array Access	4	4					4	4				
EEPROM Array Access	4	4					4	4				
NVM Commands	(254)	4					(254)	(254)				
BDM	4	4					—	(255)				
DBG Module Trace	4	4					—	—				

Notes

254.Restricted NVM command set only. Refer to the NVM wrapper block guides for detailed information.

255.BDM hardware commands restricted to peripheral registers only.

5.20.1.3 Securing the Microcontroller

Once the user has programmed the Flash and EEPROM, the chip can be secured by programming the security bits located in the options/security byte in the Flash memory array. These non-volatile bits will keep the device secured through reset and power-down.

The options/security byte is located at address 0xFF0F (= global address 0x7F_FF0F) in the Flash memory array. This byte can be erased and programmed like any other Flash location. Two bits of this byte are used for security (SEC[1:0]). On devices which have a memory page window, the Flash options/security byte is also available at address 0xBF0F by selecting page 0x3F with the PPAGE register. The contents of this byte are copied into the Flash security register (FSEC) during a reset sequence.

Table 389. Flash Options/Security Byte

	7	6	5	4	3	2	1	0
0xFF0F	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0

5.22.3.2.16 S12CPMU Oscillator Register (CPMUOSC)

This register configures the external oscillator (OSCLCP).

Table 434. S12CPMU Oscillator Register (CPMUOSC)

0x02FA

	7	6	5	4	3	2	1	0
R	OSCE	OSCBW	OSCPINS_EN	OSCFILT[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), else write has no effect.

NOTE.

Write to this register clears the LOCK and UPOSC status bits.

NOTE.

If the chosen VCOCLK-to-OSCCLK ratio divided by two ((f_{VCO} / f_{OSC})/2) is not an integer number, the filter can not be used and the OSCFILT[4:0] bits must be set to 0.

NOTE

The frequency modulation (FM1 and FM0) can not be used if the Adaptive Oscillator Filter is enabled.

Table 435. CPMUOSC Field Descriptions

Field	Description
7 OSCE	**Oscillator Enable Bit** — This bit enables the external oscillator (OSCLCP). The UPOSC status bit in the CPMUFLG register indicates when the oscillation is stable and OSCCLK can be selected as bus clock or source of the COP or RTI. A loss of oscillation will lead to a clock monitor reset. 0 External oscillator is disabled. REFCLK for PLL is IRCCLK. 1 External oscillator is enabled.Clock monitor is enabled. REFCLK for PLL is external oscillator clock divided by REFDIV. **Note:** When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup time of the external oscillator t_{UPOSC} before entering Pseudo Stop mode.
6 OSCBW	**Oscillator Filter Bandwidth Bit** — If the VCOCLK frequency exceeds 25 MHz wide bandwidth must be selected. The Oscillator Filter is described in more detail in Section 5.22.4.5.2, “The Adaptive Oscillator Filter" 0 Oscillator filter bandwidth is narrow (window for expected OSCCLK edge is one VCOCLK cycle). 1 Oscillator filter bandwidth is wide (window for expected OSCCLK edge is three VCOCLK cycles).
5 OSCPINS_EN	Oscillator Pins EXTAL and XTAL Enable Bit If OSCE=1 this read-only bit is set. It can only be cleared with the next reset. Enabling the external oscillator reserves the EXTAL and XTAL pins exclusively for oscillator application. 0 EXTAL and XTAL pins are not reserved for oscillator. 1 EXTAL and XTAL pins exclusively reserved for oscillator.
4-0 OSCFILT	**Oscillator Filter Bits** — When using the oscillator a noise filter can be enabled, which filters noise from the incoming external oscillator clock and detects if the external oscillator clock is qualified or not (quality status shown by bit UPOSC). The VCOCLK-to-OSCCLK ratio divided by two ((f_{VCO} / f_{OSC})/2) must be an integer value. This value must be written to the OSCFILT[4:0] bits to enable the Adaptive Oscillator Filter. 0x0000 Adaptive Oscillator Filter disabled, else Adaptive Oscillator Filter enabled]

Table 451. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

5.23.3.2.3 SPI Baud Rate Register (SPIBR)

Table 452. SPI Baud Rate Register (SPIBR)

0x00EA

	7	6	5	4	3	2	1	0
R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 453. SPIBR Field Descriptions

Field	Description
6–4 SPPR[2:0]	**SPI Baud Rate Preselection Bits** — These bits specify the SPI baud rates as shown in Table 454. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.
2–0 SPR[2:0]	**SPI Baud Rate Selection Bits** — These bits specify the SPI baud rates as shown in Table 454. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.

The baud rate divisor equation is as follows:

$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 4}$$

The baud rate can be calculated with the following equation:

$$\text{Baud Rate} = \text{BusClock} / \text{BaudRateDivisor} \qquad \textit{Eqn. 5}$$

NOTE

For maximum allowed baud rates, refer to Section 4.6.2.5, “SPI Timing" of this data sheet.

Table 454. Example SPI Baud Rate Selection (25 MHz Bus Clock)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	0	0	0	0	2	12.5 Mbit/s
0	0	0	0	0	1	4	6.25 Mbit/s
0	0	0	0	1	0	8	3.125 Mbit/s
0	0	0	0	1	1	16	1.5625 Mbit/s
0	0	0	1	0	0	32	781.25 kbit/s
0	0	0	1	0	1	64	390.63 kbit/s
0	0	0	1	1	0	128	195.31 kbit/s
0	0	0	1	1	1	256	97.66 kbit/s
0	0	1	0	0	0	4	6.25 Mbit/s

Table 454. Example SPI Baud Rate Selection (25 MHz Bus Clock) (continued)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	1	0	0	1	8	3.125 Mbit/s
0	0	1	0	1	0	16	1.5625 Mbit/s
0	0	1	0	1	1	32	781.25 kbit/s
0	0	1	1	0	0	64	390.63 kbit/s
0	0	1	1	0	1	128	195.31 kbit/s
0	0	1	1	1	0	256	97.66 kbit/s
0	0	1	1	1	1	512	48.83 kbit/s
0	1	0	0	0	0	6	4.16667 Mbit/s
0	1	0	0	0	1	12	2.08333 Mbit/s
0	1	0	0	1	0	24	1.04167 Mbit/s
0	1	0	0	1	1	48	520.83 kbit/s
0	1	0	1	0	0	96	260.42 kbit/s
0	1	0	1	0	1	192	130.21 kbit/s
0	1	0	1	1	0	384	65.10 kbit/s
0	1	0	1	1	1	768	32.55 kbit/s
0	1	1	0	0	0	8	3.125 Mbit/s
0	1	1	0	0	1	16	1.5625 Mbit/s
0	1	1	0	1	0	32	781.25 kbit/s
0	1	1	0	1	1	64	390.63 kbit/s
0	1	1	1	0	0	128	195.31 kbit/s
0	1	1	1	0	1	256	97.66 kbit/s
0	1	1	1	1	0	512	48.83 kbit/s
0	1	1	1	1	1	1024	24.41 kbit/s
1	0	0	0	0	0	10	2.5 Mbit/s
1	0	0	0	0	1	20	1.25 Mbit/s
1	0	0	0	1	0	40	625 kbit/s
1	0	0	0	1	1	80	312.5 kbit/s
1	0	0	1	0	0	160	156.25 kbit/s
1	0	0	1	0	1	320	78.13 kbit/s
1	0	0	1	1	0	640	39.06 kbit/s
1	0	0	1	1	1	1280	19.53 kbit/s
1	0	1	0	0	0	12	2.08333 Mbit/s
1	0	1	0	0	1	24	1.04167 Mbit/s
1	0	1	0	1	0	48	520.83 kbit/s
1	0	1	0	1	1	96	260.42 kbit/s
1	0	1	1	0	0	192	130.21 kbit/s
1	0	1	1	0	1	384	65.10 kbit/s
1	0	1	1	1	0	768	32.55 kbit/s
1	0	1	1	1	1	1536	16.28 kbit/s
1	1	0	0	0	0	14	1.78571 Mbit/s
1	1	0	0	0	1	28	892.86 kbit/s
1	1	0	0	1	0	56	446.43 kbit/s

Table 471. FSEC Field Descriptions

Field	Description
7–6 KEYEN[1:0]	**Backdoor Key Security Enable Bits** — The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 472.
5–2 RNV[5:2}	**Reserved Nonvolatile Bits** — The RNV bits should remain in the erased state for future enhancements.
1–0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 473. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 472. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01	DISABLED(284)
10	ENABLED
11	DISABLED

Notes
284.Preferred KEYEN state to disable backdoor key access.

Table 473. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01	SECURED(285)
10	UNSECURED
11	SECURED

Notes
285.Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 5.24.5, “Security".

5.24.3.2.3 Flash CCOB Index Register (FCCOBIX)

The FCCOBIX register is used to index the FCCOB register for Flash memory operations.

Table 474. FCCOB Index Register (FCCOBIX)

Address: 0x0102

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CCOBIX[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

CCOBIX bits are readable and writable while remaining bits read 0 and are not writable.

Table 475. FCCOBIX Field Descriptions

Field	Description
2–0 CCOBIX[1:0]	**Common Command Register Index**— The CCOBIX bits are used to select to which word of the FCCOB register array is being read or written. See Section 5.24.3.2.11, “Flash Common Command Object Register (FCCOB)" for more details.

Table 527. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0]!= 001 at command launch
		Set if command not available in current mode (see Table 508)
		Set if an invalid global address [17:16] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

5.24.4.5.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 528. Erase P-Flash Sector Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0A	Global address [17:16] to identify P-Flash block to be erased
001	Global address [15:0] anywhere within the sector to be erased. Refer to Section 5.24.1.2.1, “P-Flash Features" for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 529. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0]!= 001 at command launch
		Set if command not available in current mode (see Table 508)
		Set if an invalid global address [17:16] is supplied
		Set if a misaligned phrase address is supplied (global address [2:0]!= 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

5.24.4.5.10 Unsecure Flash Command

The Unsecure Flash command will erase the entire P-Flash and D-Flash memory space and, if the erase is successful, will release security.

Table 530. Unsecure Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0B	Not required

Upon clearing CCIF to launch the Unsecure Flash command, the Memory Controller will erase the entire P-Flash and D-Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. If the erase verify is not successful, the Unsecure Flash operation sets MGSTAT1 and terminates without changing the security state. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag is set after the Unsecure Flash operation has completed.

Table 534. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Global address [17:16] to identify the Flash block
001	Margin level setting	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the D-Flash block is targeted, the D-Flash user margin levels are applied only to the D-Flash reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and D-Flash reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 535.

Table 535. Valid Set User Margin Level Settings

CCOB (CCOBIX=001)	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level(299)
0x0002	User Margin-0 Level(300)

Notes
299.Read margin to the erased state
300.Read margin to the programmed state

Table 536. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0]!= 001 at command launch
		Set if command not available in current mode (see Table 508)
		Set if an invalid global address [17:16] is supplied
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

5.24.4.5.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or D-Flash block.

Table 540. Erase Verify D-Flash Section Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x10	Global address [17:16] to identify the D-Flash block
001	Global address [15:0] of the first word to be verified	
010	Number of words to be verified	

Upon clearing CCIF to launch the Erase Verify D-Flash Section command, the Memory Controller will verify the selected section of D-Flash memory is erased. The CCIF flag will set after the Erase Verify D-Flash Section operation has completed.

Table 541. Erase Verify D-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0]!= 010 at command launch
		Set if command not available in current mode (see Table 508)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0]!= 0)
		Set if the requested section breaches the end of the D-Flash block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

5.24.4.5.15 Program D-Flash Command

The Program D-Flash operation programs one to four previously erased words in the D-Flash block. The Program D-Flash operation will confirm that the targeted location(s) were successfully programmed upon completion.

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 542. Program D-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [17:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. The CCIF flag is set when the operation has completed.

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