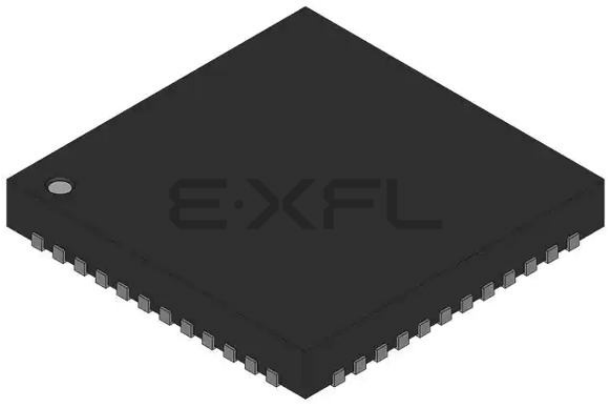

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Table 4. MM912_637 Pin Description

Pin #	Pin Name	Formal Name	Description
28	VTEMP	Temperature Sensor Input	External temperature sensor input. See Section 5.6, “Temperature Measurement - TSENSE".
29	TSUP	Temperature Sensor Supply Output	Supply for the external temperature sensor. TSUP frequency compensation option to allow capacitor CTSUP. See Section 5.6, “Temperature Measurement - TSENSE".
30	GNDSUB	Substrate Ground	Substrate ground connection to improve EMC behavior.
31	ISENSEL	Current Sense L	Current sense input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
32	ISENSEH	Current Sense H	Current sense input “high”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. See Section 5.4, “Current Measurement - ISENSE".
33	ADCGND	Analog Digital Converter Ground	Analog digital converter ground connection. See Section 5.2, “Analog Die - Power, Clock and Resets - PCR".
34	VSENSE	Voltage Sense	Precision battery voltage measurement input. This pin can be connected directly to the battery line for voltage measurements. The voltage preset at this input is scaled down by an internal voltage divider. The pin is self protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection. See Section 5.5, “Voltage Measurement - VSENSE".
35	VOPT	Optional Voltage Sense	Optional voltage measurement input. See Section 5.5, “Voltage Measurement - VSENSE".
36	PTB3 / L0	General Purpose Input 3 - High Voltage Input 0	This is the high voltage general purpose input pin 3, based on VDDX with the following shared functions: • Internal clamping structure to operate as a high voltage input (L0). When used as high voltage input, a series resistor (RL0) and capacitor to GND (C_{L0}) must be used to protect against automotive transients, when used to connect outside the PCB. • 5.0 V (VDDX) digital port input • Selectable internal pull-down resistor • Selectable wake-up input during low power mode. • Selectable timer channel input • Selectable connection to the LIN / SCI (Input only) See Section 5.10, “General Purpose I/O - GPIO".
37	PTB2	General Purpose I/O 2	This is the general purpose I/O pin 2 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
38	PTB1	General Purpose I/O 1	This is the general purpose I/O pin 1, based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".
39	PTB0	General Purpose I/O 0	This is the general purpose I/O pin 0 based on VDDX with the following shared functions: • Bidirectional 5.0 V (VDDX) digital port I/O • Selectable internal pull-up resistor • Selectable timer channel input/output • Selectable connection to the LIN / SCI See Section 5.10, “General Purpose I/O - GPIO".

Table 49. Device Register Memory Map Overview (continued)

Address	Module	Size (Bytes)
0x00E0–0x00E7	Reserved	32
0x00E8–0x00EF	SPI (serial peripheral interface)	8
0x00F0–0x00FF	Reserved	32
0x0100–0x0113	FTMRC control registers	20
0x0114–0x011F	Reserved	12
0x0120–0x017F	PIM (port integration module)	96
0x0180–0x01EF	Reserved	112
0x01F0–0x01FC	CPMU (clock and power management)	13
0x01FD–0x01FF	Reserved	3
0x0200-0x02FF	D2DI (die 2 die initiator, blocking access window)	256
0x0300–0x03FF	D2DI (die 2 die initiator, non-blocking write window)	256

NOTE

The reserved register space shown in Table 49 is not allocated to any module. This register space is reserved for future use. Writing to these locations has no effect. Read access to these locations returns a zero.

5.0.3 Detailed Module Register Map

Table 50 to Table 63 show the detailed module maps of the MM912_637.

Table 50. 0x0000–0x0009 Port Integration Module (PIM) 1 of 3

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0000	PTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W								
0x0001	PTE	R	0	0	0	0	0	0	PE1	PE0
		W								
0x0002	DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
0x0003	DDRE	R	0	0	0	0	0	0	DDRE1	DDRE0
		W								
0x0004-0 x0009	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 51. 0x000A–0x000B Memory Map Control (MMC) 1 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x000A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x000B	MODE	R	MODC	0	0	0	0	0	0	0
		W								

Figure 22 and Figure 23 show the different clock sources for normal and low power mode.

NOTE

D2DFCLK has to be set to match 512 kHz, resulting in D2DSCLK being 1.0, 2.0, 4.0, or 8.0 kHz, based on PF[1:0]

The minimum value for PRESC[15:0] has to be 0x0400. Any value lower than 0x0400 will result in faulty behavior and is not recommended. Values of 0x0003 or less are not stored by the internal logic.

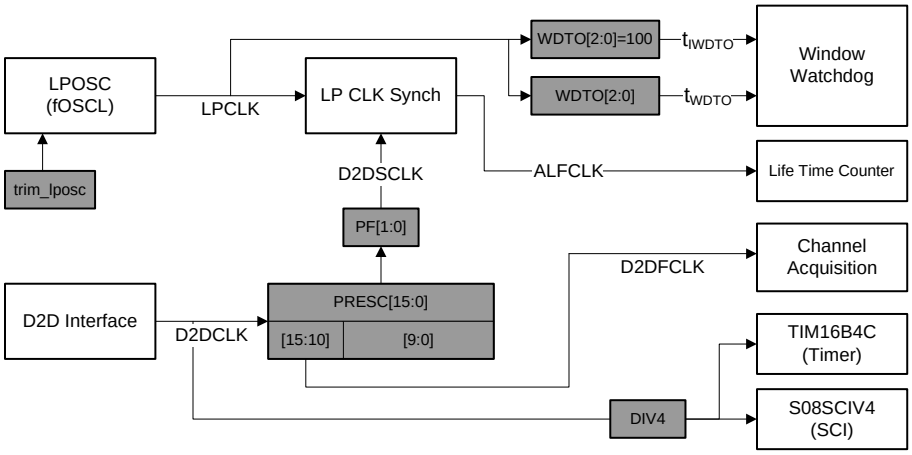

Figure 22. Clock Tree Overview - Normal Mode

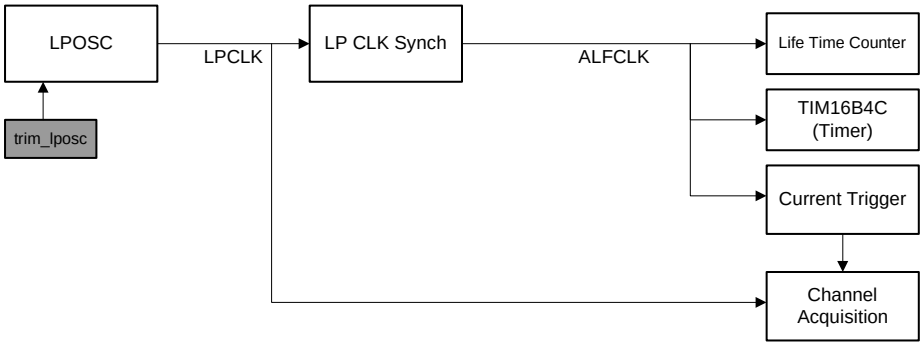

Figure 23. Clock Tree Overview - Low Power Modes

5.2.5.2 ALFCLK Calibration

To increase the accuracy of the 1.0 kHz (or 2.0, 4.0, 8.0 7kHz based on PF[1:0]) system clock (ALFCLK), the low power oscillator (LPCLK) is synchronized to the more precise D2DCLK, via the D2DSCLK signal. The “Calibrated Low Power Clock” (ALFCLK) could be trimmed to the D2DCLK accuracy plus a maximum error adder of 1 LPCLK period, by internally counting the number of periods of the LPCLK (512 kHz) during a D2DSCLK period. The APRESC[12:0] register will represent the calculated internal prescaler. The PRDF bit (Prescaler Ready flag) will indicate the synchronization complete after a power up or prescaler (PRESC/PF) change.

The adjustment is continuously performed during Normal mode. During low power mode (STOP or SLEEP), the last adjustment factor would be used.

5.7 Channel Acquisition

5.7.1 Introduction

This chapter documents the current, voltage, and temperature acquisition flow. The chapter is structured in the following sections.

- Section 5.7.2, “Channel Structure Overview"
- Section 5.7.3, “Current and Voltage Measurement"
  - Section 5.7.3.1, “Shunt Sense, PGA, and GCB (Current Channel only)"
  - Section 5.7.3.2, “Voltage Sense Multiplexer (Voltage Channel only)"
  - Section 5.7.3.3, “Sigma Delta Converter"
  - Section 5.7.3.4, “Compensation"
  - Section 5.7.3.5, “IIR / Decimation / Chopping Stage"
  - Section 5.7.3.6, “Low Pass Filter"
  - Section 5.7.3.7, “Format and Clamping"
- Section 5.7.4, “Temperature Measurement Channel"
  - Section 5.7.4.1, “Compensation"
- Section 5.7.5, “Calibration"
- Section 5.7.6, “Memory Map and Registers"

5.7.2 Channel Structure Overview

The MM912_637 offers three parallel measurement channels. Current, Voltage, and Temperature. The Voltage Channel is shared between the VSENSE and VOPT voltage source, the Temperature channel between ETEMP and ITEMP.

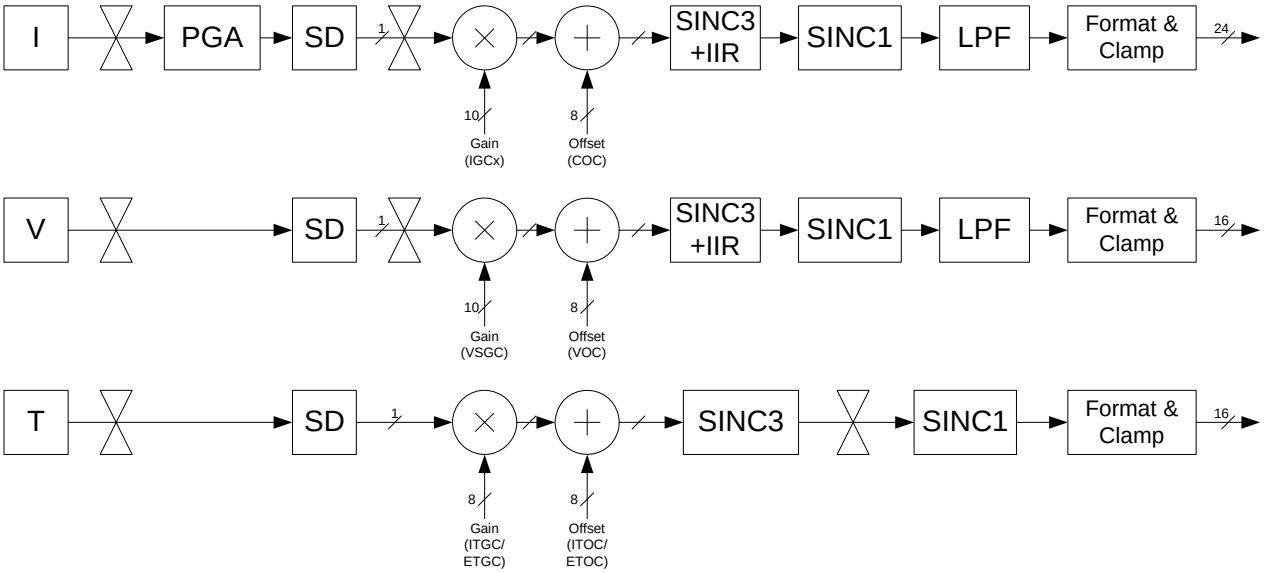

Figure 32. Simplified Measurement Channel

Figure 33 shows an overview of the detailed dependencies between the control and status registers and the channels. Refer to the following sections of this chapter for details.

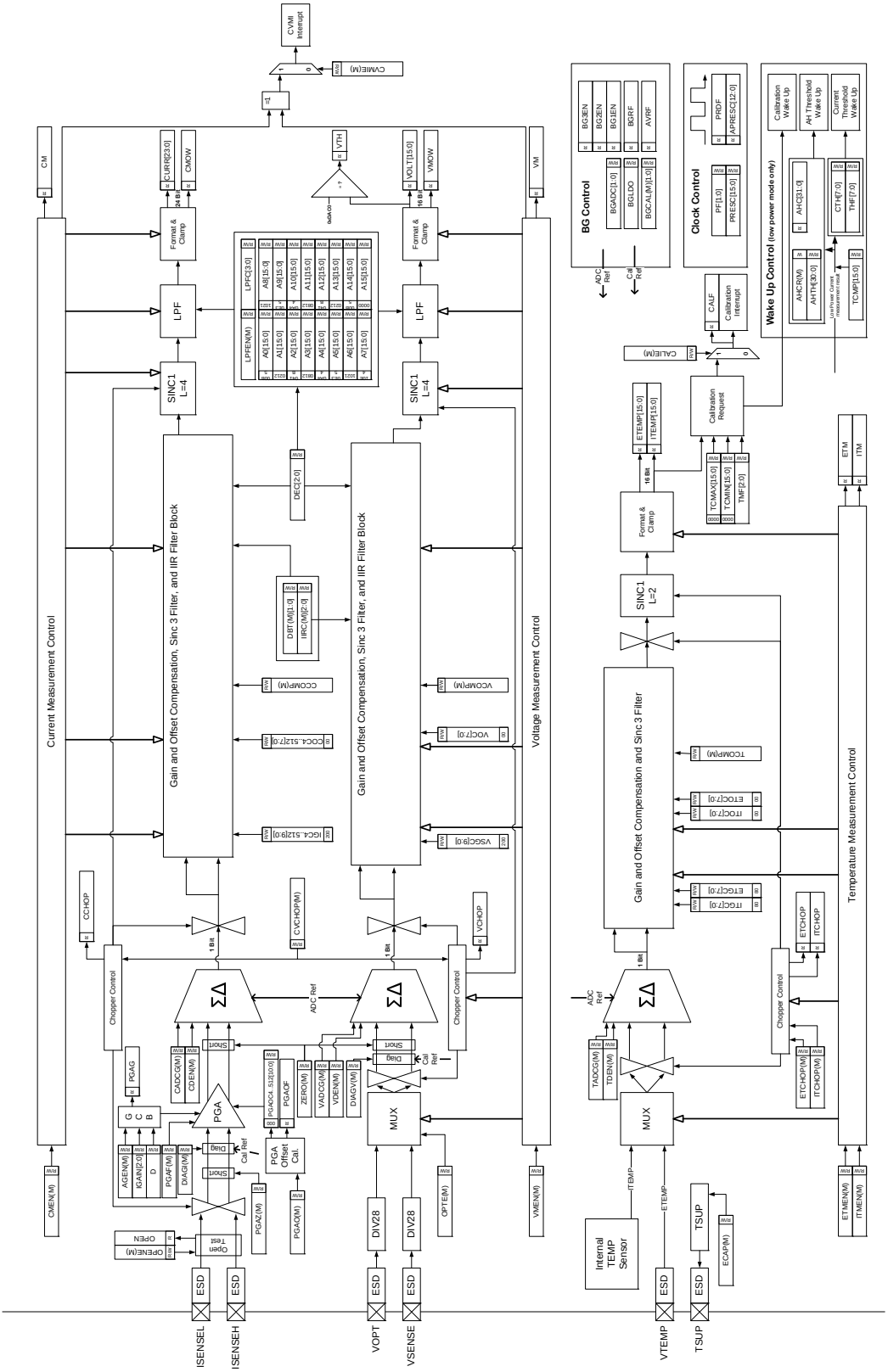

Figure 33. Channel Complete Overview

Table 108. Module Memory Map

Offset	Name		7	6	5	4	3	2	1	0
0xBA	COMP_IG128 Gain current compensation 128	R	0	0	0	0	0	0	IGC128[9:8]	
		W								
		R	IGC128[7:0]							
		W								
0xBC	COMP_IG256 Gain current compensation 256	R	0	0	0	0	0	0	IGC256[9:8]	
		W								
		R	IGC256[7:0]							
		W								
0xBE	COMP_IG512 Gain current compensation 512	R	0	0	0	0	0	0	IGC512[9:8]	
		W								
		R	IGC512[7:0]							
		W								
0xC0	COMP_PGAO4 Offset PGA compensation 4	R	0	0	0	0	0	PGAOC4[10:8]		
		W								
		R	PGAOC4[7:0]							
		W								
0xC2	COMP_PGAO8 Offset PGA compensation 8	R	0	0	0	0	0	PGAOC8[10:8]		
		W								
		R	PGAOC8[7:0]							
		W								
0xC4	COMP_PGAO16 Offset PGA compensation 16	R	0	0	0	0	0	PGAOC16[10:8]		
		W								
		R	PGAOC16[7:0]							
		W								
0xC6	COMP_PGAO32 Offset PGA compensation 32	R	0	0	0	0	0	PGAOC32[10:8]		
		W								
		R	PGAOC32[7:0]							
		W								
0xC8	COMP_PGAO64 Offset PGA compensation 64	R	0	0	0	0	0	PGAOC64[10:8]		
		W								
		R	PGAOC64[7:0]							
		W								
0xCA	COMP_PGAO128 Offset PGA compensation 128	R	0	0	0	0	0	PGAOC128[10:8]		
		W								
		R	PGAOC128[7:0]							
		W								
0xCC	COMP_PGAO256 Offset PGA compensation 256	R	0	0	0	0	0	PGAOC256[10:8]		
		W								
		R	PGAOC256[7:0]							
		W								

Table 150. Low Power Ah Counter (ACQ_AHC1 (hi) / ACQ_AHC1 (lo) / ACQ_AHC0 (hi) / ACQ_AHC0 (lo)) - Register Field Descriptions

Field	Description
31-0 AHC[31:0]	Low power Ah counter (32-Bit signed integer, two's complement). Reading one 16-Bit part of the register will buffer the second. Reading the second will unlock the buffer. See Section 5.2.4.1.1.2, "Current Ampere Hour Threshold Wake-up".

5.7.6.3.22 Low Pass Filter Coefficient Ax (LPF_Ax (hi))

Table 151. Low Pass Filter Coefficient Ax (LPF_Ax (hi))

Offset[142] 0x80...0x9E — Access: User read/write

	7	6	5	4	3	2	1	0
R W	Ax[15:8]							
Reset	see Table 154							

Notes
142.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.7.6.3.23 Low Pass Filter Coefficient Ax (LPF_Ax (lo))

Table 152. Low Pass Filter Coefficient Ax (LPF_Ax (lo))

Offset[143] 0x81...0x9F — Access: User read/write

	7	6	5	4	3	2	1	0
R W	Ax[7:0]							
Reset	see Table 154							

Notes
143.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 153. Low Pass Filter Coefficient Ax - Register Field Descriptions

Field	Description
15-0 Ax[15:0]	Low Pass Filter Coefficient Value. x = 0...15. Data Format: MSB = Sign ("1" minus). [14:0] integer.

Table 154. Low Pass Filter Coefficient Ax - Reset Values

Field	Reset Value	Field	Reset Value
A0	0x00F5	A8	0x1021
A1	0x0312	A9	0x0E35
A2	0x051F	A10	0x0B44
A3	0x0852	A11	0x0852
A4	0x0B44	A12	0x051F
A5	0x0E35	A13	0x0312
A6	0x1021	A14	0x00F5
A7	0x10E5	A15	0x0000

Table 156. Compensation Control Register (COMP_CTL) - Register Field Descriptions

Field	Description
3 DIAGV	Diagnostic Mode Voltage Channel 0 - Calibration reference disconnected from the voltage channel input 1 - Calibration reference connected to the voltage channel input for calibration. Manual conversion needed to measure reference
2 DIAGI	Diagnostic Mode Current Channel 0 - Calibration reference disconnected from the current channel input 1 - Calibration reference connected to the current channel input for calibration. Manual conversion needed to measure reference
0 CALIE	Calibration IRQ Enable 0 - Calibration request interrupt disabled 1 - Calibration request interrupt enabled. A temperature “out of calibration range” will cause a calibration interrupt request

5.7.6.3.25 Compensation Status Register (COMP_SR)

Table 157. Compensation Status Register (COMP_SR)

Offset[146] 0xA2 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	BGRF	0	PGAOF	0	0	0	CALF
W	Write 1 will clear the flags and will start next calibration steps							
Reset	0	0	0	0	0	0	0	0

Notes
146.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 158. Compensation Status Register (COMP_SR) - Register Field Descriptions

Field	Description
6 BGRF	Band Gap Reference Status Flag 0 - Indicates the reference bandgap has not been set / applied 1 - Reference bandgap has been set. Writing 1 will clear the flag
4 PGAOF	PGA Internal Offset Compensation Complete Flag 0 - PGA offset compensation ongoing or not started since last flag clear 1 - PGA offset compensation finished since last flag clear. Writing 1 will clear the flag
0 CALF	Calibration Request Status Flag 0 - No Temperature out of range condition detected 1 - Temperature out of range condition detected. Writing 1 will clear the flag

5.7.6.3.26 Temperature Filtering Period (COMP_TF)

Table 159. Temperature Filtering Period (COMP_TF)

Offset[147] 0xA3 — Access: User read / write

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TMF[2:0]		
W								
Reset	0	0	0	0	0	0	0	0

Notes
147.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 221. Timer Input Capture/Output Compare Register 1(TC1)

Offset[190] 0x30, 0x31 — Access: User read/write

	15	14	13	12	11	10	9	8
R W	tc1_15	tc1_14	tc1_13	tc1_12	tc1_11	tc1_10	tc1_9	tc1_8
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R W	tc1_7	tc1_6	tc1_5	tc1_4	tc1_3	tc1_2	tc1_1	tc1_0
Reset	0	0	0	0	0	0	0	0

Notes
190.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 222. Timer Input Capture/Output Compare Register 2(TC2)

Offset[191] 0x32, 0x33 — Access: User read/write

	15	14	13	12	11	10	9	8
R W	tc2_15	tc2_14	tc2_13	tc2_12	tc2_11	tc2_10	tc2_9	tc2_8
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R W	tc2_7	tc2_6	tc2_5	tc2_4	tc2_3	tc2_2	tc2_1	tc2_0
Reset	0	0	0	0	0	0	0	0

Notes
191.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 223. Timer Input Capture/Output Compare Register 3(TC3)

Offset[192] 0x34, 0x35 — Access: User read/write

	15	14	13	12	11	10	9	8
R W	tc3_15	tc3_14	tc3_13	tc3_12	tc3_11	tc3_10	tc3_9	tc3_8
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R W	tc3_7	tc3_6	tc3_5	tc3_4	tc3_3	tc3_2	tc3_1	tc3_0
Reset	0	0	0	0	0	0	0	0

Notes
192.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 224. TCn - Register Field Descriptions

Field	Description
15-0 tcn[15-0]	16 Timer Input Capture/Output Compare Registers

5.12.2.3.4 SCI Status Register 1 (SCIS1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.

Table 267. SCI Status Register 1 (SCIS1)

Offset(222) 0x1C — Access: User read/write

	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Notes
222.Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 268. SCIS1 Field Descriptions

Field	Description
7 TDRE	**Transmit Data Register Empty Flag** — TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCIS1 with TDRE = 1 and then write to the SCI data register (SCID). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.
6 TC	**Transmission Complete Flag** — TC is set out of reset and when TDRE = 1 and no data, preamble, or break character is being transmitted. 0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete). TC is cleared automatically by reading SCIS1 with TC = 1 and then doing one of the following three things: • Write to the SCI data register (SCID) to transmit new data • Queue a preamble by changing TE from 0 to 1 • Queue a break character by writing 1 to SBK in SCIC2
5 RDRF	**Receive Data Register Full Flag** — RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCID). To clear RDRF, read SCIS1 with RDRF = 1 and then read the SCI data register (SCID). 0 Receive data register empty. 1 Receive data register full.
4 IDLE	**Idle Line Flag** — IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT = 0, the receiver starts counting idle bit times after the start bit. So if the receive character is all 1s, these bit times and the stop bit time count toward the full character time of logic high (10 or 11 bit times depending on the M control bit) needed for the receiver to detect an idle line. When ILT = 1, the receiver doesn't start counting idle bit times until after the stop bit. So the stop bit and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, read SCIS1 with IDLE = 1 and then read the SCI data register (SCID). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE will get set only once even if the receive line remains idle for an extended period. 0 No idle line detected. 1 Idle line was detected.
3 OR	**Receiver Overrun Flag** — OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCID yet. In this case, the new character (and all associated error information) is lost because there is no room to move it into SCID. To clear OR, read SCIS1 with OR = 1 and then read the SCI data register (SCID). 0 No overrun. 1 Receive overrun (new SCI data lost).

5.15.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each revision of the chip. Table 285 shows the assigned part ID number and Mask Set number.

The Version ID in Table 285 is a word located in a flash information row. The version ID number indicates a specific version of internal NVM controller.

Table 285. Assigned Part ID Numbers

Device	Mask Set Number	Part ID[235]	Version ID
MM912_637	0M96X	0x3880	0x0000

Notes

235.The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-6: Minor family identifier
Bit 5-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor — non full — mask set revision

5.15.7 System Clock Description

Refer to Section 5.22, “S12 Clock, Reset, and Power Management Unit (S12CPMU)" for the system clock description.

5.15.8 Modes of Operation

The MCU can operate in different modes. These are described in Section 5.15.8.1, “Chip Configuration Summary".

The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in Section 5.15.8.2, “Low Power Operation".

Some modules feature a software programmable option to freeze the module status while the background debug module is active to facilitate debugging.

5.15.8.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 286). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of RESET.

Table 286. Chip Modes

Chip Modes	MODC
Normal single chip	1
Special single chip	0

5.15.8.1.1 Normal Single-chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

5.15.8.1.2 Special Single-chip Mode

This mode is used for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware waits for additional serial commands through the BKGD pin.

NOTE

Care must be taken to ensure that all interrupt requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not get processed at all or the result may be a spurious interrupt request (vector at address (vector base + 0x0080)).

5.17.4.3 Reset Exception Requests

The INT module supports three system reset exception request types (Refer to the Clock and Reset generator module for details):

1. Pin reset, power-on reset or illegal address reset, low voltage reset (if applicable)
2. Clock monitor reset request
3. COP watchdog reset request

5.17.4.4 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT module upon request by the CPU is shown in Table 312.

Table 312. Exception Vector Map and Priority

Vector Address[240]	Source
0xFFFE	Pin reset, power-on reset, illegal address reset, low voltage reset (if applicable)
0xFFFC	Clock monitor reset
0xFFFA	COP watchdog reset
(Vector base + 0x00F8)	Unimplemented opcode trap
(Vector base + 0x00F6)	Software interrupt instruction (SWI) or BDM vector request
(Vector base + 0x00F4)	X bit maskable interrupt request (XIRQ or D2D error interrupt)[241]
(Vector base + 0x00F2)	IRQ or D2D interrupt request[242]
(Vector base + 0x00F0–0x0082)	Device specific I bit maskable interrupt sources (priority determined by the low byte of the vector address, in descending order)
(Vector base + 0x0080)	Spurious interrupt

Notes
240.16-bit vector address based
241.D2D error interrupt on MCUs featuring a D2D initiator module, otherwise XIRQ pin interrupt
242.D2D interrupt on MCUs featuring a D2D initiator module, otherwise IRQ pin interrupt

5.17.5 Initialization/Application Information

5.17.5.1 Initialization

After a system reset, the software should:

1. Initialize the interrupt vector base register, if the interrupt vector table is not located at the default location (0xFF80–0xFFF9).
2. Enable I bit maskable interrupts by clearing the I bit in the CCR.
3. Enable the X bit maskable interrupt by clearing the X bit in the CCR.

5.19.3.2.8.5 Debug Comparator Data High Register (DBGADH)

Table 366. Debug Comparator Data High Register (DBGADH)

Address: 0x002C

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00
Write: If COMRV[1:0] = 00 and DBG not armed

Table 367. DBGADH Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Compare Bits**— The Comparator data high compare bits control whether the selected comparator compares the data bus bits [15:8] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparator A. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear. 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

5.19.3.2.8.6 Debug Comparator Data Low Register (DBGADL)

Table 368. Debug Comparator Data Low Register (DBGADL)

Address: 0x002D

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00
Write: If COMRV[1:0] = 00 and DBG not armed

Table 369. DBGADL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Compare Bits** — The Comparator data low compare bits control, whether the selected comparator compares the data bus bits [7:0] to a logic one or a logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is a logic 1. This register is available only for comparator A. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin, and when the data bus cycle is complete. See Section 5.21.4.3, “BDM Hardware Commands" and Section 5.21.4.4, “Standard BDM Firmware Commands" for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command issues an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command issues an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL(262) command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

5.21.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands, because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (The lowest serial communication frequency is determined by the settings for the VCO clock (CPMUSYNR). The BDM clock frequency is always VCO clock frequency divided by 8.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high-impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic one.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high-impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed, and the communication protocol can easily tolerate speed errors of several percent.

As soon as the SYNC request is detected by the target, any partially received command or bit retrieved is discarded. This is referred to as a soft-reset, equivalent to a time-out in the serial communication. After the SYNC response, the target will consider the next negative edge (issued by the host) as the start of a new BDM command or the start of new SYNC request.

Another use of the SYNC command pulse is to abort a pending ACK pulse. The behavior is exactly the same as in a regular SYNC command. Note that one of the possible causes for a command to not be acknowledged by the target is a host-target synchronization problem. In this case, the command may not have been understood by the target, so an ACK response pulse will not be issued.

NOTE

When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop mode with OSCE bit already 1), the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop mode.

5.22.1.3 S12CPMU Block Diagram

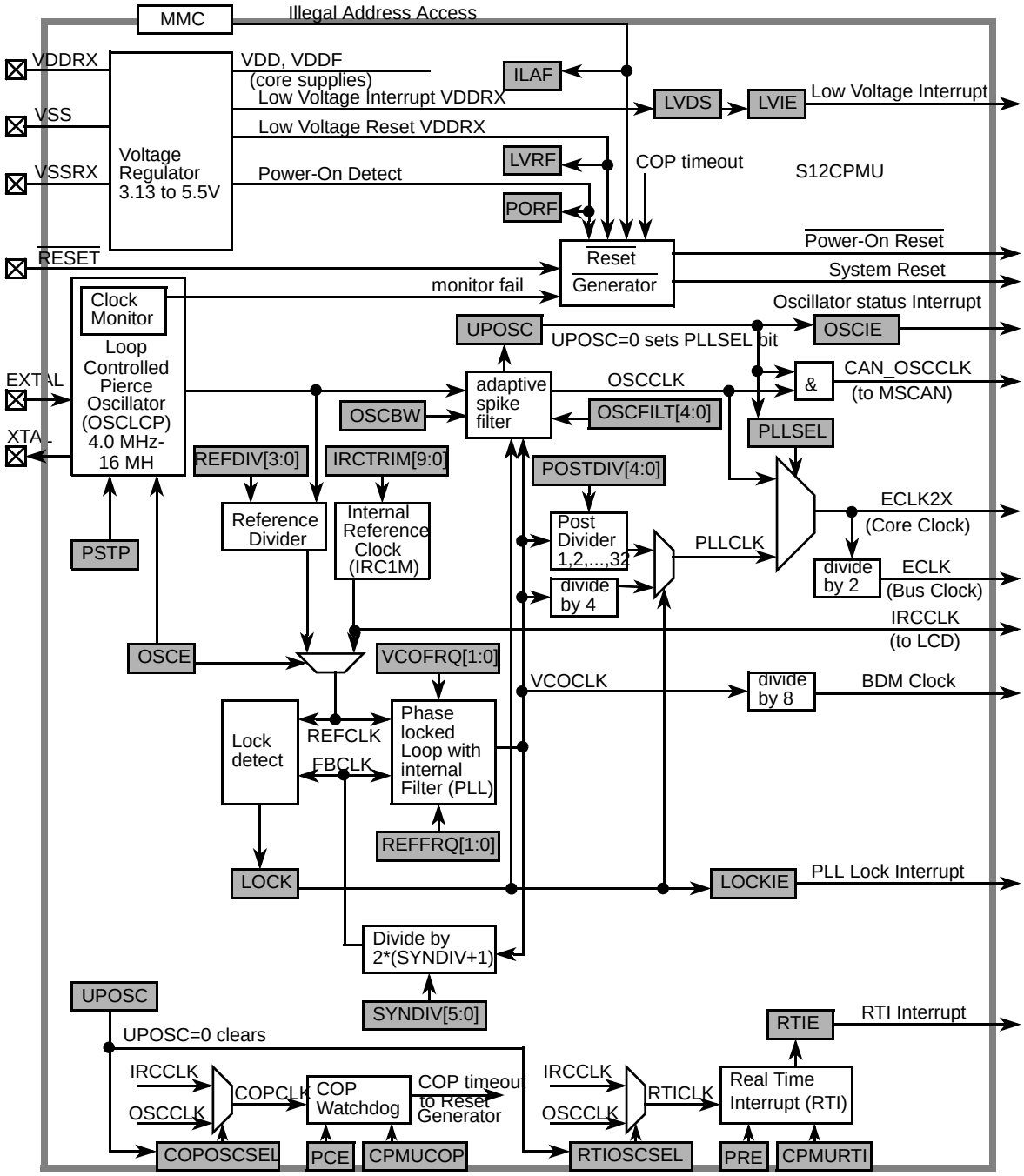

Figure 90. Block Diagram of S12CPMU

Table 442. Reset Vector Selection

Sampled $\overline{\text{RESET}}$ Pin (256 cycles after release)	Oscillator monitor fail pending	COP timeout pending	Vector Fetch
1	0	0	POR LVR Illegal Address Reset External pin $\overline{\text{RESET}}$
1	1	X	Clock Monitor Reset
1	0	1	COP Reset
0	X	X	POR LVR Illegal Address Reset External pin $\overline{\text{RESET}}$

NOTE

While System Reset is asserted, the PLLCLK runs with the frequency f_{VCORST}.

The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the $\overline{\text{RESET}}$ pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

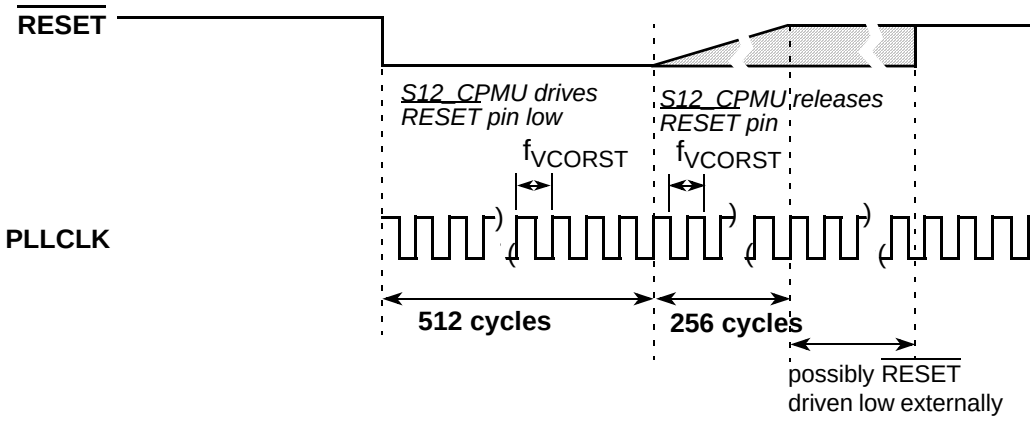

Figure 100. RESET Timing

5.22.5.2.1 Clock Monitor Reset

When the external oscillator is enabled (OSCE=1), in case of a loss of oscillation or the oscillator frequency is below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU generates a clock monitor reset. In Full Stop mode the external oscillator and the clock monitor are disabled.

5.22.5.2.2 Computer Operating Properly Watchdog (COP) Reset

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out, it is an indication that the software is no longer being executed in the intended sequence, and a COP reset is generated.

The clock source for the COP is either IRCCLK or OSCCLK, depending on the setting of the COPOSCSEL bit. In Stop mode with PSTP=1 (Pseudo Stop mode), COPOSCSEL=1 and PCE=1 the COP continues to run, else the COP counter halts in Stop mode.

Three control bits in the CPMUCOP register allow selection of seven COP timeout periods.

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 102).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 103).

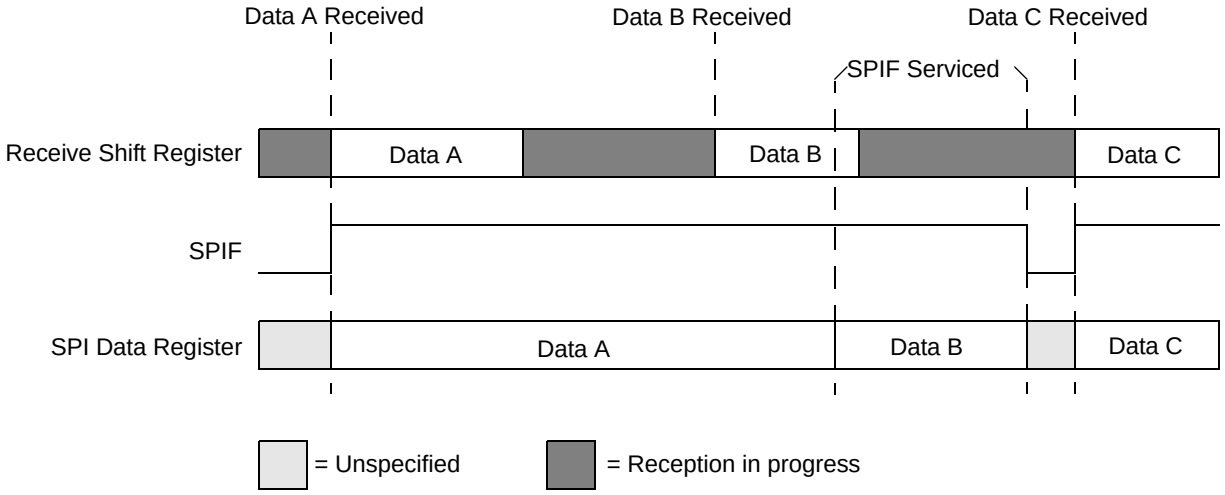

Figure 102. Reception with SPIF Serviced in Time

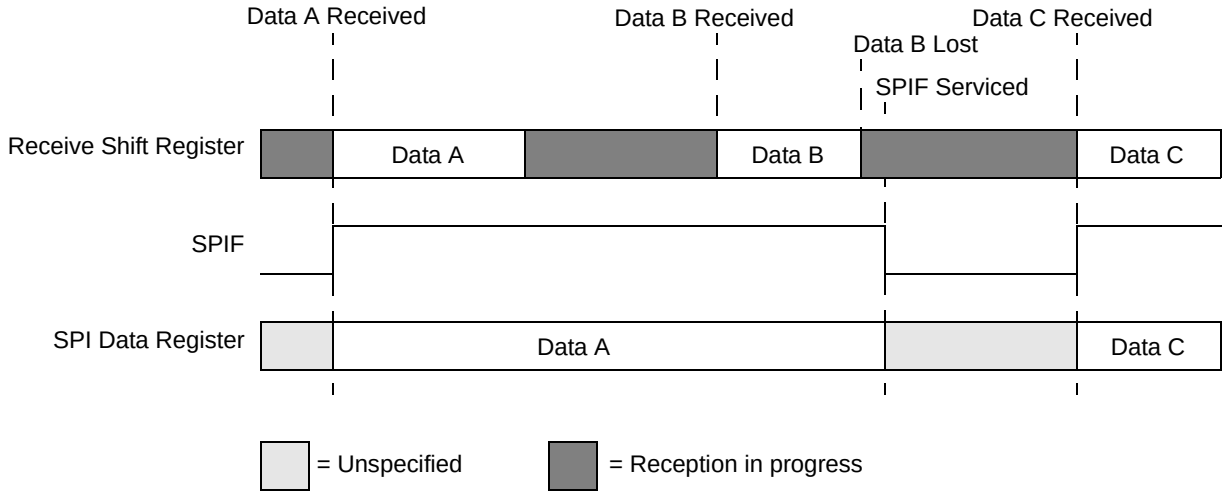

Figure 103. Reception with SPIF Serviced Too Late

Table 486. FPROT Field Descriptions (continued)

Field	Description
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 488. The FPHS bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1–0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 489. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 487. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[288]
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

Notes
288.For range sizes, refer to Table 488 and Table 489.

Table 488. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2.0 kbytes
01	0x3_F000–0x3_FFFF	4.0 kbytes
10	0x3_E000–0x3_FFFF	8.0 kbytes
11	0x3_C000–0x3_FFFF	16 kbytes

Table 489. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1.0 kbyte
01	0x3_8000–0x3_87FF	2.0 kbytes
10	0x3_8000–0x3_8FFF	4.0 kbytes
11	0x3_8000–0x3_9FFF	8.0 kbytes

All possible P-Flash protection scenarios are shown in Figure 112. Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible, if reprogramming is not required.

Table 564. Analog Die Trimming Information

Global Address (IFRON)	OFFSET		Byte Description								Target Register	
	HEX	DEC	7	6	5	4	3	2	1	0	Name	Offset
0x0_40C0	00	00							IGC4[9:8]		COMP_IG4 (hi)	0xB0
0x0_40C1	01	01	IGC4[7:0]								COMP_IG4 (lo)	
0x0_40C2	02	02							IGC8[9:8]		COMP_IG8 (hi)	0xB2
0x0_40C3	03	03	IGC8[7:0]								COMP_IG8 (lo)	
0x0_40C4	04	04							IGC16[9:8]		COMP_IG16 (hi)	0xB4
0x0_40C5	05	05	IGC16[7:0]								COMP_IG16 (lo)	
0x0_40C6	06	06							IGC32[9:8]		COMP_IG32 (hi)	0xB6
0x0_40C7	07	07	IGC32[7:0]								COMP_IG32 (lo)	
0x0_40C8	08	08							IGC64[9:8]		COMP_IG64 (hi)	0xB8
0x0_40C9	09	09	IGC64[7:0]								COMP_IG64 (lo)	
0x0_40CA	0A	10							IGC128[9:8]		COMP_IG128 (hi)	0xBA
0x0_40CB	0B	11	IGC128[7:0]								COMP_IG128 (lo)	
0x0_40CC	0C	12							IGC256[9:8]		COMP_IG256 (hi)	0xBC
0x0_40CD	0D	13	IGC256[7:0]								COMP_IG256 (lo)	
0x0_40CE	0E	14							IGC512[9:8]		COMP_IG512 (hi)	0xBE
0x0_40CF	0F	15	IGC512[7:0]								COMP_IG512 (lo)	
0x0_40D0	10	16			TCIBG2[2:0]			SLPBG[2:0]			TRIM_BG0 (hi)	0xE0
0x0_40D1	11	17			IBG2[2:0]			IBG1[2:0]			TRIM_BG0 (lo)	0xE1
0x0_40D2	12	18	UBG 3	DBG 3	TCBG2[2:0]			TCBG1[2:0]			TRIM_BG1 (hi)	0xE2
0x0_40D3	13	19						SLPBG[2:0]			TRIM_BG1 (lo)	0xE3
0x0_40D4	14	20	V1P2BG2[3:0]				V1P2BG1[3:0]				TRIM_BG2 (hi)	0xE4
0x0_40D5	15	21	V2P5BG2[3:0]				V2P5BG1[3:0]				TRIM_BG2 (lo)	0xE5
0x0_40D6	16	22								LIN	TRIM_LIN	0xE6
0x0_40D7	17	23								LVT	TRIM_LVT	0xE7
0x0_40D8	18	24				LPOSC[12:8]					TRIM_OSC (hi)	0xE8
0x0_40D9	19	25	LPOSC[7:0]								TRIM_OSC (lo)	0xE9
0x0_40DA	1A	26	VOC_S[7:0]								COMP_VOS	0xAA[306]
0x0_40DB	1B	27	VOC_O[7:0]								COMP_VOO	0xAA[306]
0x0_40DC	1C	28	VOC_S[7:0] (Chopper Mode)								COMP_VOS_CHOP	0xAA[306]
0x0_40DD	1D	29	VOC_O[7:0] (Chopper Mode)								COMP_VOO_CHOP	0xAA[306]
0x0_40DE	1E	30							VSGC[9:8]		COMP_VSG (hi)	0xAC[306]
0x0_40DF	1F	31	VSGC[7:0]								COMP_VSG (lo)	
0x0_40E0	20	32							VOGC[9:8]		COMP_VOG (hi)	0xAC[306]
0x0_40E1	21	33	VOGC[7:0]								COMP_VOG (lo)	
0x0_40E2	22	34	ITO[7:0]								COMP_ITO	0xD0
0x0_40E3	23	35	ITG[7:0]								COMP_ITG	0xD1
0x0_40E4	24	36	BG3 diag measurement from Vsense channel after cal at room								GAIN_CAL_VSENSE_ROOM (hi)	n.a.
0x0_40E5	25	37									GAIN_CAL_VSENSE_ROOM (lo)	n.a.
0x0_40E6	26	38	BG3 diag measurement from Vopt channel after cal at room								GAIN_CAL_VOPT_ROOM (hi)	n.a.
0x0_40E7	27	39									GAIN_CAL_VOPT_ROOM (lo)	n.a.

Table 564. Analog Die Trimming Information

Global Address (IFRON)	OFFSET		Byte Description								Target Register	
	HEX	DEC	7	6	5	4	3	2	1	0	Name	Offset
0x0_40E8	28	40	BG3 diag measurement from I channel (gain4) at room								GAIN_CAL_IG4_ROOM (hi)	n.a.
0x0_40E9	29	41									GAIN_CAL_IG4_ROOM (med)	n.a.
0x0_40EA	2A	42									GAIN_CAL_IG4_ROOM (lo)	n.a.
0x0_40EB	2B	43	Reserved									
0x0_40EC	2C	44	COMP_VSG_COLD[7:0]								VSENSE Channel Gain Compensation - COLD Temp(307)	n.a.
0x0_40ED	2D	45	COMP_VSG_HOT[7:0]								VSENSE Channel Gain Compensation - HOT Temp(307)	n.a.
0x0_40EE	2E	46	COMP_VOG_COLD[7:0]								VOPT Channel Gain Compensation - COLD Temp(307)	n.a.
0x0_40EF	2F	47	COMP_VOG_HOT[7:0]								VOPT Channel Gain Compensation - HOT Temp(307)	n.a.
0x0_40F0	30	48	IGC4_COLD[7:0]								Current Channel Gain (4) Compensation - COLD Temp(307)	n.a.
0x0_40F1	31	49	IGC4_HOT[7:0]								Current Channel Gain (4) Compensation - HOT Temp(307)	n.a.
0x0_40F2	32	50	IGC8_COLD[7:0]								Current Channel Gain (8) Compensation - COLD Temp(307)	n.a.
0x0_40F3	33	51	IGC8_HOT[7:0]								Current Channel Gain (8) Compensation - HOT Temp(307)	n.a.
0x0_40F4	34	52	IGC16_COLD[7:0]								Current Channel Gain (16) Compensation - COLD Temp(307)	n.a.
0x0_40F5	35	53	IGC16_HOT[7:0]								Current Channel Gain (16) Compensation - HOT Temp(307)	n.a.
0x0_40F6	36	54	IGC32_COLD[7:0]								Current Channel Gain (32) Compensation - COLD Temp(307)	n.a.
0x0_40F7	37	55	IGC32_HOT[7:0]								Current Channel Gain (32) Compensation - HOT Temp(307)	n.a.
0x0_40F8	38	56	IGC64_COLD[7:0]								Current Channel Gain (64) Compensation - COLD Temp(307)	n.a.
0x0_40F9	39	57	IGC64_HOT[7:0]								Current Channel Gain (64) Compensation - HOT Temp(307)	n.a.
0x0_40FA	3A	58	IGC128_COLD[7:0]								Current Channel Gain (128) Compensation - COLD Temp(307)	n.a.
0x0_40FB	3B	59	IGC128_HOT[7:0]								Current Channel Gain (128) Compensation - HOT Temp(307)	n.a.
0x0_40FC	3C	60	IGC256_COLD[7:0]								Current Channel Gain (256) Compensation - COLD Temp(307)	n.a.
0x0_40FD	3D	61	IGC256_HOT[7:0]								Current Channel Gain (256) Compensation - HOT Temp(307)	n.a.
0x0_40FE	3E	62	IGC512_COLD[7:0]								Current Channel Gain (512) Compensation - COLD Temp(307)	n.a.
0x0_40FF	3F	63	IGC512_HOT[7:0]								Current Channel Gain (512) Compensation - HOT Temp(307)	n.a.

Notes

306.Based on the selection of the voltage measurement source (VSENSE or VOPT) and the activation of chopper mode.

307.7 Bit character with bit 7 (MSB) as sign (0 = “+”; 1 = “-”) with the difference to the corresponding room temperature value (e.g. 10000010 = “-2”).